REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make change to figure 2 terminal connections, pin 7 $\overline{RE}$ description. Update document paragraphs to current requirements. - ro	18-04-03	C. SAFFLE
B	Update document to current requirements. - ro	23-08-03	J. ESCHMEYER
C	Update document per vendor request; part lead finish changed from Sn-Pb (finish B) to NiPdAu (finish E). Revise info in section 6.4 to obsolete previous part numbers and reflect new part numbers; no other changes to part. - cgh	26-03-16	J. ESCHMEYER

Vendor Item Drawing

Prepared in accordance with ASME Y14.24
The CAGE Code 16236 entity has been changed to DLA Weapons Support (Columbus).

Revision Status of Sheets																						
REV																						
SHEET																						
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C								
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14								

PMIC N/A

Original date of drawing
YY-MM-DD

10-03-18

PREPARED BY
RICK OFFICER

CHECKED BY
RAJESH PITHADIA

APPROVED BY
CHARLES F. SAFFLE

DLA WEAPONS SUPPORT
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/landandmaritime

TITLE
MICROCIRCUIT, LINEAR, 16 Mbps, FAIL SAFE, LOW POWER, RS-485 / RS-422 RECEIVER, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/10601
REV C		PAGE 1 OF 14

AMSC N/A
5962-V028-26

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 16 Mbps, fail safe, low power, RS-485 / RS-422 receiver microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/10601	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ISL3282	16 Mbps, fail safe, low power, RS-485 / RS-422 receiver

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	See figure 1	Thin dual flat leadless plastic package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium 1/
F	Tin-lead alloy (BGA/CGA)
Z	Other

1/ The lead finish designator E alloy is gold flash palladium (NiPdAu or NiPdAuAg). Contact the manufacturer for more information.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) to GND	-0.3 V to 7 V
Logic supply (V_L) to GND	-0.3 V to (V_{CC} + 0.3) V
Input voltages:	
Receiver output enable ($\overline{RE}$)	-0.3 V to 7 V
Input/output voltages:	
Receiver inputs (A, B)	-8 V to +13 V
Receiver output (RO)	-0.3 V to (V_L + 0.3) V
Short circuit duration:	
Receiver output (RO)	Indefinite
Maximum junction temperature (T_J)	+150°C
Maximum storage temperature range	-65°C to +150°C
Power dissipation (P_D) with output shorted	467.5 mW
Thermal resistance, junction to case (θ_{JC}):	
X package	8°C/W 2/
Thermal resistance, junction to ambient (θ_{JA}):	
X package	65°C/W 3/

1.4 Recommended operating conditions. 4/

Supply voltage range (V_{CC})	3.0 V to 5.5 V
Operating free-air temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ For θ_{JC}, the case temperature measurement location is the center of the exposed metal pad on the package underside.

3/ θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See manufacturer’s tech brief TB379.

4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 - Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

International Electrotechnical Commission

IEC 61000-4-2 - Electromagnetic Compatibility (EMC) - Part 4-2:
Testing and measurement techniques - Electrostatic discharge immunity test

(Copies of these documents are available from https://www.iec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Data rate table. The data rate table shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuits. The timing waveforms and test circuits shall be as shown in figures 5 and 6.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ V_{CC} = 3.0 V to 5.5 V, $V_L = V_{CC}$, unless otherwise specified	Temperature, T_A	Device type	Limits 3/		Unit
					Min	Max	
DC CHARACTERISTICS.							
Input high voltage 4/ $\overline{RE}$	V_{IH1}	$V_L = V_{CC}$. $V_{CC} \le 3.6$ V	-55°C to +125°C	01	2	---	V
	V_{IH2}	$V_L = V_{CC}$. $V_{CC} \le 5.5$ V			2.4	---	
	V_{IH3}	2.7 V $\le V_L <$ 3.0 V			1.7	---	
	V_{IH4}	2.3 V $\le V_L <$ 2.7 V			1.6	---	
	V_{IH5}	1.6 V $\le V_L <$ 2.3 V			0.72 x V_L	---	
	V_{IH6}	1.35 V $\le V_L <$ 1.6 V 5/	+25°C		0.5 x V_L typical		
Input low voltage 4/ $\overline{RE}$	V_{IL1}	$V_L = V_{CC}$	-55°C to +125°C	01	---	0.7	V
	V_{IL2}	$V_L \ge 2.7$ V			---	0.7	
	V_{IL3}	2.3 V $\le V_L \le$ 2.7 V			---	0.6	
	V_{IL4}	1.6 V $\le V_L \le$ 2.3 V			---	0.25 x V_L	
	V_{IL5}	1.35 V $\le V_L \le$ 1.6 V 5/	+25°C		0.33 x V_L typical		
Logic input current	I_{IN1}	$\overline{RE}$ = 0 V or V_{CC}	-55°C to +125°C	01	-15	15	µA
Input current (A, B)	I_{IN2}	V_{IN} = 12 V, V_{CC} = 0 V, 3.6 V, or 5.5 V	-55°C to +125°C	01	---	125	µA
		V_{IN} = -7 V, V_{CC} = 0 V, 3.6 V, or 5.5 V			-100	---	
Receiver differential threshold voltage	V_{TH}	-7 V $\le V_{CM} \le$ 12 V	-55°C to +125°C	01	-200	-50	mV
Receiver input hysteresis	ΔV_{TH}	V_{CM} = 0 V 5/	+25°C	01	15 typical		mV

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions 2/ V_{CC} = 3.0 V to 5.5 V, $V_L = V_{CC}$, unless otherwise specified	Temperature, T_A	Device type	Limits 3/		Unit
					Min	Max	
DC CHARACTERISTICS - continued.							
Receiver input resistance	R_{IN}	-7 V ≤ V_{CM} ≤ 12 V 5/	-55°C to +125°C	01	150 typical		kΩ
Receiver short circuit current	I_{OSR}	0 V ≤ V_O ≤ V_{CC}	-55°C to +125°C	01	±7	±85	mA
Receiver output high voltage	V_{OH1}	I_O = 3.5 mA, V_{ID} = -50 mV, $V_L = V_{CC}$	-55°C to +125°C	01	V_{CC} – 0.4	---	V
	V_{OH2}	I_O = -1 mA, V_L ≥ 1.6 V			V_L – 0.4	---	
	V_{OH3}	I_O = -500 µA, V_L = 1.5 V			1.2	---	
	V_{OH4}	I_O = -150 µA, V_L = 1.35 V			1.15	---	
	V_{OH5}	I_O = -100 µA, V_L ≥ 1.35 V			V_L – 0.1	---	
Receiver output low voltage	V_{OL1}	I_O = 4 mA, V_{ID} = -200 mV, V_L ≥ 2.2 V	-55°C to +125°C	01	---	0.4	V
	V_{OL2}	I_O = 2 mA, V_L ≥ 1.5 V			---	0.4	
	V_{OL3}	I_O = 1 mA, V_L ≥ 1.35 V			---	0.4	
	V_{OL4}	I_O = 500 µA, V_L ≥ 1.35 V 5/	+25°C		0.1 typical		
Three-state (high impedance) receiver output current 4/	I_{OZR}	0 V ≤ V_O ≤ V_{CC}	-55°C to +125°C	01	-1	1	µA
SUPPLY CURRENT.							
No load supply current	I_{CC}	$\overline{RE}$ = V_{CC} / 0 V	-55°C to +125°C	01	---	500	µA
Shutdown supply current	I_{SHDN}	$\overline{RE}$ = 0 V / V_{CC}	-55°C to +125°C	01	---	20	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions 2/ V_{CC} = 3.0 V to 5.5 V, $V_L = V_{CC}$, unless otherwise specified	Temperature, T_A	Device type	Limits 3/		Unit
					Min	Max	
ESD PERFORMANCE.							
RS-485 pins (A, B)		IEC61000-4-2, air gap discharge method 5/	+25°C	01	±16.5 typical		kV
		IEC61000-4-2, contact discharge method 5/			±9 typical		
		Human body model (HBM), from bus pins to GND 5/			±16.5 typical		
All pins		Human body model (HBM) per MIL-STD-883, method 3015 3/	+25°C	01	±5 typical		kV
		Machine model (MM) 5/			±250 typical		V
RECEIVER SWITCHING CHARACTERISTICS.							
Maximum data rate	f_{MAX}	V_{ID} = ±2 V, V_{CM} = 0 V, see figures 4 and 5	-55°C to +125°C	01	16	---	Mbps
Receiver input to output delay	t_{PLH}, t_{PHL}	V_{ID} = ±2 V, V_{CM} = 0 V, see figure 5	-55°C to +125°C	01	20	60	ns
		$V_L \geq$ 1.5 V, see figure 5 5/	+25°C		44 typical		
Receiver skew $\lvert t_{PLH} - t_{PHL} \rvert$	t_{SK1}	V_{CC} = 3.3 V ±10%, see figure 5, $V_L = V_{CC}$	-55°C to +125°C	01	---	5.5	ns
	t_{SK2}	V_{CC} = 5 V ±10%, see figure 5, $V_L = V_{CC}$			---	7.5	
	t_{SK3}	$V_L \geq$ 1.8 V, see figure 5 5/	+25°C		2 typical		
	t_{SK4}	V_L = 1.5 V, see figure 5 5/			4 typical		
Receiver enable to output high	t_{ZH}	R_L = 1 kΩ, C_L = 15 pF, SW = GND, see figure 6	-55°C to +125°C	01	---	500	ns
		R_L = 1 kΩ, C_L = 15 pF, V_{CC} = 3.3 V, $V_L \geq$ 1.5 V, SW = GND, see figure 6	+25°C		250 typical		
		R_L = 1 kΩ, C_L = 15 pF, V_{CC} = 5 V, $V_L \geq$ 1.5 V, SW = GND, see figure 6	+25°C		120 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions 2/ V_{CC} = 3.0 V to 5.5 V, $V_L = V_{CC}$, unless otherwise specified	Temperature, T_A	Device type	Limits 3/		Unit
					Min	Max	
RECEIVER SWITCHING CHARACTERISTICS - continued.							
Receiver enable to output low	t_{ZL}	R_L = 1 kΩ, C_L = 15 pF, SW = V_{CC}, see figure 6	-55°C to +125°C	01	---	500	ns
		R_L = 1 kΩ, C_L = 15 pF, V_{CC} = 3.3 V, $V_L \geq$ 1.5 V, SW = V_{CC}, see figure 6	+25°C		250 typical		
		R_L = 1 kΩ, C_L = 15 pF, V_{CC} = 5 V, $V_L \geq$ 1.5 V, SW = V_{CC}, see figure 6	+25°C		120 typical		
Receiver disable from output high	t_{HZ}	R_L = 1 kΩ, C_L = 15 pF, SW = GND, see figure 6	-55°C to +125°C	01	---	20	ns
		R_L = 1 kΩ, C_L = 15 pF, V_{CC} = 3.3 V, $V_L \geq$ 1.5 V, SW = GND, see figure 6	+25°C		24 typical		
		R_L = 1 kΩ, C_L = 15 pF, V_{CC} = 5 V, $V_L \geq$ 1.5 V, SW = GND, see figure 6	+25°C		20 typical		
Receiver disable from output low	t_{LZ}	R_L = 1 kΩ, C_L = 15 pF, SW = V_{CC}, see figure 6	-55°C to +125°C	01	---	20	ns
		R_L = 1 kΩ, C_L = 15 pF, V_{CC} = 3.3 V, $V_L \geq$ 1.5 V, SW = V_{CC}, see figure 6	+25°C		24 typical		
		R_L = 1 kΩ, C_L = 15 pF, V_{CC} = 5 V, $V_L \geq$ 1.5 V, SW = V_{CC}, see figure 6	+25°C		20 typical		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature ranges. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ All currents into device pins are positive; all currents out of device pins are negative. All voltages are referred to device ground unless otherwise specified.

3/ Parts are tested 100% at +25°C. Over-temperature limits are established by characterization and are not production tested.

4/ If the RX enable function isn't needed, connect the enable pin to the appropriate supply, as described in figure 2.

5/ Parameters with a single typical entry apply to V_{CC} = 3.3 V and 5.5 V.

Case X

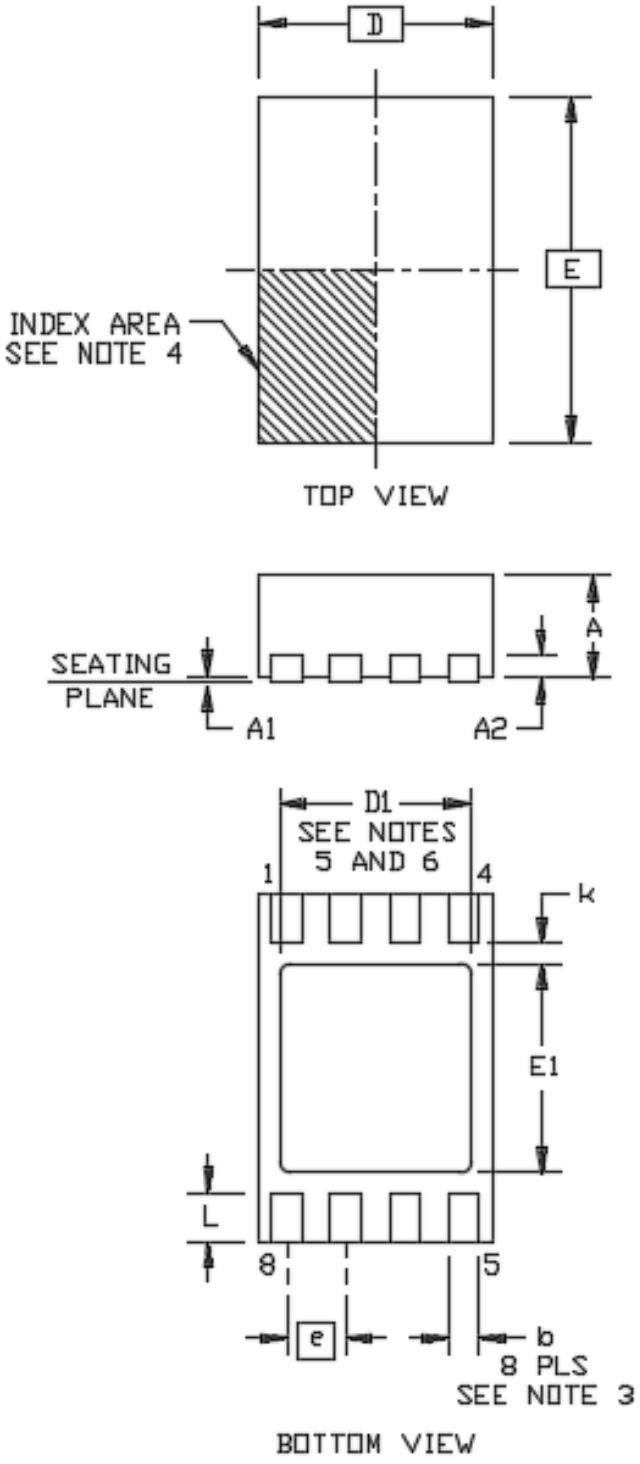


FIGURE 1. Case outline.

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
A	0.027	0.031	0.70	0.80	---
A1	---	0.002	---	0.05	---
A2	0.007 REF		0.20 REF		---
b	0.007	0.012	0.20	0.32	3, 6
D	0.078 BSC		2.00 BSC		---
D1	0.059	0.068	1.50	1.75	5, 6
E	0.118 BSC		3.00 BSC		---
E1	0.064	0.074	1.65	1.90	5, 6
e	0.019 BSC		0.50 BSC		---
k	0.007	---	0.20	---	---
L	0.011	0.019	0.30	0.50	6
N	8				7

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5-1994.
3. Dimension b applies to the metalized terminal and is measured between 0.25 mm (0.009 inch) and 0.30 mm (0.011 inch) from the terminal tip.
4. The configuration of the number one pin identifier is optional, but must be located within the zone indicated. The number one pin identifier may be either a mold or mark feature.
5. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
6. Nominal dimensions are provided to assist with the printed circuit board land pattern design efforts, see manufacturer's technical brief TB389.
7. Number of terminals.

FIGURE 1. Case outline - continued.

Device type	01	
Case outlines	X	
Terminal number	Terminal symbol	Description
1	RO	Receiver output: - If (A – B) ≥ -50 mV, RO is high - If (A – B) ≤ -200 mV, RO is low - RO = high if A and B are unconnected (floating) or shorted.
2	GND	Ground connection. This is also the potential of the thin dual flat leadless package thermal pad.
3	NC	No connection.
4	V_{CC}	System power supply input (3.0 V to 5.5 V). In reference to the V_L pin, power up V_{CC} first.
5	A	±16.5 V IEC61000 ESD protected RS-485, RS-422 level, non-inverting receiver input.
6	V_L	Logic-level supply which sets the V_{IL}/V_{IH} levels for the DI and DE pins. Power-up this supply after V_{CC}, and keep $V_L \leq V_{CC}$.
7	$\overline{RE}$	Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high. If the Rx enable function isn't used, connect $\overline{RE}$ directly to GND. Resistor to V_{CC}. $\overline{RE}$ is internally pulled high.
8	B	±16.5 V IEC61000 ESD protected RS-485, RS-422 level, inverting receiver input.

FIGURE 2. Terminal connections.

Receiver		
Inputs		Output
$\overline{RE}$	A - B	RO
0	≥ -0.05 V	1
0	≤ -0.2 V	0
0	Inputs open / shorted	1
1	X	High Z (Shutdown mode)

X = Don’t care

FIGURE 3. Truth table.

V_L (Volts)	V_{IH} (Volts)	V_{IL} (Volts)	Data rate (Mbps)
1.35	0.55	0.5	11
1.6	0.7	0.6	16
1.8	0.8	0.7	23
2.3	1	0.9	27
2.7	1.1	1	30
3.3	1.3	1.2	30
5.5	2	1.8	24

V_{IH}, V_{IL}, and data rate versus V_L for V_{CC} = 3.3 V or 5.5 V

FIGURE 4. Data rate table.

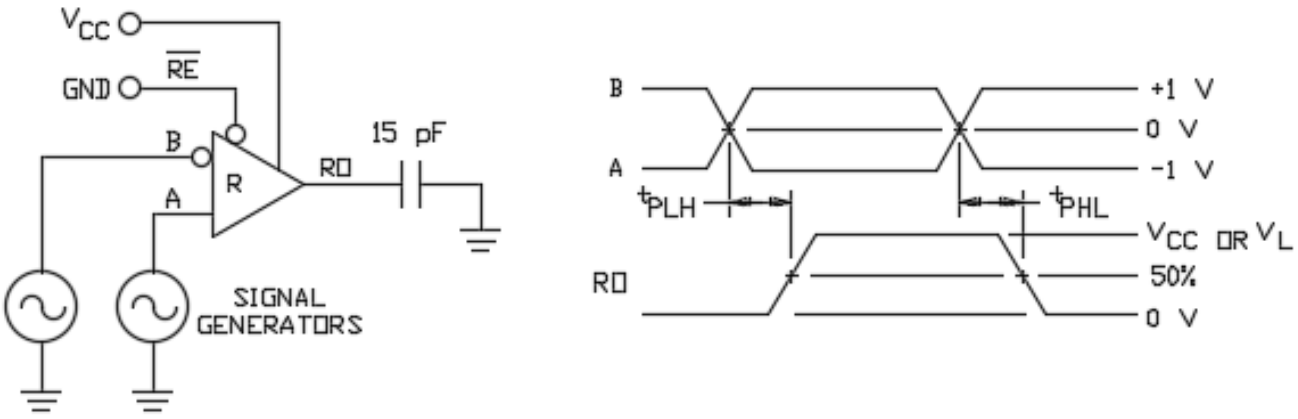
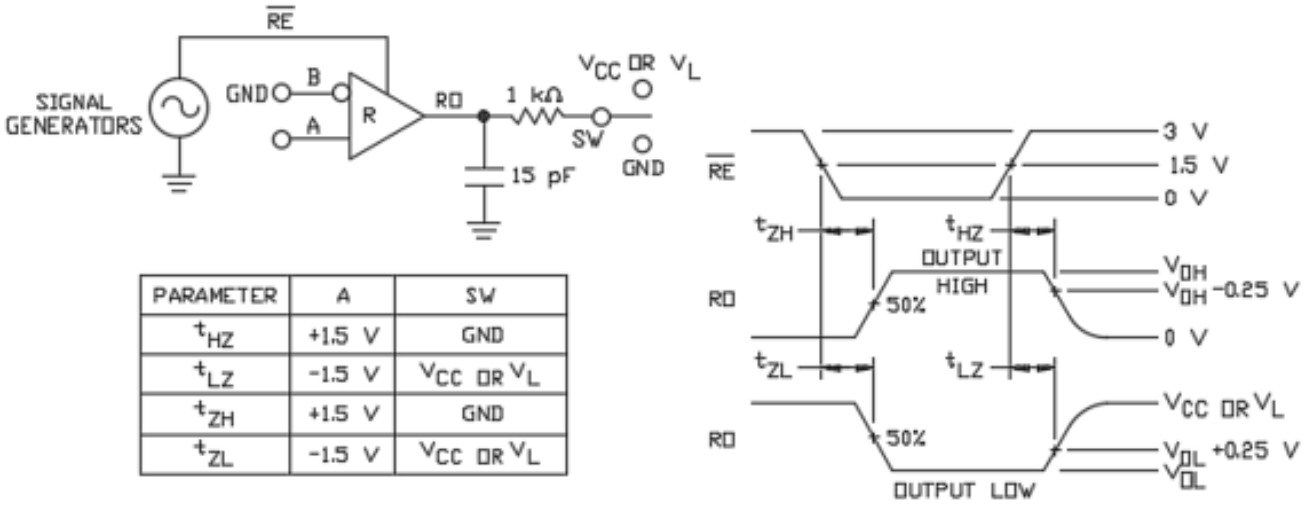


FIGURE 5. Receiver propagation delay and data rate.



PARAMETER	A	SW
t_{HZ}	+1.5 V	GND
t_{LZ}	-1.5 V	V_{CC} OR V_L
t_{ZH}	+1.5 V	GND
t_{ZL}	-1.5 V	V_{CC} OR V_L

FIGURE 6. Receiver enable and disable times.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source of supply. Identification of the suggested source of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Weapons Support (Columbus) maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Top side marking	Vendor part number 2/
V62/10601-01XB	3/	282	ISL3282EMRTEP-T ISL3282EMRTEP-TK
V62/10601-01XE	34371	82Z	ISL3282EMRTEPZ-TK

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Add suffix -T for 6 thousand pieces per reel.
Add suffix -TK for 1 thousand pieces per reel.
3/ Not available from an approved source of supply. Last known supplier CAGE 34371 is listed below.

CAGE code	Source of supply
34371	Renesas Electronics America 1650 Robert J Conlan Blvd NE Palm Bay, FL 32905