REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
PAGE	40	41	42	43	44	45	46	47	48	49	50	51	52	53								
REV																						
PAGE	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39

REV STATUS OF PAGES	REV																	
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

PMIC N/A	PREPARED BY Phu H. Nguyen	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**
Original date of drawing YY MM DD 10-06-22	CHECKED BY Phu H. Nguyen APPROVED BY Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL, FIXED POINT DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON
	SIZE: A CODE IDENT. NO.: 16236	DWG NO. **V62/09647**
	REV: A	PAGE 1 OF 53

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance Fixed-Point Digital Signal Processor microcircuit, with an operating temperature range of -55°C to +85°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/09647	-	01	X	A
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s). 1/

Device type	Generic	Circuit function
01	SM320VC5507-EP	Fixed Point Digital Signal Processor

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	Package style
X	144	Plastic ball grid array

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage I/O range, (DV_{DD}) ..... -0.3 V to +4.0 V 4/
Supply voltage core range, (CV_{DD}) ..... -0.3 V to +2.0 V 4/
Input voltage range, (V_I) ..... -0.3 V to +4.5 V
Output voltage range (V_O) ..... -0.3 V to +4.5 V
Operating case temperature ranges, (T_C): (Extended) ..... -55°C to +85°C
Storage temperature range, (T_{STG})..... -55°C to +150°C

1/ Users are cautioned to review the manufacturers data manual for additional user information relating to this device.
2/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
3/ Long term high temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See manufacturer data for additional information on enhanced plastic packaging.
4/ All voltage values are with respect to V_{SS}.

1.4 Recommended operating conditions. 5/

For CV_{DD} = 1.2 V (108 MHz)

CORE
Device supply voltage (CV_{DD}) ..... +1.14 V to +1.26 V
PERIPHERALS
RTC module supply voltage, core (RCV_{DD}) ..... +1.14 V to +1.26 V
RTC module supply voltage, I/O (RTCINX1 and RTCINX2), (RDV_{DD}) ..... +1.14 V to +1.26 V
USBPLL supply voltage, ($USBPLLV_{DD}$) ..... +1.14 V to +1.26 V 6/
USB module supply voltage, I/O (DP, DN, and PU), ($USBV_{DD}$) ..... +3.0 V to +3.6 V
Device supply voltage, I/O (except DP, DN, PU, SDA, SCL), (DV_{DD})..... +2.7 V to +3.6 V 7/
A/D module digital supply voltage, (ADV_{DD}) ..... +2.7 V to +3.6 V
A/D module analog supply voltage, (AV_{DD}) ..... +2.7 V to +3.6 V
GROUNDS
Supply voltage, GND, I/O, and core (V_{SS}) ..... 0 V
Supply voltage, GND, A/D module, digital (ADV_{SS}) ..... 0 V
Supply voltage, GND, A/D module, analog (AV_{SS}) ..... 0 V
Supply voltage, GND, USBPLL ($USBPLLV_{SS}$) ..... 0 V
High level input voltage, I/O (V_{IH}):
DN and DP ..... +2 V minimum 8/
SDA and SCL: V_{DD} related input level ..... 0.7 x DV_{DD} to DV_{DD} (max) + 0.5 V 7/
All other inputs (including hysteresis inputs) ..... +2 V to DV_{DD} +0.3 V
Low level input voltage, I/O (V_{IL}):
DN and DP ..... +0.8 V maximum 8/
SDA and SCL: V_{DD} related input level ..... -0.5 V to0.3 x DV_{DD} 7/
All other inputs (including hysteresis inputs) ..... -0.3 V to +0.8 V
Hysteresis level, (V_{hys}) – Inputs with hysteresis only ..... 0.1 x DV_{DD}
High level output current, (I_{OH}):
DN and DP (V_{OH} = 2.45 V) ..... -17 mA max 8/
All other outputs ..... - 4 mA max
Low level output current, (I_{OL}):
DN and DP (V_{OL} = 0.36 V) ..... 17mA min 8/
SDA and SCL ..... 3 mA max
All other outputs ..... 4 mA max
Operating case temperature (T_C) ..... -55°C to +85°C

5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
6/ USB PLL is susceptible to power supply ripple. The maximum allowable supply ripple is 1% for 1 Hz to 5 kHz; 1.5% for 5 kHz to 10 MHz; 3% for 10 MHz to 100 MHz , and less than 5% for 100 MHz or greater.
7/ The I^2C pins SDA and SCL do not feature fail-safer I/O buffers. These pins could potentially draw current when the device is powered down. Due to the fact that different voltage devices can be connected to the I^2C bus, the level of logic 0 (low) and logic 1 (high) are not fixed and depends on the associated V_{DD}.
8/ USB I/O pins DP and DN can tolerate a short circuit at D+ and D- to 0 V or 5 V, as long as the recommended series resistors (see Figure 40) are connected between the D+ and DP (package), and the D- and DN (package). Do not apply a short circuit to the USB I/O pins DP and DN in absence of the series resistors.

1.4 Recommended operating conditions - Continued.

For CV_{DD} = 1.35 V (144 MHz)

CORE

Device supply voltage (CV_{DD}) ..... +1.28 V to +1.42 V

PERIPHERALS

RTC module supply voltage, core (RCV_{DD}) ..... +1.28 V to +1.42 V
RTC module supply voltage, I/O (RTCINX1 and RTCINX2), (RDV_{DD}) ..... +1.28 V to +1.42 V
USBPLL supply voltage, ($USBPLLV_{DD}$) ..... +1.28 V to +1.42 V 6/
USB module supply voltage, I/O (DP, DN, and PU), ($USBV_{DD}$) ..... +3.0 V to +3.6 V
Device supply voltage, I/O (except DP, DN, PU, SDA, SCL), (DV_{DD})..... +2.7 V to +3.6 V 7/
A/D module digital supply voltage, (ADV_{DD}) ..... +2.7 V to +3.6 V
A/D module analog supply voltage, (AV_{DD}) ..... +2.7 V to +3.6 V

GROUNDS

Supply voltage, GND, I/O, and core (V_{SS}) ..... 0 V
Supply voltage, GND, A/D module, digital (ADV_{SS}) ..... 0 V
Supply voltage, GND, A/D module, analog (AV_{SS}) ..... 0 V
Supply voltage, GND, USBPLL ($USBPLLV_{SS}$) ..... 0 V

High level input voltage, I/O (V_{IH}):
DN and DP ..... +2 V minimum 8/
SDA and SCL: V_{DD} related input level ..... 0.7 x DV_{DD} to DV_{DD} (max) + 0.5 V 7/
All other inputs (including hysteresis inputs) ..... +2 V to DV_{DD} +0.3 V

Low level input voltage, I/O (V_{IL}):
DN and DP ..... +0.8 V maximum 8/
SDA and SCL: V_{DD} related input level ..... -0.5 V to0.3 x DV_{DD} 7/
All other inputs (including hysteresis inputs) ..... -0.3 V to +0.8 V

Hysteresis level, (V_{hys}) – Inputs with hysteresis only ..... 0.1 x DV_{DD}

High level output current, (I_{OH}):
DN and DP (V_{OH} = 2.45 V) ..... -17 mA max 8/
All other outputs ..... - 4 mA max

Low level output current, (I_{OL}):
DN and DP (V_{OL} = 0.36 V) ..... 17mA min 8/
SDA and SCL ..... 3 mA max
All other outputs ..... 4 mA max

Operating case temperature (T_C) ..... -55°C to +85°C

1.4 Recommended operating conditions - Continued.

For CV_{DD} = 1.6 V (200 MHz)

CORE
Device supply voltage (CV_{DD}) ..... +1.55 V to +1.65 V
PERIPHERALS
RTC module supply voltage, core (RCV_{DD}) ..... +1.55 V to +1.65 V
RTC module supply voltage, I/O (RTCINX1 and RTCINX2), (RDV_{DD}) ..... +1.55 V to +1.65 V
USBPLL supply voltage, ($USBPLLV_{DD}$) ..... +1.55 V to +1.65 V 6/
USB module supply voltage, I/O (DP, DN, and PU), ($USBV_{DD}$) ..... +3.0 V to +3.6 V
Device supply voltage, I/O (except DP, DN, PU, SDA, SCL), (DV_{DD})..... +2.7 V to +3.6 V 7/
A/D module digital supply voltage, (ADV_{DD}) ..... +2.7 V to +3.6 V
A/D module analog supply voltage, (AV_{DD}) ..... +2.7 V to +3.6 V
GROUNDS
Supply voltage, GND, I/O, and core (V_{SS}) ..... 0 V
Supply voltage, GND, A/D module, digital (ADV_{SS}) ..... 0 V
Supply voltage, GND, A/D module, analog (AV_{SS}) ..... 0 V
Supply voltage, GND, USBPLL ($USBPLLV_{SS}$) ..... 0 V
High level input voltage, I/O (V_{IH}):
DN and DP ..... +2 V minimum 8/
SDA and SCL: V_{DD} related input level ..... 0.7 x DV_{DD} to DV_{DD} (max) + 0.5 V 7/
All other inputs (including hysteresis inputs) ..... +2 V to DV_{DD} +0.3 V
Low level input voltage, I/O (V_{IL}):
DN and DP ..... +0.8 V maximum 8/
SDA and SCL: V_{DD} related input level ..... -0.5 V to0.3 x DV_{DD} 7/
All other inputs (including hysteresis inputs) ..... -0.3 V to +0.8 V
Hysteresis level, (V_{hys}) – Inputs with hysteresis only ..... 0.1 x DV_{DD}
High level output current, (I_{OH}):
DN and DP (V_{OH} = 2.45 V) ..... -17 mA max 8/
All other outputs ..... - 4 mA max
Low level output current, (I_{OL}):
DN and DP (V_{OL} = 0.36 V) ..... 17mA min 8/
SDA and SCL ..... 3 mA max
All other outputs ..... 4 mA max
Operating case temperature (T_C) ..... -55°C to +85°C

Thermal resistance characteristics (ambient temperature)

Package	$R_{\theta JA}$(°C/W)	Board type 9/	Air flow (LFM)
Case outline X	71.2	High - K	0
	61.8	High - K	150
	58.9	High - K	250
	54.8	High - K	500
	103.6	Low - K	0
	84.2	Low - K	150
	77.8	Low - K	250
	69.4	Low - K	500

Thermal resistance characteristics (Case temperature)

Package	$R_{\theta JA}$(°C/W)	Board type 9/
Case outline X	13.8	2s JEDEC test card

9/ Board types are defined by JEDEC. Reference JEDEC standard JESD51-9. test board are array surface mount package.

2. APPLICABLE DOCUMENTS

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2

3.5.3 Functional block diagram. The functional block diagram shall be as specified in figure 3.

3.5.5 Timing waveforms. The timing waveforms shall be as shown in figure 4-40.

TABLE I. Electrical performance characteristics. 1/

Test		Symbol	Test condition 2/	Limits						Unit
				CV_{DD} -= 1.2 V (108 MHz)		CV_{DD} -= 1.35 V (144 MHz)		CV_{DD} -= 1.6 V (200 MHz)		
				Min	Max	Min	Max	Min	Max	
High level output voltage	DN and DP 3/	V_{OH}	$USBDV_{DD}$ = 3.0 V to 3.6 V I_{OH} = -300 µA	2.8	$USBV_{DD}$	2.8	$USBV_{DD}$	2.8	$USBV_{DD}$	V
	PU			0.9 x $USBV_{DD}$	$USBV_{DD}$	0.9 x $USBV_{DD}$	$USBV_{DD}$	0.9 x $USBV_{DD}$	$USBV_{DD}$	
	All other outputs		DV_{DD} = 2.7 V to 3.6 V I_{OH} = -300 µA	0.75 x DV_{DD}		0.75 x DV_{DD}		0.75 x DV_{DD}		
Low level output voltage	SDA & SCL 4/	V_{OL}	At 3 mA sink current	0	0.4	0	0.4	0	0.4	V
	DN and DP 3/		I_{OL} = 3.0 mA		0.3		0.3		0.3	
	All other outputs		I_{OL} = MAX		0.4		0.4		0.4	
Input current for outputs in high-impedance	Output-only or I/O pins with bus keepers (enabled)	I_{IZ}	DV_{DD} = MAX, V_O = V_{SS} to DV_{DD}	-300	300	-300	300	-300	300	µA
	All other output-only or I/O pins			-5	5	-5	5	-5	5	
Input current	Input pins with internal pulldown (enabled)	I_I	DV_{DD} = MAX, V_I = V_{SS} to DV_{DD}	30	300	30	300	30	300	µA
	Input pins with internal pullup (enabled)			-300	-30	-300	-30	-300	-30	
	X2/CLKIN			-50	50	-50	50	-50	50	
	All other input-only pins			-5	5	-5	5	-5	5	
Input capacitance		C_I		3 TYP		3 TYP		3 TYP		pF
Output capacitance		C_O		3 TYP		3 TYP		3 TYP		pF
For CV_{DD} = 1.2 V (108 MHz)										
CV_{DD} supply current, CPU + internal memory access 5/		I_{DDC}	CV_{DD} = 1.2 V, T_C = 25°C CPU clock = 108 MHz	0.45 TYP						mA/ MHz
DV_{DD} supply current, pins active 6/		I_{DDP}	DV_{DD} = 3.3 V, T_C = 25°C CPU clock = 108 MHz	5.5 TYP						mA
CV_{DD} supply current, standby 7/	Oscillator disabled. All domains in low – power state	I_{DDC}	CV_{DD} = 1.2 V, T_C = 25°C (Nominal process)	100 TYP						µA
DV_{DD} supply current, standby	Oscillator disabled. All domains in low – power state	I_{DDP}	DV_{DD} = 3.3 V, T_C = 25°C No I/O activity	10 TYP						µA

See footnote at end of table

TABLE I. Electrical performance characteristics - Continued. 1/

Test		Symbol	Test condition 2/	Limits						Unit
				CV_{DD} -= 1.2 V (108 MHz)		CV_{DD} -= 1.35 V (144 MHz)		CV_{DD} -= 1.6 V (200 MHz)		
				Min	Max	Min	Max	Min	Max	
For CV_{DD} = 1.35 V (144 MHz)										
CV_{DD} supply current, CPU + internal memory access 5/		I_{DDC}	CV_{DD} = 1.35 V, T_C = 25°C CPU clock = 144 MHz			0.51 TYP				mA/ MHz
DV_{DD} supply current, pins active 6/		I_{DDP}	DV_{DD} = 3.3 V, T_C = 25°C CPU clock = 144 MHz			5.5 TYP				mA
CV_{DD} supply current, standby 7/	Oscillator disabled. All domains in low – power state	I_{DDC}	CV_{DD} = 1.35 V, T_C = 25°C (Nominal process)			125 TYP				µA
DV_{DD} supply current, standby	Oscillator disabled. All domains in low – power state	I_{DDP}	DV_{DD} = 3.3 V, T_C = 25°C No I/O activity			10 TYP				µA
For CV_{DD} = 1.6 V (200 MHz)										
CV_{DD} supply current, CPU + internal memory access 5/		I_{DDC}	CV_{DD} = 1.6 V, T_C = 25°C CPU clock = 200 MHz					0.6 TYP		mA/ MHz
DV_{DD} supply current, pins active 6/		I_{DDP}	DV_{DD} = 3.3 V, T_C = 25°C CPU clock = 200 MHz					5.5 TYP		mA
CV_{DD} supply current, standby 7/	Oscillator disabled. All domains in low – power state	I_{DDC}	CV_{DD} = 1.6 V, T_C = 25°C (Nominal process)					150 TYP		µA
DV_{DD} supply current, standby	Oscillator disabled. All domains in low – power state	I_{DDP}	DV_{DD} = 3.3 V, T_C = 25°C No I/O activity					10 TYP		µA

See footnote at end of table

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/	Limits				Unit
				CV_{DD}= 1.2 V CV_{DD} = 1.35 V		CV_{DD} = 1.6 V		
				Min	Max	Min	Max	
CLOCK GENERATION IN BYPASS MODE (DPLL DISABLED)								
CLKIN timing requirements								
C1	Cycle time, X2/CLKIN	$t_{c(CI)}$	See figure 4	20	400 8/	20	400 8/	ns
C2	Fall time, X2/CLKIN	$t_{f(CI)}$			4		4	
C3	Rise time, X2/CLKIN	$t_{r(CI)}$			4		4	
C10	Pulse duration CLKIN low	$t_{w(CIL)}$		6		6		
C11	Pulse duration CLKIN high	$t_{w(CIH)}$		6		6		
CLKOUT switching characteristics								
C4	Cycle time, CLKOUT	$t_{c(CO)}$		20 9/	1600 10/	20 9/	1600 8/	ns
C5	Delay time, X2/CLKIN high to CLKOUT high/low	$t_{d(CI-CO)}$		5	25	5	25	
C6	Fall time, CLKOUT	$t_{f(CO)}$		1 TYP		1 TYP		
C7	Rise time, CLKOUT	$t_{r(CO)}$		1 TYP		1 TYP		
C8	Pulse duration CLKOUT low	$t_{w(COL)}$		H - 1	H + 1	H - 1	H + 1	
C9	Pulse duration CLKOUT high	$t_{w(COH)}$		H - 1	H + 1	H - 1	H + 1	
CLOCK GENERATION IN LOCK MODE (DPLL SYNTHESIS ENABLED)								
CLKIN timing requirements								
C1	Cycle time, X2/CLKIN	$t_{c(CI)}$	DPLL synthesis enabled	20	400 8/	20	400 8/	ns
C2	Fall time, X2/CLKIN	$t_{f(CI)}$			4		4	
C3	Rise time, X2/CLKIN	$t_{r(CI)}$			4		4	
C10	Pulse duration CLKIN low	$t_{w(CIL)}$		6		6		
C11	Pulse duration CLKIN high	$t_{w(CIH)}$		6		6		
Multiply by N clock operation switching characteristics See figure 5								
C4	Cycle time, CLKOUT	$t_{c(CO)}$	for CV_{DD} = 1.2 V	9.26	1600	5	1600	ns
C4	Cycle time, CLKOUT	$t_{c(CO)}$	for CV_{DD} = 1.35 V	6.95	1600	5	1600	
C6	Fall time, CLKOUT	$t_{f(CO)}$		1 TYP		1 TYP		
C7	Rise time, CLKOUT	$t_{r(CO)}$		1 TYP		1 TYP		
C8	Pulse duration CLKOUT low	$t_{w(COL)}$		H - 1	H + 1	H - 1	H + 1	
C9	Pulse duration CLKOUT high	$t_{w(COH)}$		H - 1	H + 1	H - 1	H + 1	
C12	Delay time, X2/CLKIN high to CLKOUT high/low	$t_{d(CI-CO)}$		5	25	5	25	

No	Test	Symbol	Test condition 2/	Limits		Unit
				Min	Max	
REAL TIME CLOCK OSCILLATOR WITH EXTERNAL CRYSTAL						
Recommended RTC crystal parameters						
	Frequency of oscillation 11/	f_o	See figure 6	32.768		kHz
	Series resistance 11/	ESR		30	60	kΩ
	Load capacitance	C_L		12.5 TYP		pF
	Crystal drive level	DL			1	µW

See footnote at end of table

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/	Limits				Unit
				CV_{DD}= 1.2 V CV_{DD} = 1.35 V		CV_{DD} = 1.6 V		
				Min	Max	Min	Max	
	ASYNCHRONUOS MEMORY TIMINGS							
Asynchronous memory cycle timing requirements								
M1	Setup time, read data valid before CLKOUT high 12/	$t_{su(DV-COH)}$	See figure 7 and 8	6		5		ns
M2	Hold time, read data after CLKOUT high	$t_{h(COH-DV)}$		0		0		
M3	Setup time, ARDY valid before CLKOUT high 12/	$t_{su(ARDY-COH)}$		10		7		
M4	Hold time, ARDY after CLKOUT high	$t_{h(COH-ARDY)}$		0		0		
Asynchronous memory cycle switching characteristics								
M5	Delay time, CLKOUT high to $\overline{\mathrm{CEx}}$ valid	$t_{d(COH-CEV)}$	See figure 7 and 8	-2	4	-2	4	ns
M6	Delay time, CLKOUT high to $\overline{\mathrm{CEx}}$ invalid	$t_{d(COH-CEIV)}$		-2	4	-2	4	
M7	Delay time, CLKOUT high to $\overline{\mathrm{BEx}}$ valid	$t_{d(COH-}$			4		4	
M8	Delay time, CLKOUT high to $\overline{\mathrm{BEx}}$ invalid	$t_{d(COH-}$		-2		-2		
M9	Delay time, CLKOUT high to address valid	$t_{d(COH-}$			4		4	
M10	Delay time, CLKOUT high to address invalid	$t_{d(COH-}$		-2		-2		
M11	Delay time, CLKOUT high to $\overline{\mathrm{AOE}}$ valid	$t_{d(COH-}$		-2	4	-2	4	
M12	Delay time, CLKOUT high to $\overline{\mathrm{AOE}}$ invalid	$t_{d(COH-}$		-2	4	-2	4	
M13	Delay time, CLKOUT high to $\overline{\mathrm{ARE}}$ valid	$t_{d(COH-}$		-2	4	-2	4	
M14	Delay time, CLKOUT high to $\overline{\mathrm{ARE}}$ invalid	$t_{d(COH-}$		-2	4	-2	4	
M15	Delay time, CLKOUT high to data valid	$t_{d(COH-}$			4		4	
M16	Delay time, CLKOUT high to data invalid	$t_{d(COH-}$		-2		-2		
M17	Delay time, CLKOUT high to $\overline{\mathrm{AWE}}$ valid	$t_{d(COH-}$		-2	4	-2	4	
M18	Delay time, CLKOUT high to $\overline{\mathrm{AWE}}$ invalid	$t_{d(COH-}$		-2	4	-2	4	

See footnote at end of table

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/	Limits				Unit
				CV_{DD}= 1.2 V CV_{DD} = 1.35 V		CV_{DD} = 1.6 V		
				Min	Max	Min	Max	
	SYNCHRONOUS DRAM (SDRAM) TIMINGS							
Synchronous DRAM cycle timing requirements								
M19	Setup time, read data valid before CLKMEN high	$t_{su(DV-CLKMENH)}$	See figure 9-15	3		3		ns
M20	Hold time, read data valid after CLKMEN high	$t_{h(CLKMENH-DV)}$		2		2		
M21	Cycle time, CLKMEN	$t_{c(CLKMEN)}$		9.26 13/		7.52 13/		
Synchronous DRAM cycle switching characteristics								
M22	Delay time, CLKMEM high to CEx low	$t_{d(CLKMEMH-CEL)}$	See figure 9-15	1.2	7	1.2	5	ns
M23	Delay time, CLKMEM high to CEx high	$t_{d(CLKMEMH-CEH)}$		1.2	7	1.2	5	
M24	Delay time, CLKMEM high to BEx valid	$t_{d(CLKMEMH-BEV)}$		1.2	7	1.2	5	
M25	Delay time, CLKMEM high to HBEx invalid	$t_{d(CLKMEMH-BEIV)}$		1.2	7	1.2	5	
M26	Delay time, CLKMEM high to address valid	$t_{d(CLKMEMH-AV)}$		1.2	7	1.2	5	
M27	Delay time, CLKMEM high to address invalid	$t_{d(CLKMEMH-AIV)}$		1.2	7	1.2	5	
M28	Delay time, CLKMEM high to SDCAS low	$t_{d(CLKMEMH-SDCASL)}$		1.2	7	1.2	5	
M29	Delay time, CLKMEM high to SDCAS high	$t_{d(CLKMEMH-SDCAH)}$		1.2	7	1.2	5	
M30	Delay time, CLKMEM high to data valid	$t_{d(CLKMEMH-DV)}$		1.2	7	1.2	5	
M31	Delay time, CLKMEM high to data invalid	$t_{d(CLKMEMH-DIV)}$		1.2	7	1.2	5	
M32	Delay time, CLKMEM high to SDWE low	$t_{d(CLKMEMH-SDWEL)}$		1.2	7	1.2	5	
M33	Delay time, CLKMEM high to SDWE high	$t_{d(CLKMEMH-SDWEH)}$		1.2	7	1.2	5	
M34	Delay time, CLKMEM high to SDA10 valid	$t_{d(CLKMEMH-SDA10V)}$		1.2	7	1.2	5	
M35	Delay time, CLKMEM high to SDA10 invalid	$t_{d(CLKMEMH-SDA10IV)}$		1.2	7	1.2	5	
M36	Delay time, CLKMEM high to SDRAS low	$t_{d(CLKMEMH-SDRASL)}$		1.2	7	1.2	5	
M37	Delay time, CLKMEM high to SDRAS high	$t_{d(CLKMEMH-SDRASH)}$		1.2	7	1.2	5	
M38	Delay time, CLKMEM high to CKE low	$t_{d(CLKMEMH-CKEL)}$		1.2	7	1.2	5	
M39	Delay time, CLKMEM high to CKE high	$t_{d(CLKMEMH-CKEH)}$		1.2	7	1.2	5	

See footnote at end of table

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/	Limits				Unit
				CV_{DD}= 1.2 V CV_{DD} = 1.35 V		CV_{DD} = 1.6 V		
				Min	Max	Min	Max	
POWER UP RESET (ON CHIP OSCILLATOR ACTIVE)								
Timing requirements								
R1	Hold time, $\overline{RESET}$ low after oscillator stable 16/	$t_{h(SUPSTBL-RSTL)}$	See figure 16	3P 15/		3P 15/		ns
POWER UP RESET (ON CHIP OSCILLATOR INACTIVE)								
Timing requirements								
R2	Hold time, CLKOUT valid to $\overline{RESET}$ low	$t_{h(CLKOUTV-RSTL)}$	See figure 16	3P 15/		3P 15/		
Switching characteristics								
R3	Delay time, CLKIN valid to CLKOUT valid	$t_{d(CLKINV-CLKOUTV)}$	See figure 16		30		30	ns
WARM RESET								
Reset timing requirements								
R4	Pulse width, reset low	$t_{w(RSL)}$	See figure 5-	3P 15/		3P 15/		ns
Reset switching characteristics 15/								
R5	Delay time, reset high to BK group valid 17/	$t_{d(RSTH-BKV)}$	See figure 18		38P+15		38P+15	ns
R6	Delay time, reset high to High group valid 18/	$t_{d(RSTH-HIGHV)}$			38P+15		38P+15	
R7	Delay time, reset low to Z group valid 19/	$t_{d(RSTL-ZIV)}$			1P+15		1P+15	
R8	Delay time, reset high to Z group valid 19/	$t_{d(RSTH-ZV)}$			38P+15		38P+15	
EXTERNAL INTERRUP TIMING								
External interrupt timing requirements 15/								
I1	Pulse width, interrupt high, CPU active	$t_{w(INTH)A}$	See figure 19	2P		2P		ns
I2	Pulse width, interrupt low, CPU active	$t_{w(INTL)A}$		3P		3P		
WAKE UP FROM IDLE								
Wake up from IDLE switching characteristics 15/								
ID1	Delay time, wake up event low to clock generation enable (CPU and clock domain idle)	$t_{d(WKPEVTL-CLKGEN)}$	See figure 20	1.25 TYP 20/		1.25 TYP 20/		ns
ID2	Hold time, clock generation enable to wake up event low (CPU and clock domain in idle)	$t_{d(CLKGEN-WKPEVTL)}$		3P 21/		3P 21/		
ID3	Pulse width, wake up event low (for CPU idle only)	$t_{w(WKPEVTL)}$		3P		3P		

See footnote at end of table

TABLE I. Electrical performance characteristics – Continued. 1/

No	Test		Symbol	Test condition 2/	Limits				Unit
					CV_{DD}= 1.2 V CV_{DD} = 1.35 V		CV_{DD} = 1.6 V		
					Min	Max	Min	Max	
XF TIMINGS									
XF switching characteristics									
X1	Delay time, CLKOUT high to XF high		$t_{d(XF)}$	See figure 21	-1	3	-1	3	ns
	Delay time, CLKOUT high to XF high				-1	3	-1	3	
GENERAL PURPOSE INPUT/OUTPUT (GPIOx) TIMINGS									
GPIO pins configured as Inputs timing requirements									
G1	Setup time, IOx input valid before CLKOUT high	GPIO	$t_{su(GPIO-COH)}$	See figure 22	4		4		ns
		AGPIO 22/			8		8		
		EHPIGPIO 23/			8		8		
G2	Hold time, IOx input valid after CLKOUT high	GPIO	$t_{h(COH-GPIO)}$		0		0		
		AGPIO 22/			0		0		
		EHPIGPIO 23/			0		0		
GPIO configured as outputs switching characteristics									
G3	Delay time, CLKOUT high to IOx output change	GPIO	$t_{d(COH-GPIO)}$	See figure 22	0	6	0	6	ns
		AGPIO 22/			0	11	0	11	
		EHPIGPIO 23/			0	13	0	13	
TIN/TOUT TIMINGS (TIMER0 ONLY)									
TIN/TOUT pins configured as inputs timing requirements 15/ 24/									
T4	Pulse width, TIN/TOUT low		$t_{w(TIN/TOUTL)}$	See figure 23	2P+1		2P+1		ns
T5	Pulse width, TIN/TOUT high		$t_{w(TIN/TOUTH)}$		2P+1		2P+1		
TIN/TOUT pins configured as outputs switching characteristics 15/ 24/ 25/									
T1	Delay time, CLKOUT high to TIN/TOUT high		$t_{d(COH-TIN/TOUTH)}$	See figure 23	-1	3	-1	3	ns
T2	Delay time, CLKOUT high to TIN/TOUT low		$t_{d(COH-TIN/TOUTL)}$		-1	3	-1	3	
T3	Pulse duration, TIN/TOUT (output)		$t_{w(TIN/TOUT)}$		P-1		P-1		

See footnote at end of table

TABLE I. Electrical performance characteristics – Continued. 1/

No	Test	Symbol	Test condition 2/	Limits				Unit
				CV_{DD}= 1.2 V CV_{DD} = 1.35 V		CV_{DD} = 1.6 V		
				Min	Max	Min	Max	
McBSP0 TIMINGS								
McBSP0 timing requirements 26/ See figure 24 and 25								
MC1	Cycle time, CLKR/X	$t_{c(CKRX)}$	CLKR/X ext	2P 15/		2P 15/		ns
MC2	Pulse duration, CLKR/X high or CLKR/X low	$t_{w(CKRX)}$	CLKR/X ext	P-1 15/		P-1 15/		
MC3	Rise time, CLKR/X	$t_{r(CKRX)}$	CLKR/X ext		6		6	
MC4	Fall time CLKR/X	$t_{f(CKRX)}$	CLKR/X ext		6		6	
MC5	Setup time, external FSR high before CLKR low	$t_{su(FRH-CKRL)}$	CLKR int	10		7		
			CLKR ext	2		2		
MC6	Hold time, external FSR high after CLKR low	$t_{h(CKRL-FRH)}$	CLKR int	-3		-3		
			CLKR ext	1		1		
MC7	Setup time, DR valid before CLKR low	$t_{su(DRV-CKRL)}$	CLKR int	10		7		
			CLKR ext	2		2		
MC8	Hold time, DR valid after CLKR low	$t_{h(CKRL-DRV)}$	CLKR int	-2		-2		
			CLKR ext	3		3		
MC9	Setup time, external FSX high before CLKX low	$t_{su(FXH-CKXL)}$	CLKR int	13		8		
			CLKR ext	3		2		
MC10	Hold time, external FSX high after CLKX low	$t_{h(CKXL-FXH)}$	CLKR int	-3		-3		
			CLKR ext	1		1		

See footnote at end of table

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test		Symbol	Test condition 2/	Limits				Unit
					CV_{DD}= 1.2 V CV_{DD} = 1.35 V		CV_{DD} = 1.6 V		
					Min	Max	Min	Max	
McBSP0 TIMINGS - Continued									
McPSP0 switching characteristics 15/ 26/ See figure 24 and 25									
MC1	Cycle time, CLKR/X		$t_{c(CKRX)}$	CLKR/X int	2P		2P		ns
MC3	Rise time, CLKR/X		$t_{r(CKRX)}$	CLKR/X int		1		1	
MC4	Fall time CLKR/X		$t_{f(CKRX)}$	CLKR/X int		1		1	
MC11	Pulse duration, CLKR/X high		$t_{w(CKRXH)}$	CLKR/X int	D-2 27/	D+2 27/	D-1 27/	D+1 27/	
MC12	Pulse duration, CLKR/X low		$t_{w(CKRXL)}$	CLKR/X int	C-2 27/	C+2 27/	C-1 27/	C+1 27/	
MC13	Delay time, CLKR high to internal FSR valid		$t_{d(CKRH-FRV)}$	CLKR int	-2	1	-2	1	
				CLKR ext	4	13	4	8	
MC14	Delay time, CLKR high to internal FSX valid		$t_{d(CKXH-FXV)}$	CLKR int	-2	2	-2	2	
				CLKR ext	4	15	4	9	
MC15	Disable time, DX high impedance from CLKX high following last data bit		$t_{dis(CKXH-DXHZ)}$	CLKR int	0	5	-5	1	
				CLKR ext	10	18	3	11	
MC16	Delay time, CLKX high to DX valid. This applies to all bits except the first bit transmitted.		$t_{d(CKXH-DXV)}$	CLKR int		5		4	
				CLKR ext		15	1	9	
	Delay time, CLKX high to DX valid 28/	DXENA = 0		CLKR int		4		2	
				CLKR ext		13		7	
	Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY = 01b or 10b) modes	DXENA = 1		CLKR int		2P+1		2P+1	
				CLKR ext		2P+4		2P+3	
MC17	Enable time, DX driven from CLKX high 28/	DXENA = 0	$t_{en(CKXH-DX)}$	CLKR int	-1		-3		
				CLKR ext	6		3		
	Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY = 01b or 10b) modes	DXENA = 1		CLKR int	P-1		P-3		
				CLKR ext	P+6		P+3		
MC18	Delay time, FSX high to DX valid 28/	DXENA = 0	$t_{d(FXH-DXV)}$	CLKR int		2		2	
				CLKR ext		13		8	
	Only applies to first bit transmitted when in Data Delay 0 (XDATDLY = 00b) mode	DXENA = 1		CLKR int		2P+1		2P+1	
				CLKR ext		2P+10		2P+10	
MC19	Enable time, DX driven from FSX high 28/	DXENA = 0	$t_{en(FXH-DX)}$	CLKR int	0		0		
				CLKR ext	8		3		
	Only applies to first bit transmitted when in Data Delay 0 (XDATDLY = 00b) mode	DXENA = 1		CLKR int	P-3		P-3		
				CLKR ext	P+8		P+4		

See footnote at end of table

TABLE I. Electrical performance characteristics – Continued. 1/

No	Test	Symbol	Test condition 2/	Limits				Unit
				CV_{DD}= 1.2 V CV_{DD} = 1.35 V		CV_{DD} = 1.6 V		
				Min	Max	Min	Max	
McBSP1 AND McBSP2 TIMINGS								
McBSP1 and McBSP2 timing requirements 26/ See figure 24 and 25								
MC1	Cycle time, CLKR/X	$t_{c(CKRX)}$	CLKR/X ext	2P 15/		2P 15/		ns
MC2	Pulse duration, CLKR/X high or CLKR/X low	$t_{w(CKRX)}$	CLKR/X ext	P-1 15/		P-1 15/		
MC3	Rise time, CLKR/X	$t_{r(CKRX)}$	CLKR/X ext		6		6	
MC4	Fall time CLKR/X	$t_{f(CKRX)}$	CLKR/X ext		6		6	
MC5	Setup time, external FSR high before CLKR low	$t_{su(FRH-CKRL)}$	CLKR int	11		7		
			CLKR ext	3		3		
MC6	Hold time, external FSR high after CLKR low	$t_{h(CKRL-FRH)}$	CLKR int	-3		-3		
			CLKR ext	1		1		
MC7	Setup time, DR valid before CLKR low	$t_{su(DRV-CKRL)}$	CLKR int	11		7		
			CLKR ext	3		3		
MC8	Hold time, DR valid after CLKR low	$t_{h(CKRL-DRV)}$	CLKR int	-2		-2		
			CLKR ext	3		3		
MC9	Setup time, external FSX high before CLKX low	$t_{su(FXH-CKXL)}$	CLKR int	14		9		
			CLKR ext	4		3		
MC10	Hold time, external FSX high after CLKX low	$t_{h(CKXL-FXH)}$	CLKR int	-3		-3		
			CLKR ext	1		1		

See footnote at end of table

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test		Symbol	Test condition 2/	Limits				Unit
					CV_{DD}= 1.2 V CV_{DD} = 1.35 V		CV_{DD} = 1.6 V		
					Min	Max	Min	Max	
McBSP1 AND McBSP2 TIMINGS - Continued									
McPSP1 and McBSP2 switching characteristics 15/ 26/ See figure 24 and 25									
MC1	Cycle time, CLKR/X		$t_{c(CKRX)}$	CLKR/X int	2P		2P		ns
MC3	Rise time, CLKR/X		$t_{r(CKRX)}$	CLKR/X int		2		2	
MC4	Fall time CLKR/X		$t_{f(CKRX)}$	CLKR/X int		2		2	
MC11	Pulse duration, CLKR/X high		$t_{w(CKRXH)}$	CLKR/X int	D-2 27/	D+2 27/	D-2 27/	D+2 27/	
MC12	Pulse duration, CLKR/X low		$t_{w(CKRXL)}$	CLKR/X int	C-2 27/	C+2 27/	C-2 27/	C+2 27/	
MC13	Delay time, CLKR high to internal FSR valid		$t_{d(CKRH-FRV)}$	CLKR int	-3	2	-3	2	
				CLKR ext	3	14	3	9	
MC14	Delay time, CLKR high to internal FSX valid		$t_{d(CKXH-FXV)}$	CLKR int	-3	2	-3	2	
				CLKR ext	4	15	4	9	
MC15	Disable time, DX high impedance from CLKX high following last data bit		$t_{dis(CKXH-DXHZ)}$	CLKR int	-3	3	-5	1	
				CLKR ext	10	19	3	12	
MC16	Delay time, CLKX high to DX valid. This applies to all bits except the first bit transmitted.		$t_{d(CKXH-DXV)}$	CLKR int		5		3	
				CLKR ext		15		9	
	Delay time, CLKX high to DX valid 28/	DXENA = 0		CLKR int		4		2	
				CLKR ext		15		9	
	Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY = 01b or 10b) modes	DXENA = 1		CLKR int		2P+1		2P+1	
				CLKR ext		2P+5		2P+3	
MC17	Enable time, DX driven from CLKX high 28/	DXENA = 0	$t_{en(CKXH-DX)}$	CLKR int	-2		-4		
				CLKR ext	9		4		
	Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY = 01b or 10b) modes	DXENA = 1		CLKR int	P-2		P-4		
				CLKR ext	P+9		P+4		
MC18	Delay time, FSX high to DX valid 28/	DXENA = 0	$t_{d(FXH-DXV)}$	CLKR int		3		2	
				CLKR ext		13		8	
	Only applies to first bit transmitted when in Data Delay 0 (XDATDLY = 00b) mode	DXENA = 1		CLKR int		2P+1		2P+1	
				CLKR ext		2P+12		2P+7	
MC19	Enable time, DX driven from FSX high 28/	DXENA = 0	$t_{en(FXH-DX)}$	CLKR int	1		0		
				CLKR ext	8		4		
	Only applies to first bit transmitted when in Data Delay 0 (XDATDLY = 00b) mode	DXENA = 1		CLKR int	P-1		P-3		
				CLKR ext	P+8		P+5		

See footnote at end of table

TABLE I. Electrical performance characteristics – Continued. 1/

No	Test	Symbol	Test condition 2/	Limits								Unit
				CV_{DD}= 1.2 V CV_{DD} = 1.35 V				CV_{DD} = 1.6 V				
				Master		Slave		Master		Slave		
				Min	Max	Min	Max	Min	Max	Min	Max	
McBSP AS SPI MASTER OR SLAVE TIMINGS												
McBSP as SPI Master or Slave timing requirements (CLKSTP = 10b, CLKXP = 0) 15/ 29/ See figure 26-29												
MC23	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXL)}$		15		3-6P		10		3-6P		ns
MC24	Hold time, DR valid after CLKX high	$t_{h(CKXL-DRV)}$		0		3+6P		0		3+6P		
MC25	Setup time, FSX low before CLKX low	$t_{su(FXL-CKXH)}$				5				5		
MC26	Cycle time, CLKX	$t_{c(CKX)}$		2P		16P		2P		16P		
McBSP as SPI Master or Slave switching characteristics (CLKSTP = 10b, CLKXP =0) 15/ 29/ See figure 26-29												
MC27	Delay time, CLKX low to FSX low 31/	$t_{d(CKXL-FXL)}$		T-5	T+5			T-5	T+5			ns
MC28	Delay time, FSX low to CLKX high 32/	$t_{d(FXL-CKXH)}$		C-5	C+5			C-5	C+5			
MC29	Delay time, CLKX high to DX valid	$t_{d(CKXH-DXV)}$		-4	6	3P+3	5P+15	-3	3	3P+3	5P+8	
MC30	Disable time, DX high impedance following last data bit from CLKX low	$t_{dis(CKXL-DXHZ)}$		C-4	C+4			C-3	C+1			
MC31	Disable time, DX high impedance following last data bit from FSX high	$t_{dis(FXH-DXHZ)}$				3P+4	3P+19			3P+3	3P+11	
MC32	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$				3P+4	3P+18			3P+4	3P+10	
McBSP as SPI Master or Slave timing requirements (CLKSTP = 11b, CLKXP = 0) 15/ 29/ See figure 26-29												
MC33	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$		15		3-6P		10		3-6P		ns
MC34	Hold time, DR valid after CLKX high	$t_{h(cKXH-DRV)}$		0		3+6P		0		3+6P		
MC25	Setup time, FSX low before CLKX high	$t_{su(FXL-CKXH)}$				5				5		
MC26	Cycle time, CLKX	$t_{c(CKX)}$		2P		16P		2P		16P		
McBSP as SPI Master or Slave switching characteristics (CLKSTP = 11b, CLKXP =0) 15/ 29/ See figure 26-29												
MC27	Delay time, CLKX low to FSX low 31/	$t_{d(CKXL-FXL)}$		C-5	C+5			C-4	C+4			ns
MC28	Delay time, FSX low to CLKX high 32/	$t_{d(FXL-CKXH)}$		T-5	T+5			T-4	T+4			
MC35	Delay time, CLKX high to DX valid	$t_{d(CKXL-DXV)}$		-4	6	3P+3	5P+15	-3	3	3P+3	5P+8	
MC30	Disable time, DX high impedance following last data bit from CLKX low	$t_{dis(CKXL-DXHZ)}$		-4	4	3P+4	3P+19	-3	1	3P+3	3P+12	
MC32	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$		D-4	D+4	3P+4	3P+18	D-3	D+3	3P+4	3P+10	

See footnote at end of table

TABLE I. Electrical performance characteristics – Continued. 1/

No	Test	Symbol	Test condition 2/	Limits								Unit
				CV_{DD}= 1.2 V CV_{DD} = 1.35 V				CV_{DD} = 1.6 V				
				Master		Slave		Master		Slave		
				Min	Max	Min	Max	Min	Max	Min	Max	
McBSP AS SPI MASTER OR SLAVE TIMINGS - Continued												
McBSP as SPI Master or Slave timing requirements (CLKSTP = 10b, CLKXP = 1) 15/ 29/ See figure 26-29												
MC33	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$		15		3-6P		10		3-6P		ns
MC34	Hold time, DR valid after CLKX high	$t_{h(CKXH-DRV)}$		0		3+6P		0		3+6P		
MC35	Setup time, FSX low before CLKX low	$t_{su(FXL-CKXL)}$				5				5		
MC26	Cycle time, CLKX	$t_{c(CKX)}$		2P		16P		2P		16P		
McBSP as SPI Master or Slave switching characteristics (CLKSTP = 10b, CLKXP =1) 15/ 29/ See figure 26-29												
MC37	Delay time, CLKX high to FSX low 31/	$t_{d(CKXH-FXL)}$		T-5	T+5			T-4	T+4			ns
MC38	Delay time, FSX low to CLKX low 32/	$t_{d(FXL-CKXL)}$		D-5	D+5			D-4	D+4			
MC39	Delay time, CLKX low to DX valid	$t_{d(CKXL-DXV)}$		-4	6	3P+3	5P+15	-3	3	3P+3	5P+8	
MC30	Disable time, DX high impedance following last data bit from CLKX high	$t_{dis(CKXH-DXHZ)}$		D-4	D+4			D-3	D+1			
MC31	Disable time, DX high impedance following last data bit from FSX high	$t_{dis(FXH-DXHZ)}$				3P+4	3P+19			3P+3	3P+11	
MC32	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$				3P+4	3P+18			3P+4	3P+10	
McBSP as SPI Master or Slave timing requirements (CLKSTP = 11b, CLKXP = 1) 15/ 29/ See figure 26-29												
MC23	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXL)}$		15		3-6P		10		3-6P		ns
MC24	Hold time, DR valid after CLKX high	$t_{h(CKXL-DRV)}$		0		3+6P		0		3+6P		
MC36	Setup time, FSX low before CLKX high	$t_{su(FXL-CKXL)}$				5				5		
MC26	Cycle time, CLKX	$t_{c(CKX)}$		2P		16P		2P		16P		
McBSP as SPI Master or Slave switching characteristics (CLKSTP = 11b, CLKXP =1) 15/ 29/ See figure 26-29												
MC37	Delay time, CLKX low to FSX low 31/	$t_{d(CKXL-FXL)}$		D-5	D+5			D-4	D+4			ns
MC38	Delay time, FSX low to CLKX high 32/	$t_{d(FXL-CKXH)}$		T-5	T+5			T-4	T+4			
MC29	Delay time, CLKX high to DX valid	$t_{d(CKXH-DXV)}$		-4	6	3P+3	5P+15	-3	3	3P+3	5P+8	
MC39	Disable time, DX high impedance following last data bit from CLKX low	$t_{dis(CKXL-DXHZ)}$		-4	4	3P+4	3P+19	-3	1	3P+3	3P+12	
MC32	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$		C-4	C+4	3P+4	3P+18	C-3	C+3	3P+4	3P+10	

See footnote at end of table

TABLE I. Electrical performance characteristics – Continued. 1/

No	Test	Symbol	Test condition 2/	Limits				Unit
				CV_{DD}= 1.2 V CV_{DD} = 1.35 V		CV_{DD} = 1.6 V		
				Min	Max	Min	Max	
McBSP GENERAL PURPOSE I/O TIMINGS								
McBSP general purpose I/O timing requirements See figure 30								
MC20	Setup time, MGPIOx input mode before CLKOUT high 33/	$t_{su(MGPIO-COH)}$		7		7		ns
MC21	Hold time, MGPIOx input mode after CLKOUT high 33/	$t_{h(COH-MGPIO)}$		0		0		
ENHANCED HOST PORT INTERFACE (EHPI) TIMINGS								
EHPI timing requirements See figure 31-36								
E11	Setup time, $\overline{HAS}$ low before $\overline{HDS}$ low	$t_{su(HASL-HDSL)}$		4		4		ns
E12	Hold time, $\overline{HAS}$ low after $\overline{HDS}$ low	$t_{h(HDSL-HASL)}$		3		3		
E13	Setup time, (HR/$\overline{W}$, HA[13:0], $\overline{HBE[1:0]}$, HCNTL[1:0]) valid before $\overline{HDS}$ low	$t_{su(HCNTLV-HDSL)}$		2		2		
E14	Hold time, (HR/$\overline{W}$, HA[13:0], $\overline{HBE[1:0]}$, HCNTL[1:0]) invalid after $\overline{HDS}$ low	$t_{h(HDSL-HCTNLIV)}$		4		4		
E15	Pulse duration, $\overline{HDS}$ low	$t_{w(HDSL)}$		4P 15/		4P 15/		
E16	Pulse duration, $\overline{HDS}$ high	$t_{w(HDSH)}$		4P 15/		4P 15/		
E17	Setup time, HD bus write data valid before $\overline{HDS}$ high	$t_{su(HDV-HDSH)}$		3		3		
E18	Hold time, HD bus write data invalid after $\overline{HDS}$ high	$t_{h(HDSH-HDIV)}$		4		4		
E19	Setup time, (HR/$\overline{W}$, $\overline{HBE}$ $\overline{[1:0]}$, HCTNL[1:0]) valid before $\overline{HAS}$ low	$t_{su(HCTNLV-HASL)}$		3		3		
E20	Hold time, (HR/$\overline{W}$, $\overline{HBE}$ $\overline{[1:0]}$, HCTNL[1:0]) valid before $\overline{HAS}$ low	$t_{h(HASL-HCTNLIV)}$		4		4		
EHPI switching characteristics See figure 31-36								
E1	Enable time, HDS low to HD bus enable (memory access)	$t_{en(HDSL-HDD)M}$		6	26	6	19	ns
E2	Delay time, HDS low to HD bus read data valid (memory access)	$t_{d(HDSL-HDV)M}$		14P 15/ 35/		14P 15/ 35/		
E4	Enable time, HDS low to HD enabled (register access)	$t_{en(HDSL-HDD)R}$		6	26	6	19	
E5	Delay time, HDS low to HD bus read data valid (register access)	$t_{d(HDSL-HDV)R}$			26		19	
E6	Disable time, HDS high to HD bus read data invalid	$t_{dis(HDSH-HDIV)}$		6	26	6	19	
E7	Delay time, HDS low to HRDY low (during reads)	$t_{d(HDSL-HRDYL)}$			18		15	
E8	Delay time, HD bus valid to HRDY high (during reads)	$t_{d(HDV-HRDYH)}$		2		2		
E9	Delay time, HDS high to HRDY low (during writes)	$t_{d(HDSH-HRDYL)}$			18		15	
E10	Delay time, HDS high to HRDY high (during writes)	$t_{d(HDSH-HRDYH)}$		14P 15/ 35/		14P 15/ 35/		
E21	Delay time, CLKOUT high to HINT high/low	$t_{d(COH-HINT)}$		0	11	0	8	

See footnote at end of table

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/	Limits								Unit
				CV_{DD}= 1.2 V CV_{DD} = 1.35 V				CV_{DD} = 1.6 V				
				Standard Mode		Fast Mode		Standard Mode		Fast Mode		
				Min	Max	Min	Max	Min	Max	Min	Max	
I^2C TIMINGS												
I^2C signals (SDA and SCL) timing requirements See figure 37-38												
IC1	Cycle time, SCL	$t_{c(SCL)}$		10		2.5		10		2.5		µs
IC2	Setup time, SCL high before SDA low for a repeated START condition	$t_{su(SCLH-SDAL)}$		4.7		0.6		4.7		0.6		
IC3	Hold time, SCL low after SDA low for a START and a repeated START condition	$t_{h(SCLL-SDAL)}$		4		0.6		4		0.6		
IC4	Pulse duration, SCL low	$t_{w(SCLL)}$		4.7		1.3		4.7		1.3		
IC5	Pulse duration, SCL high	$t_{w(SCLH)}$		4		0.6		4		0.6		
IC6	Setup time, SDA valid before SCL high	$t_{su(SDA-SCLH)}$		250		100 36/		250		100 36/		ns
IC7	Hold time, SDA valid after SCL low	$t_{h(SDA-SCLL)}$		0 37/		0 37/	0.9 38/	0 37/		0 37/	0.9 38/	µs
IC8	Pulse duration, SDA high between STOP and START conditions	$t_{w(SDAH)}$		4.7		1.3		4.7		1.3		
IC9	Rise time, SDA	$t_{r(SDA)}$			1000	39/ 40/	300		1000	39/ 40/	300	ns
IC10	Rise time, SCL	$t_{r(SCL)}$			1000	39/ 40/	300		1000	39/ 40/	300	
IC11	Fall time, SDA	$t_{f(SDA)}$			300	39/ 40/	300		300	39/ 40/	300	
IC12	Fall time, SCL	$t_{f(SCL)}$			300	39/ 40/	300		300	39/ 40/	300	
IC13	Setup time, SCL high before SDA high (for STOP condition)	$t_{su(SCLH-SDAH)}$		4		0.6		4		0.6		µs
IC14	Pulse duration, spike (must be suppressed)	$t_{w(SP)}$				0	50			0	50	ns
IC15	Capacitive load for each bus line	C_b 40/			400		400		400		400	pF

See footnote at end of table

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/	Limits								Unit
				CV_{DD}= 1.2 V CV_{DD} = 1.35 V				CV_{DD} = 1.6 V				
				Standard Mode		Fast Mode		Standard Mode		Fast Mode		
				Min	Max	Min	Max	Min	Max	Min	Max	
			I^2C TIMINGS									
I^2C signals (SDA and SCL) timing requirements- Continued See figure 37-38												
IC16	Cycle time, SCL	$t_{c(SCL)}$		10		2.5		10		2.5		µs
IC17	Delay time, SCL high before SDA low for a repeated START condition	$t_{d(SCLH-SDAL)}$		4.7		0.6		4.7		0.6		
IC18	Delay time, SDA low to SCL low for a START and a repeated START condition	$t_{h(SDAL-CLLL)}$		4		0.6		4		0.6		
IC19	Pulse duration, SCL low	$t_{w(SCLL)}$		4.7		1.3		4.7		1.3		
IC20	Pulse duration, SCL high	$t_{w(SCLH)}$		4		0.6		4		0.6		
IC21	Delay time, SDA valid to SCL high	$t_{d(SDA-SCLH)}$		250		100		250		100		ns
IC22	Valid time, SDA valid after SCL low	$t_{h(SCLL-=SDAV)}$		0		0	0.9	0		0	0.9	µs
IC23	Pulse duration, SDA high between STOP and START conditions	$t_{w(SDAH)}$		4.7		1.3		4.7		1.3		
IC24	Rise time, SDA	$t_{r(SDA)}$			1000	39/ 40/	300		1000	39/ 40/	300	ns
IC25	Rise time, SCL	$t_{r(SCL)}$			1000	39/ 40/	300		1000	39/ 40/	300	
IC26	Fall time, SDA	$t_{f(SDA)}$			300	39/ 40/	300		300	39/ 40/	300	
IC27	Fall time, SCL	$t_{f(SCL)}$			300	39/ 40/	300		300	39/ 40/	300	
IC28	Delay time, SCL high before SDA high (for STOP condition)	$t_{d(SCLH-SDAH)}$		4		0.6		4		0.6		µs
IC29	Capacitive load for each bus line	C_b 40/			400		400		400		400	pF

See footnote at end of table

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/	Limits				Unit
				CV_{DD}= 1.2 V CV_{DD} = 1.35 V		CV_{DD} = 1.6 V		
				Full speed 12Mbps		Full speed 12Mbps		
				Min	Max	Min	Max	
	UNIVERSAL SERIAL BUS (USB) TIMINGS							
Universal serial bus (ISB) characteristics	See figure 39 and 40							
U1	Rise time of DP and DN signal 41/	t_r		4	20	4	20	ns
U2	Fall time of DP and DN signal 41/	t_f		4	20	4	20	
	Rise/Fall time matching 42/	t_{RFM}		90	111.11	90	111.11	%
	Output signal cross over voltage 41/	V_{CRS}		1.3	2	1.3	2	V
	Differential propagation jitter 43/ 44/	t_{jr}		-2	2	-2	2	ns
	Operating frequency (full speed mode)	f_{op}		12 TYP		12 TYP		Mb/s
U3	Series resistor	$R_{s(DP)}$		24 TYP		24 TYP		W
U4	Series resistor	$R_{s(DN)}$		24 TYP		24 TYP		W
U5	Edge rate control capacitor	$C_{edge(DP)}$		22 TYP		22 TYP		pF
U6	Edge rate control capacitor	$C_{edge(DN)}$		22 TYP		22 TYP		
	ADC TIMINGS							
ADC characteristics								
A1	Cycle time, ADC internal conversion clock	$t_{c(SCLC)}$		500		500		ns
A2	Delay time, ADC sample and hold acquisition time	$t_{d(AQ)}$			40		40	µs
A3	Delay time, ADC conversion time	$t_{d(CONV)}$			45/		45/	ns
A4	Static differential non-linearity error	S_{DNL}			2		2	LSB
	Static integral non-linearity error				3		3	
A5	Zero scale offset error	Z_{set}			9		9	LSB
A6	Full scale offset error	F_{set}			9		9	LSB
A7	Analog input impendance			1		1		MW

See footnote at end of table

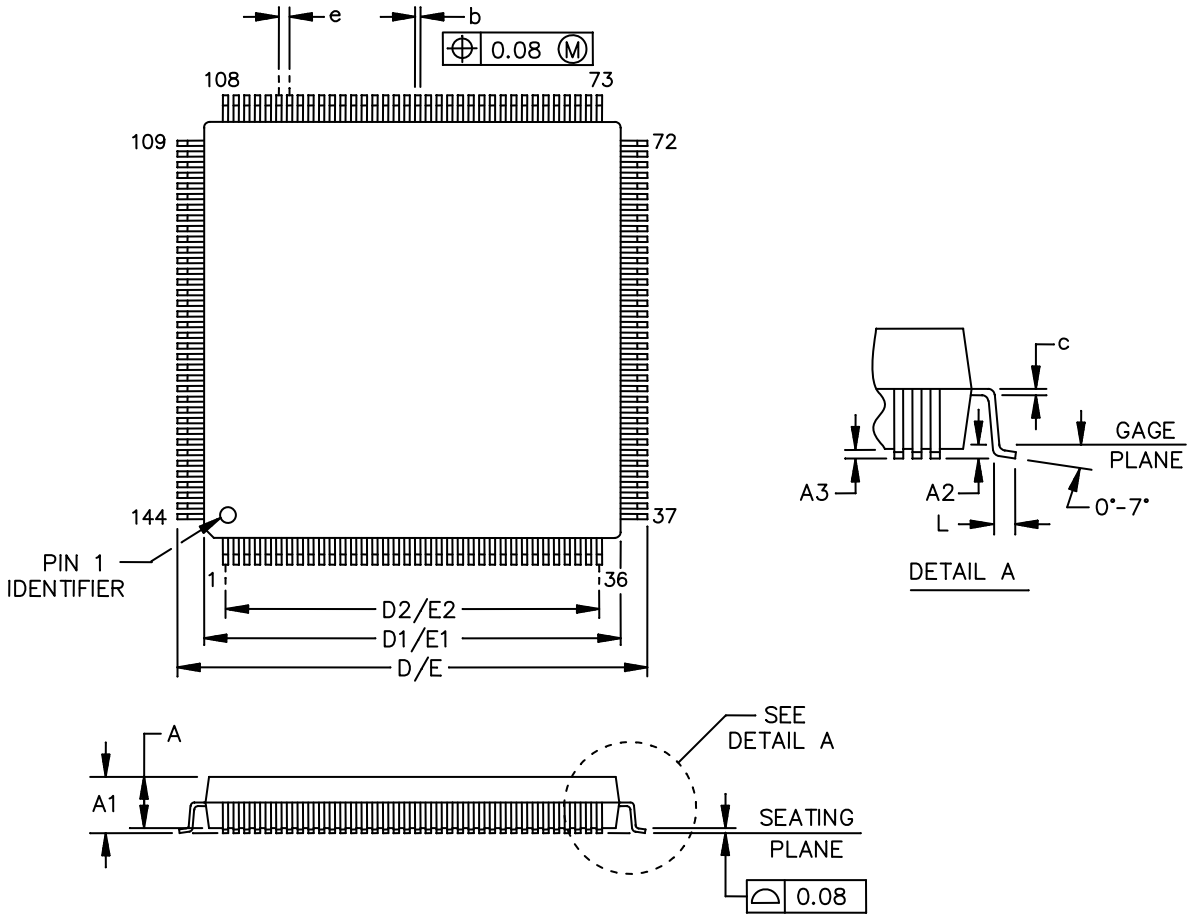
TABLE I. Electrical performance characteristics - Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ Over recommended operating case temperature range; unless otherwise noted.
3/ USB I/O pins DP and DN can tolerate a short circuit at D+ and D- to 0 V or 5 V, as long as the recommended series resistors (see Figure 40) are connected between the D+ and DP (package), and the D- and DN (package. Do not apply a short circuit to the USB I/O pins DP and DN in absence of the series resistors.
4/ The I^2C pins SDA and SCL do not feature fail-safe I/O buffers, These pins could potentially draw current when the device is powered down.
5/ CPU executing 75% dual MAC + 25% ADD with moderate data bus activity (table of sine values). CPU and CLKGEN (DPLL) domain are active. All other domain are idled.
6/ One world of a table of a 16-bit sine value is writtern to the EMIF every 250 ns (64 Mbps). Each EMIF output pin is connected to a 10 pF load.
7/ In CLKGEN domain idle mode, X2/CLKIN becomes output and is driven low to stop external crystals (if used) from oscillating. Standby current will be higher if an external clock source tries to drive the X2/CLKIN pin during this time.
8/ This device utilizes a fully static design and therefore can operate with $t_{c(Cl)}$ approaching ∞. If an external crystal is used, the X2/CLKIN cycle time is limited by the crystal frequency range listed in manufacturer data.
9/ It is recommended that the DPLL synthesized clocking option be used to obtain maximum operating frequency.
10/ N = Clock frequency synthesis factor.
11/ ESR must be 200 kΩ or greater at frequency other than 32.768 kHz. Otherwise, oscillations at overtone frequency may occur.
12/ To ensure data setup time, simply program the strobe width wide enough. ARDY is internally synchronized. If ARDY does meet setup or hold time, it may be recognized in the current cycle or the next cycle. Thus ARDY can be asynchronous input.
13/ Maximum SDRAM operating frequency = 108 MHz. Actual attainable maximum operating frequency will depend on the quality of the PC board design and the memory chip timing requirement.
14/ Maximum SDRAM operating frequency = 133 MHz. Actual attainable maximum operating frequency will depend on the quality of the PC board design and the memory chip timing requirement.
15/ P = 1/(input clock frequency) in ns. For example, when running parts at 12 MHz, P = 83.33 ns.
16/ Oscillator stable time depends on the crystal characteristics (i.e., frequency, ESR, etc.) which varies from one crystal manufacturer to another. Based on the crystal characteristics, the oscillator stable time can be in the range of a few to 10 s of ms. A reset circuit with 100 ms or more dealy time will ensure the oscillator before the $\overline{\text{RESET}}$ goes high.
17/ BK group: Pins with bus keepers, hold previous state during reset. Following low-to-high transition of $\overline{\text{RESET}}$, these pins go to their post reset logic state.
BK group pins: A'[0], A[15:0], D[15:0], C[14:2], c0, GPIO5, DX1, and DX2.
18/ High group: Following low to high transition of $\overline{\text{RESET}}$, these pins go to logic high state.
High group pins: C1[HPI.$\overline{\text{HINT}}$], XF
19/ Z group: Bidirectional pins which became input or output pins. Following low to high transition of $\overline{\text{RESET}}$, these pins go to high impedance state.
Z group pins: C1[EMIF.AOE], GPIO[7:6, 4:0], TIN/TOUT0, SDA, SCL, CLKR0, FSR0, CLKX0, DX0, FSX0, FSX2, CLKX2, FSR2, DR2, CLKR2, FSX1, CLKX1, FSR1, DR1, CLKR1, A[20:16].
20/ Estimated data based on 12 MHz crystal used with on-chip oscillator at 25°C. This number will vary based on the actual crystal characteristics operating condition and the PC board layout and the parasitic.
21/ Following the clock generation domain idle, the $\overline{\text{INTx}}$ becomes level sensitive and stay that way until the low to high transaction of $\overline{\text{INTx}}$ following the CPU wake up. Holding the $\overline{\text{INTx}}$ low longer than minimum requirement will send more than one interrupt to the CPU. The number of interrupts sent to the CPU depends on the $\overline{\text{INTx}}$ low time following the CPU wake up from IDLE.
22/ AGPIO pins: A[15:0]
23/ EHPIGPIO pins: C13, C10, C7, C5, C4 , and C0

TABLE I. Electrical performance characteristics - Continued. 1/

24/ Only the Timer0 signal is externally available. The Timer1 signal is internally terminated and is not available for external use.
25/ For proper operation of the TIN/TOUT pin configured as an output, the timer period must be configured for at least 4 cycles.
26/ Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any signals is inverted, then the timing references of that signal are also inverted.
27/ T = CLKRX period = (1 + CLKGDV) * P
C = CLKRX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * P when CLKGDV is even
D = CLKRX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * P when CLKGDV is even.
28/ See manufacturer data for a description of the DX enable (DXENA) and data delay features of the McBSP.
29/ For all SPI slave modes, CLKG is programmed as ½ of the CPU clock by setting CLKSM = CLKGDV = 1.
30/ T = CLKRX period = (1 + CLKGDV) * 2P
C = CLKRX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * 2P when CLKGDV is even
31/ FSRP = FSXP = 1. As a SPI master, BFSX is inverted to provide active low slave enable output. As a slave, the active low signal input on BFSX and BFSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP.
32/ FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).
33/ MGPIOx refers to CLKRx, FSRx, DRx, CLKXx, or FSXx when configured as a general purpose input.
34/ MGPIOx refers to CLKRx, FSRx, DRx, CLKXx, or FSXx when configured as a general purpose output.
35/ EHPI latency is dependent on the number of DMA channels active, their priorities and their source/destination ports. The latency shown assumes no competing CPU or DMA activity to the memory resource being accessed by the EHPI.
36/ A fast mode I^2C bus device can be used in a Standard mode I^2C bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + $t_{su(SDA-ASCLH)}$ = 1000 + 250 = 1250 ns (according to the Standard mode I2C Bus specification) before the SCL line is released.
37/ A device must internally provide a hold time for at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
38/ The maximum $t_{h(SDA-SCLL)}$ has only to bet met if the device does not stretch the LOW period [$t_{w(SCLL)}$] of the SCL signal.
39/ $20 + 0.1C_b$
40/ C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall times are allowed.
41/ C_L = 50 pF
42/ $(t_r/t_f) \times 100$
43/ $t_{px(1)} \times t_{px(0)}$
44/ USB PLL is susceptible to power supply ripple, refer to recommended operating conditions for allowable supply ripple to meet the USB pea to peak jitter specification.
45/ $13*t_{c(SCLC)}$

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	1.35	1.45	D/E	21.80	22.20
A1		1.60	D1/E1	19.80	20.20
A2	0.25 TYP		D2/E2	17.50 TYP	
A3	0.05		e	0.50 BSC	
b	0.17	0.27	L	0.45	0.75
c	0.13 NOM				

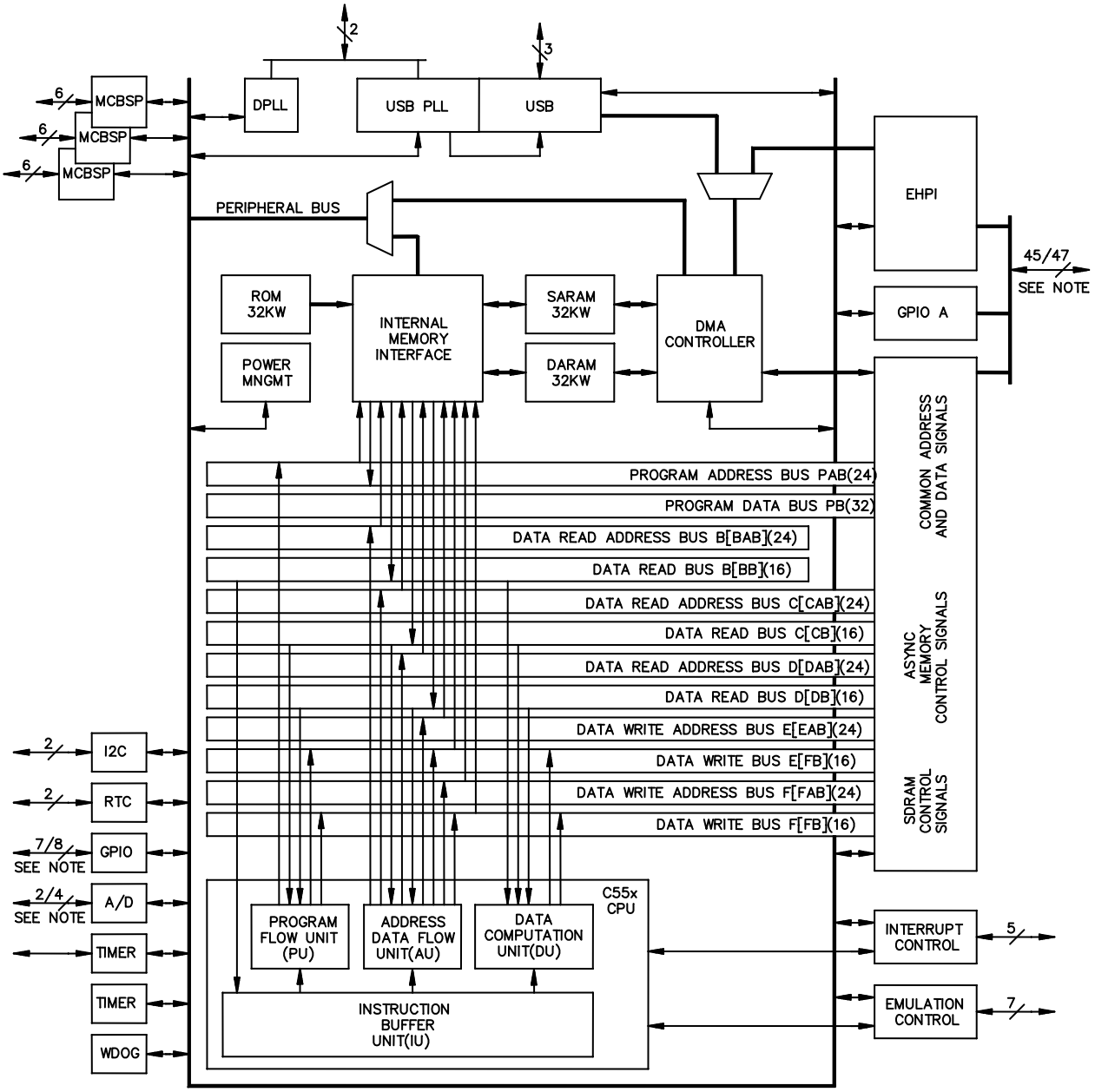
NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.

FIGURE 1. Case outlines.

Case X

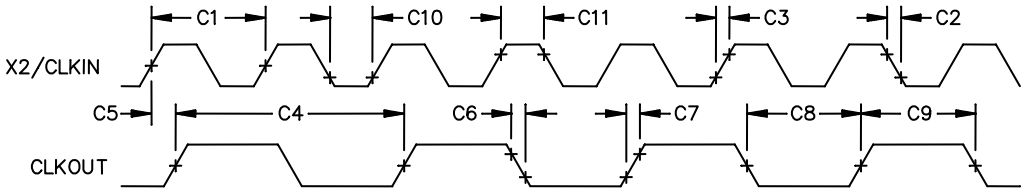
Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	V_{SS}	37	V_{SS}	73	V_{SS}	109	RDV_{DD}
2	PU	38	A13	74	D12	110	RCV_{DD}
3	DP	39	A12	75	D13	111	RTCINX2
4	DN	40	A11	76	D14	112	RTCINX1
5	$USBV_{DD}$	41	CV_{DD}	77	D15	113	V_{SS}
6	GPIO7	42	A10	78	CV_{DD}	114	V_{SS}
7	V_{SS}	43	A9	79	EMU0	115	V_{SS}
8	DV_{DD}	44	A8	80	EMU1/$\overline{OFF}$	116	DX2
9	GPIO2	45	V_{SS}	81	TDO	117	FSX2
10	GPIO1	46	A7	82	TDI	118	CV_{DD}
11	V_{SS}	47	A6	83	CV_{DD}	119	CLKX2
12	GPIO0	48	A5	84	$\overline{TRST}$	120	DR2
13	X2/CLKIN	49	DV_{DD}	85	TCK	121	FSR2
14	X1	50	A4	86	TMS	122	V_{SS}
15	CLKOUT	51	A3	87	CV_{DD}	123	CLKR2
16	C0	52	A2	88	DV_{DD}	124	DX1
17	C1	53	CV_{DD}	89	SDA	125	FSX1
18	CV_{DD}	54	A1	90	SCL	126	DV_{DD}
19	C2	55	A0	91	$\overline{RESET}$	127	CLKX1
20	C3	56	DV_{DD}	92	$USBPLLV_{SS}$	128	DR1
21	C4	57	D0	93	$\overline{INT0}$	129	FSR1
22	C5	58	D1	94	$\overline{INT1}$	130	CLKR1
23	C6	59	D2	95	$USBPLLV_{DD}$	131	DX09
24	DV_{DD}	60	V_{SS}	96	$\overline{INT2}$	132	CV_{DD}
25	C7	61	D3	97	$\overline{INT3}$	133	FSX0
26	C8	62	D4	98	DV_{DD}	134	CLKX0
27	C9	63	D5	99	$\overline{INT4}$	135	DR0
28	C11	64	V_{SS}	100	V_{SS}	136	FSR0
29	CV_{DD}	65	D6	101	XF	137	CLKR0
30	CV_{DD}	66	D7	102	V_{SS}	138	V_{SS}
31	C14	67	D8	103	ADV_{SS}	139	DV_{DD}
32	C12	68	CV_{DD}	104	ADV_{DD}	140	TIN/TOUT0
33	V_{SS}	69	D9	105	AIN0	141	GPIO6
34	C10	70	D10	106	AIN1	142	GPIO4
35	C13	71	D11	107	AV_{DD}	143	GPIO3
36	V_{SS}	72	DV_{DD}	108	AV_{SS}	144	V_{SS}

FIGURE 2. Terminal connections.



NOTE:
1. Number of pins determined by package type.

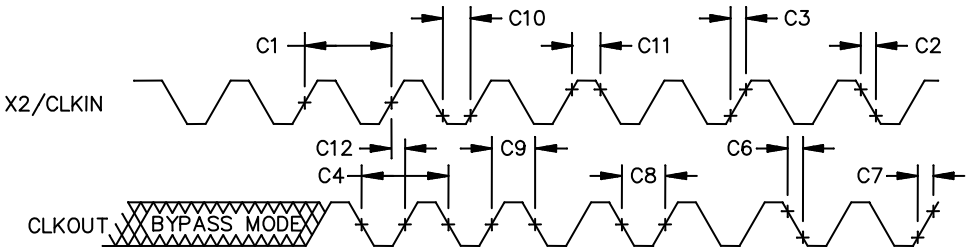
FIGURE 3. Functional block diagram.



BYPASS MODE CLOCK TIMING

NOTE:
1. The relationship of X2/CLKIN to CLKOUT depends on the PLL bypass divide factor chosen for the CLKMD register. The waveform relationship shown in this figure is intended to illustrate the timing parameters based on CLKOUT = ½(CLKIN) configuration.

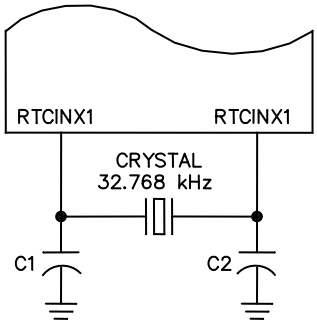
FIGURE 4. Timing waveforms.



EXTERNAL MULTIPLY-BY-N CLOCK TIMINGS

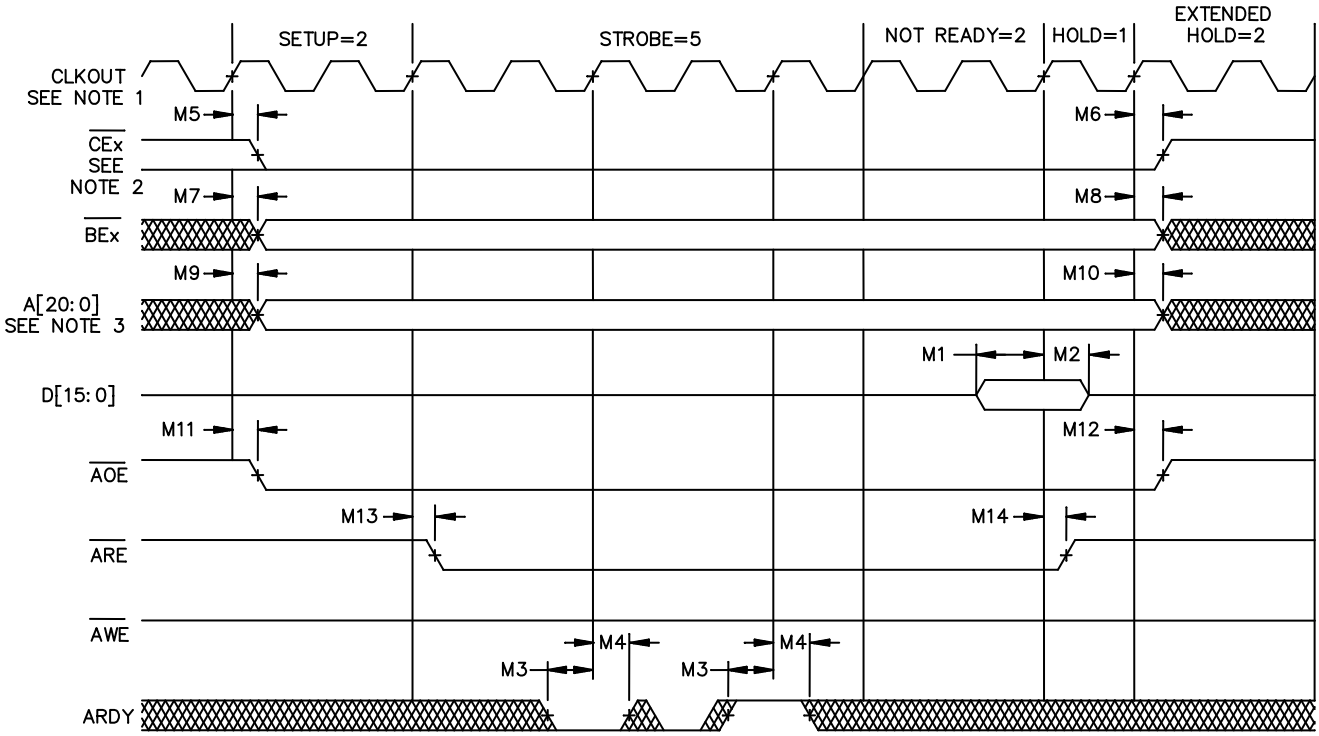
NOTE:
1. The relationship of X2/CLKIN to CLKOUT depends on the PLL multiply and divide factor chosen for the CLKMD register. The waveform relationship shown in this figure is intended to illustrate the timing parameters based on CLKOUT = 1xCLKIN configuration.

FIGURE 5. Timing waveforms.



REAL-TIME CLOCK OSCILLATOR WITH EXTERNAL CRYSTAL

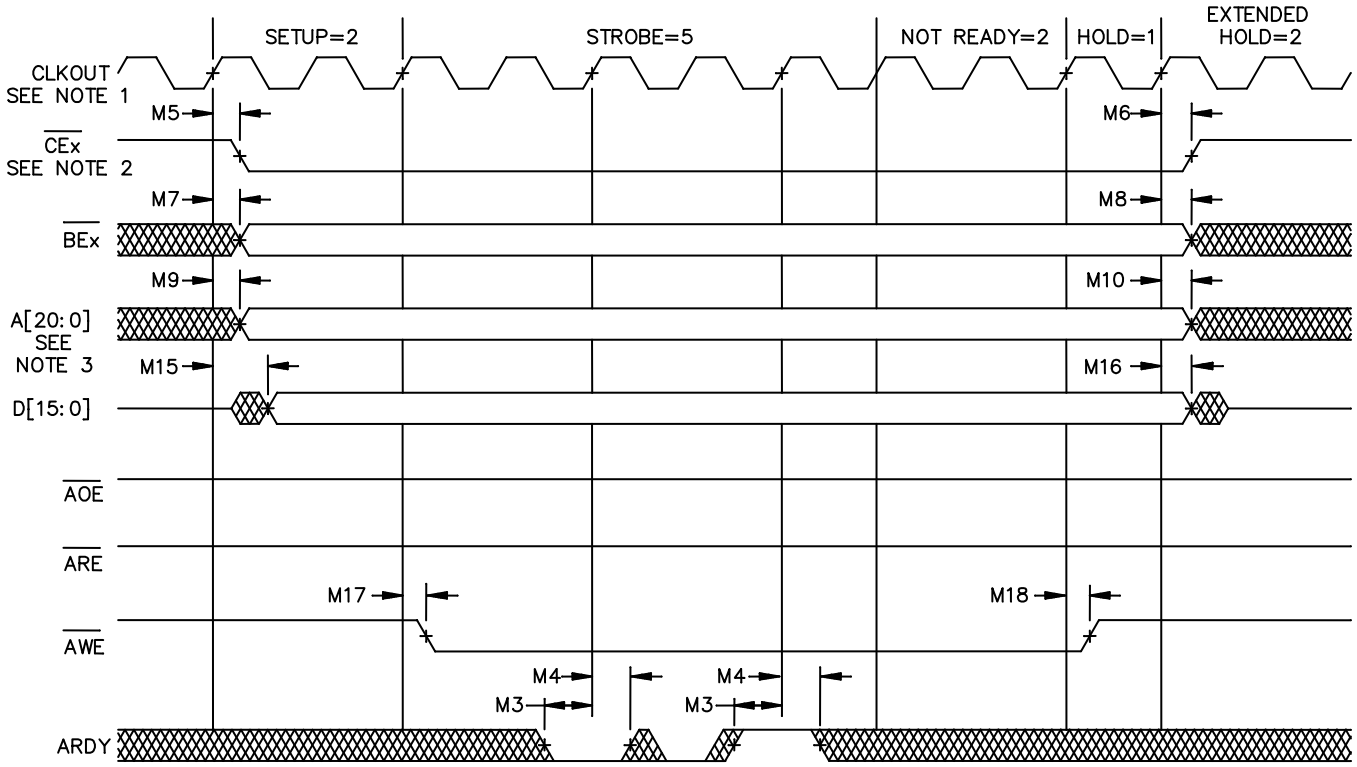
FIGURE 6. Timing waveforms.



ASYNCHRONOUS MEMORY READ TIMINGS

NOTES:
1. CLKOUT is equal to CPU clock.
2. $\overline{\text{CEx}}$ becomes active depending on the memory address space being accessed.
3. A[13:0] for LQFP

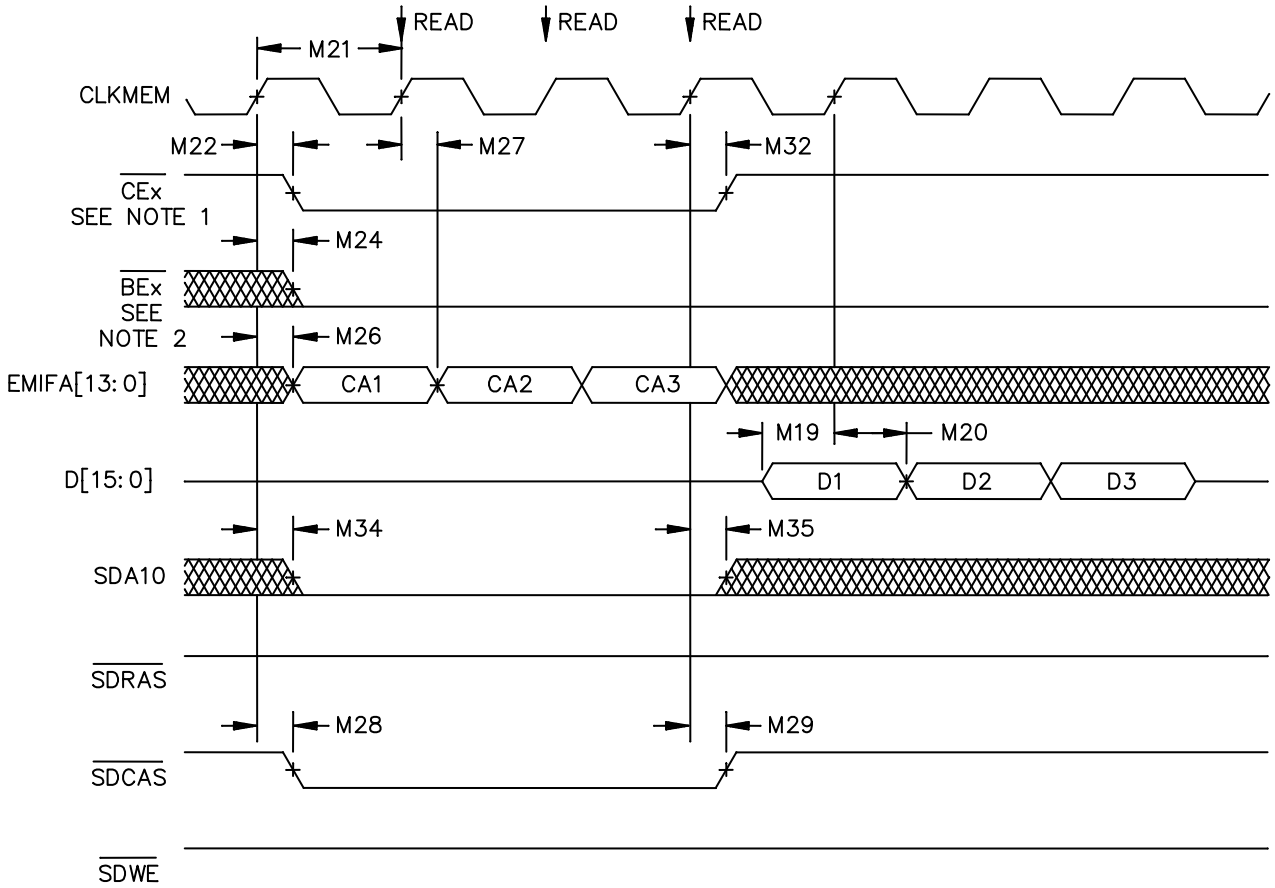
FIGURE 7. Timing waveforms.



ASYNCHRONOUS MEMORY WRITE TIMING

NOTES:
1. CLKOUT is equal to CPU clock.
2. $\overline{\text{CEx}}$ becomes active depending on the memory address space being accessed.
3. A[13:0] for LQFP

FIGURE 8. Timing waveforms.

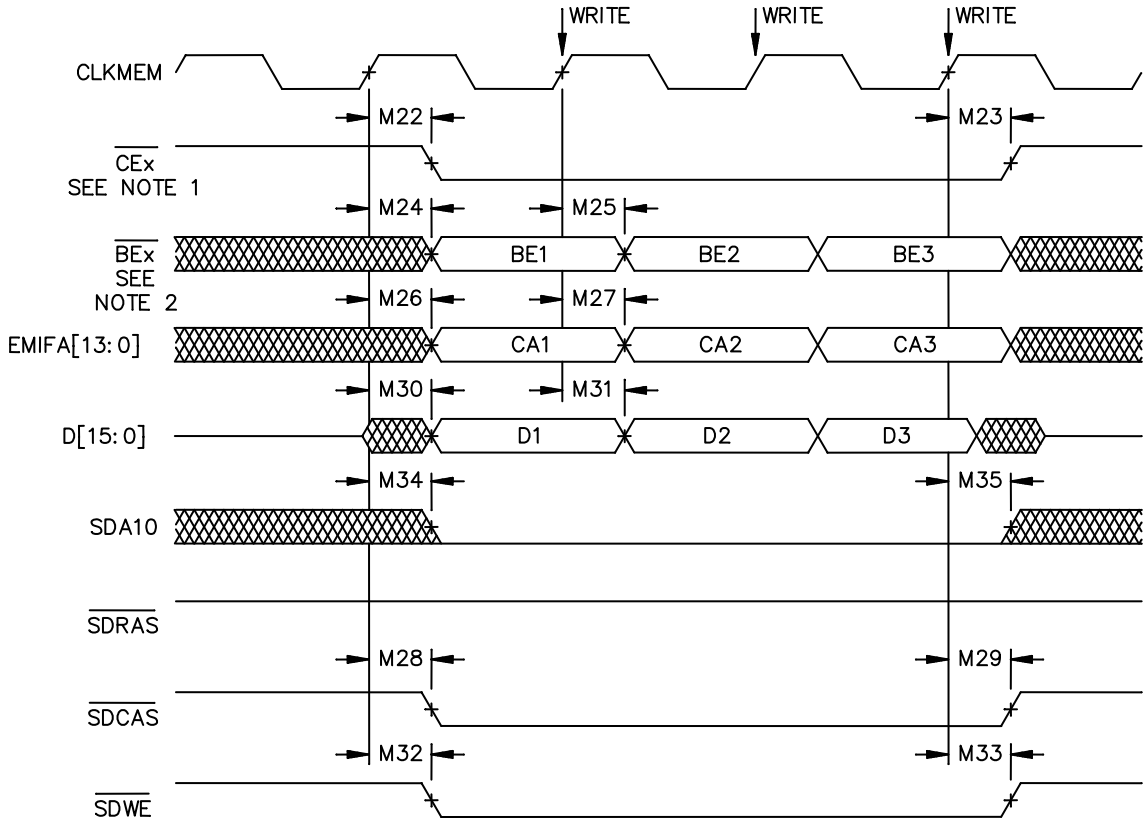


THREE SDRAM READ COMMANDS

NOTES:

1. The chip enable that becomes active depends on the address being accessed.
2. All $\overline{BE[1:0]}$ signals are driven low (active) during reads. Byte manipulation of the read data is performed inside EMIF. These signals remain active until the next access that is not an SDRAM read occurs

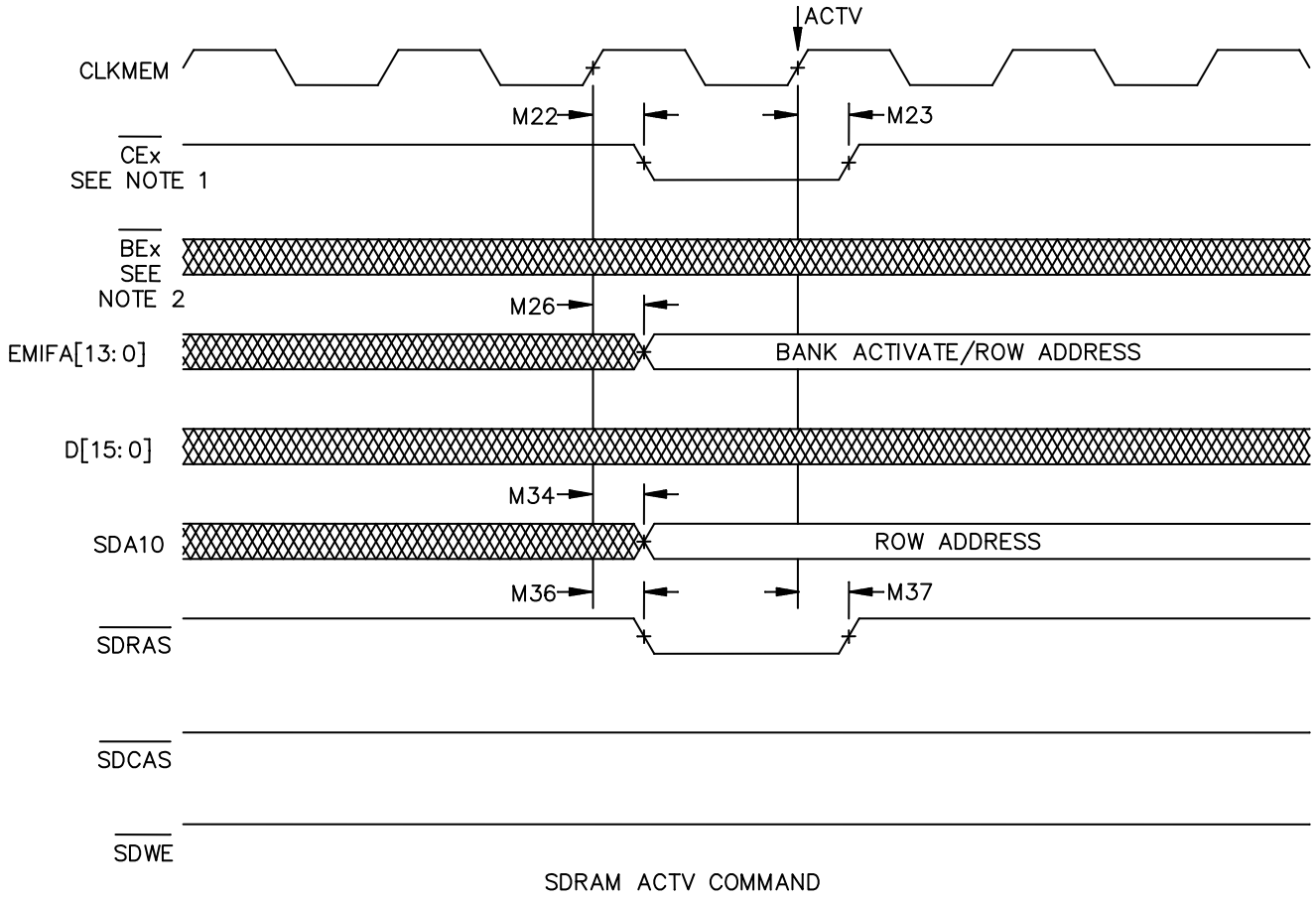
FIGURE 9. Timing waveforms.



NOTES:

1. The chip enable that becomes active depends on the address being accessed.
2. All $\overline{BE[1:0]}$ signals are driven low (active) during reads. Byte manipulation of the read data is performed inside EMIF. These signals remain active until the next access that is not an SDRAM read occurs

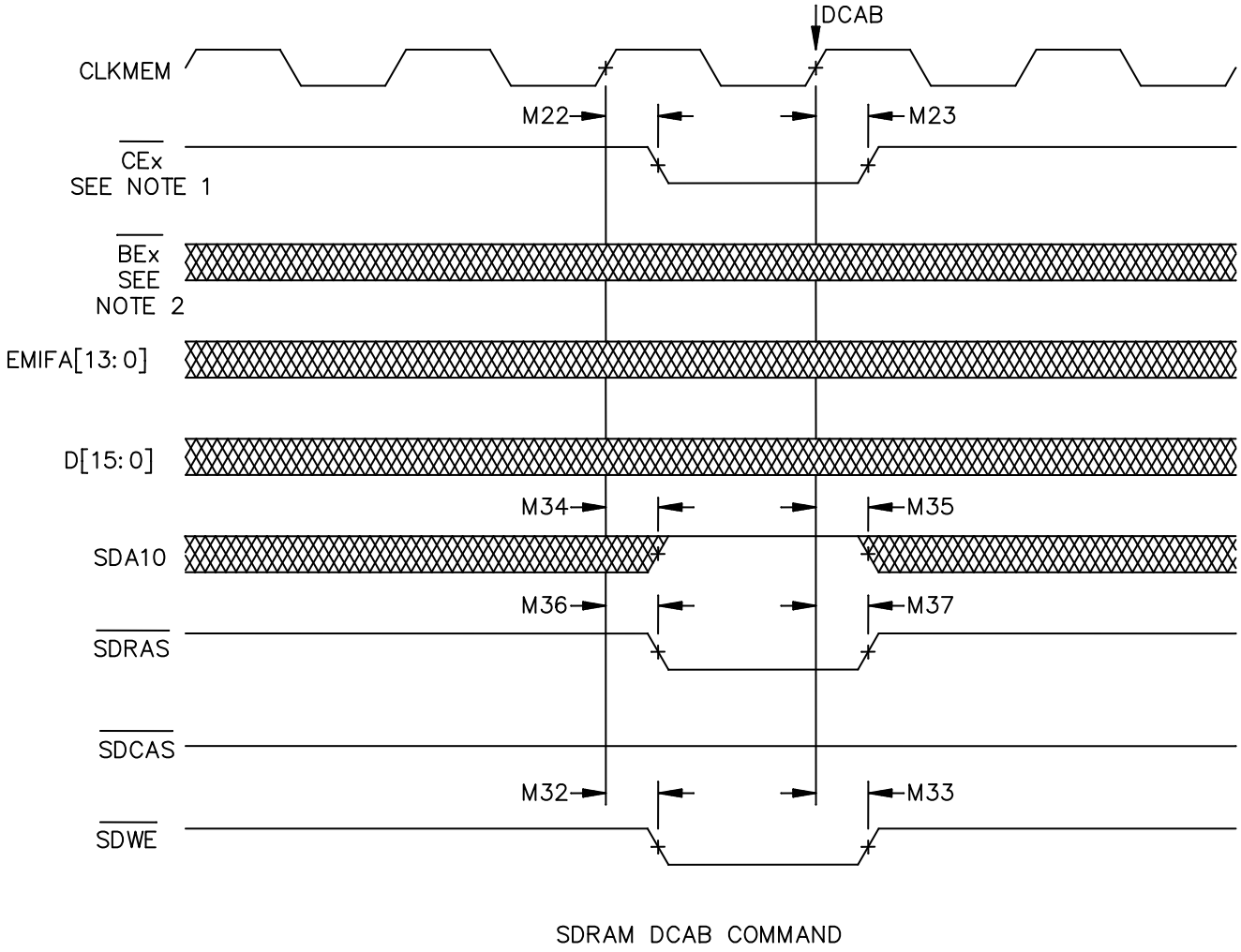
FIGURE 10. Timing waveforms.



NOTES:

1. The chip enable that becomes active depends on the address being accessed.
2. All $\overline{\mathrm{BE}[1:0]}$ signals are driven low (active) during reads. Byte manipulation of the read data is performed inside EMIF. These signals remain active until the next access that is not an SDRAM read occurs

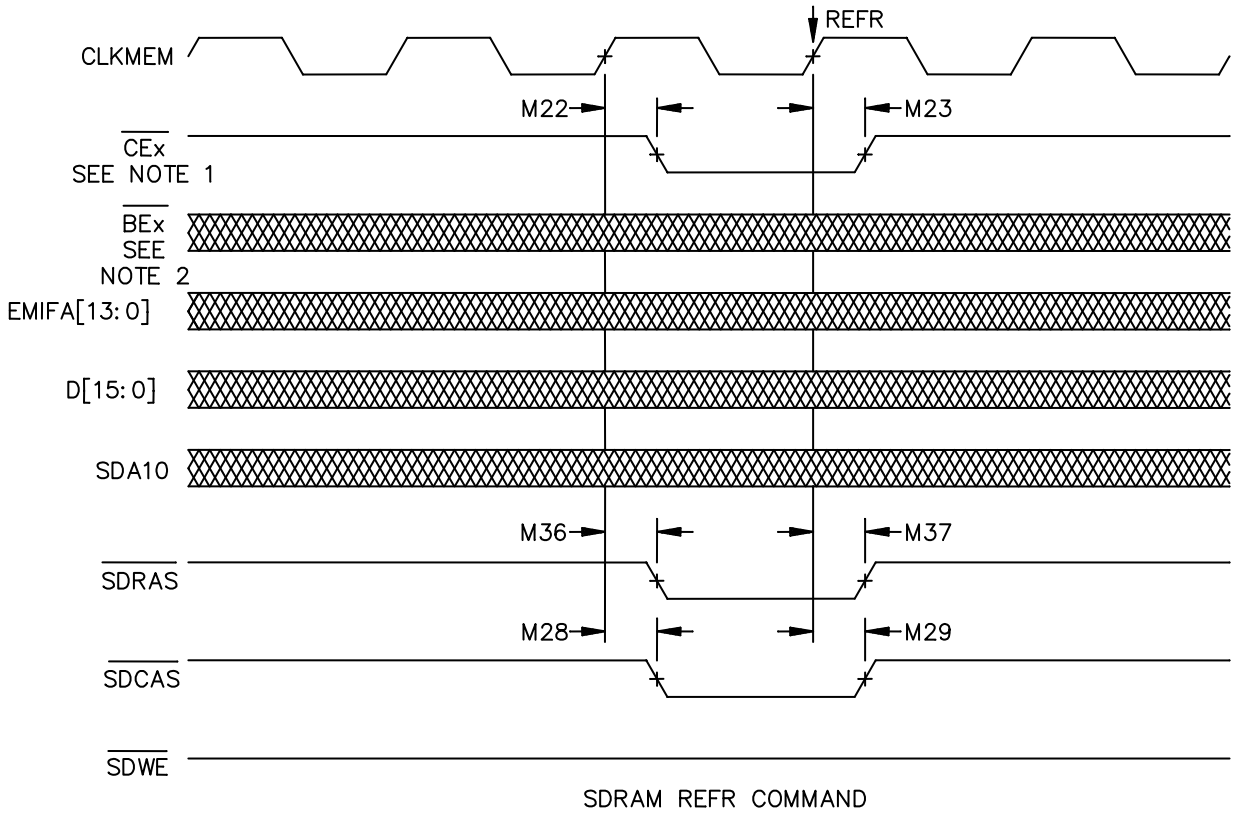
FIGURE 11. Timing waveforms.



NOTES:

1. The chip enable that becomes active depends on the address being accessed.
2. All $\overline{\mathrm{BE}[1:0]}$ signals are driven low (active) during reads. Byte manipulation of the read data is performed inside EMIF. These signals remain active until the next access that is not an SDRAM read occurs

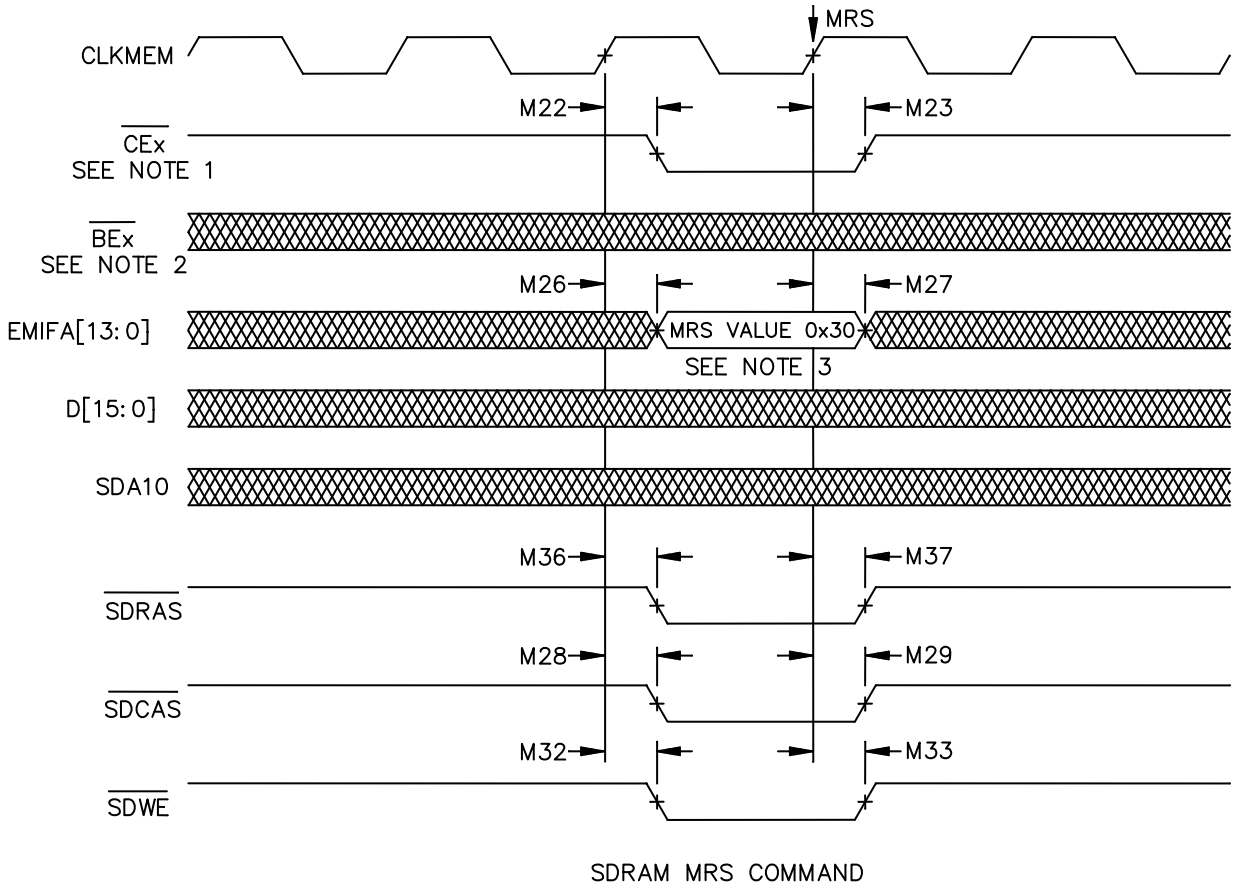
FIGURE 12. Timing waveforms.



NOTES:

1. The chip enable that becomes active depends on the address being accessed.
2. All $\overline{\mathrm{BE}[1:0]}$ signals are driven low (active) during reads. Byte manipulation of the read data is performed inside EMIF. These signals remain active until the next access that is not an SDRAM read occurs

FIGURE 13 Timing waveforms.



NOTES:

1. The chip enable that becomes active depends on the address being accessed.
2. All $\overline{\mathrm{BE}[1:0]}$ signals are driven low (active) during reads. Byte manipulation of the read data is performed inside EMIF. These signals remain active until the next access that is not an SDRAM read occurs.
3. Write burst length = 1
   Read latency = 3
   Burst type = 0 (serial)
   Burst length = 1

FIGURE 14 Timing waveforms.

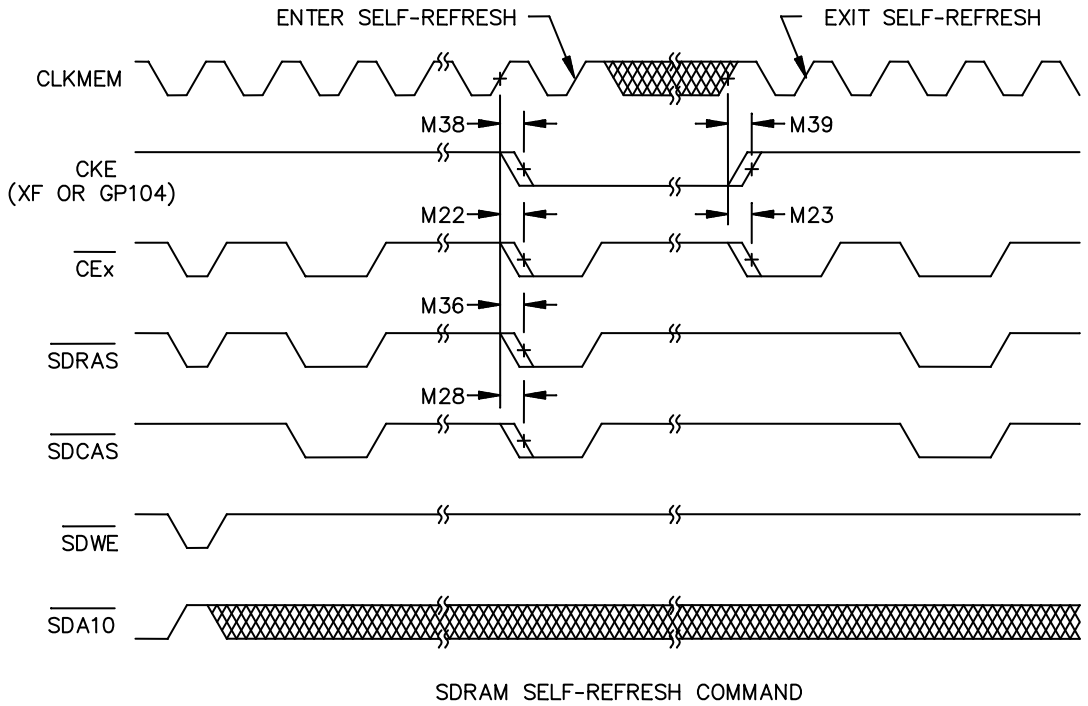


FIGURE 15 Timing waveforms.

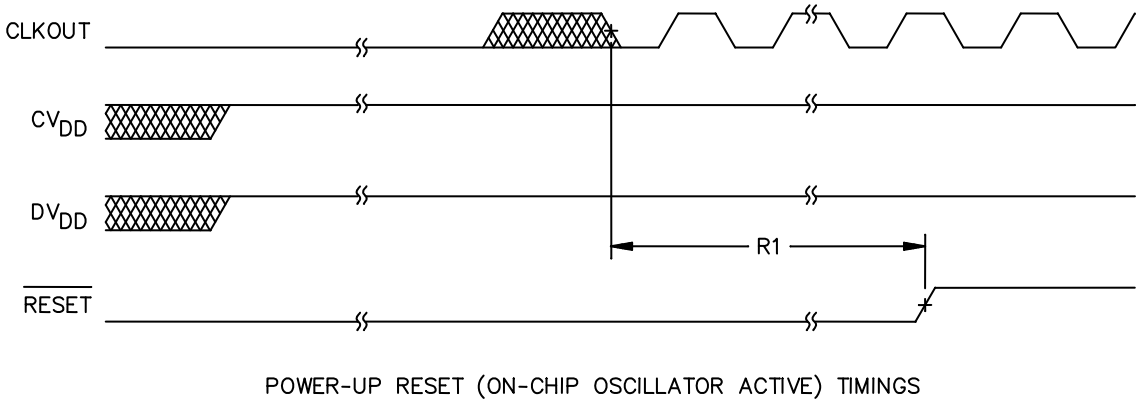


FIGURE 16 Timing waveforms.

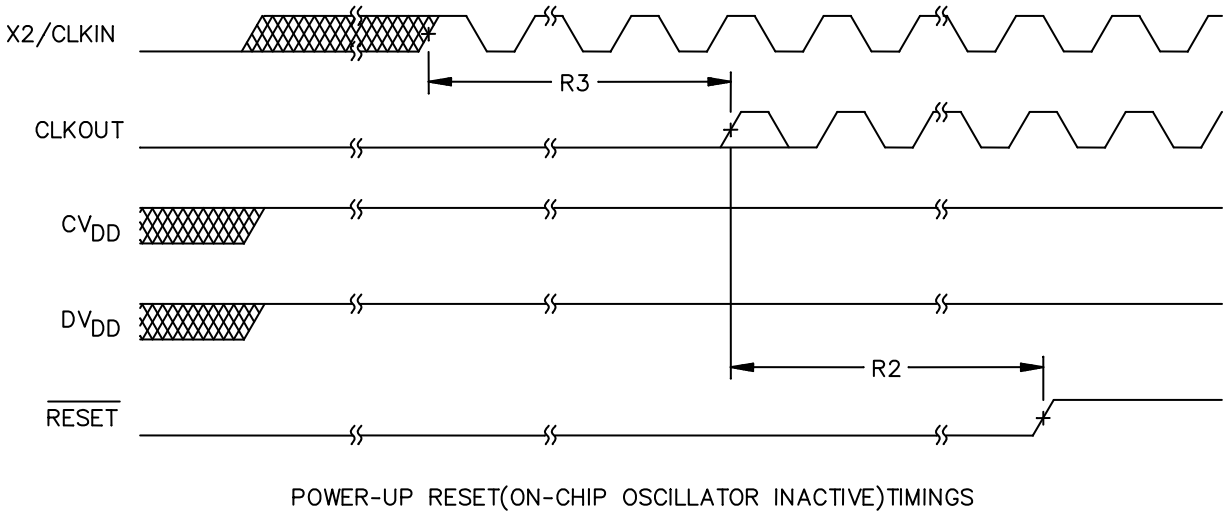
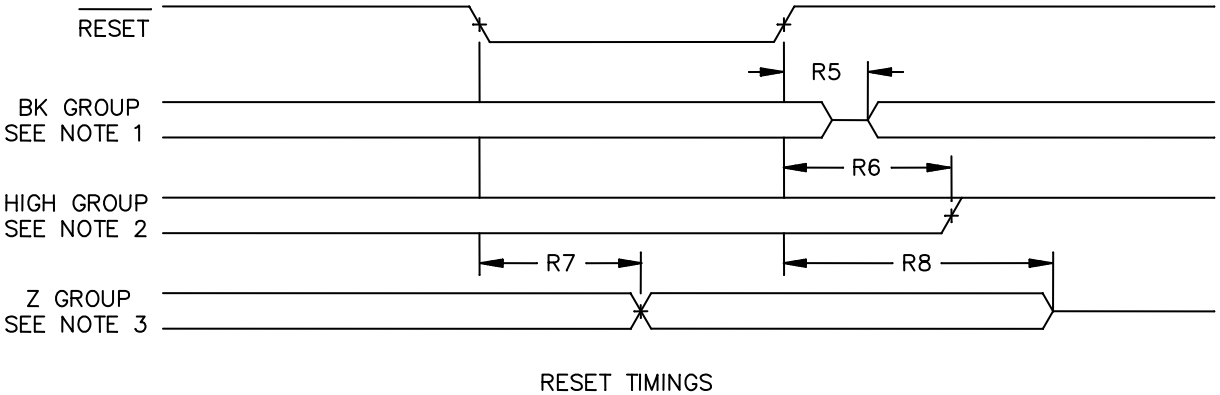


FIGURE 17 Timing waveforms.



NOTES:

1. BK group pins: A'[0], A[15:0], D[15:0], C[14:2], C0, GPIO5, DX1, and DX2.
2. High group pins: C1[HPI.$\overline{\text{HINT}}$], XF.
3. Z group pins: c1[EMIF.AOE], GPIO[7:6, 4:0], TIN/TOUT0, SDA, SCL, CLKR0, FSR0, CLKX0, DFX0, FDSX0, FSX2, CLKX2, FSR2, DR2, CLKR2, FSX1, CLKX1, FSR1, DR1, CLKR1, a[20:16].

FIGURE 18 Timing waveforms.

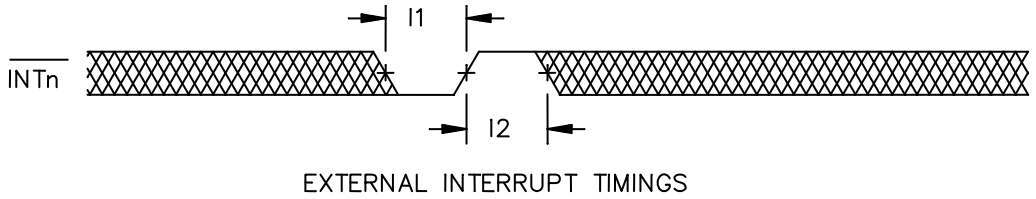


FIGURE 19 Timing waveforms.

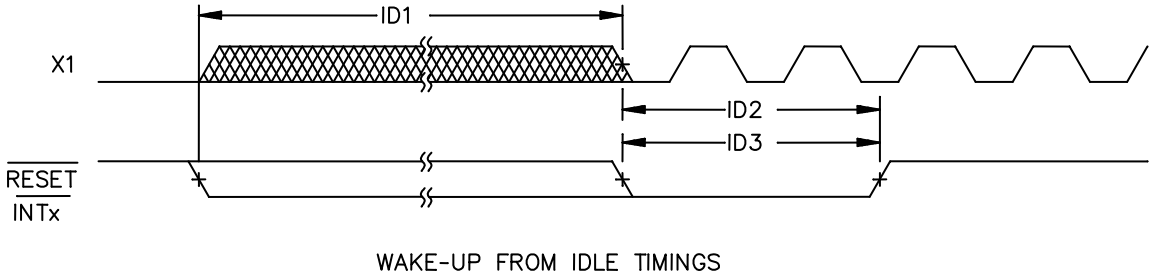
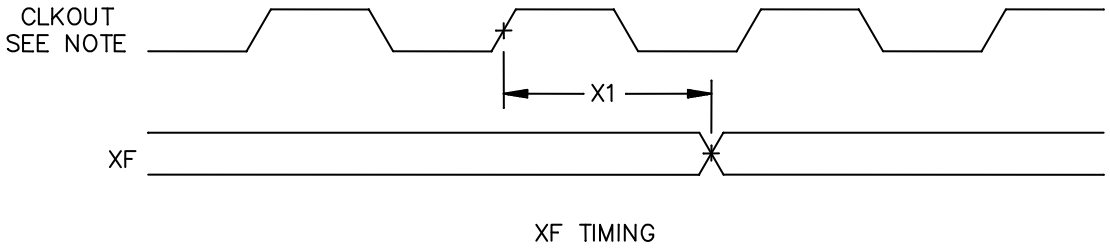
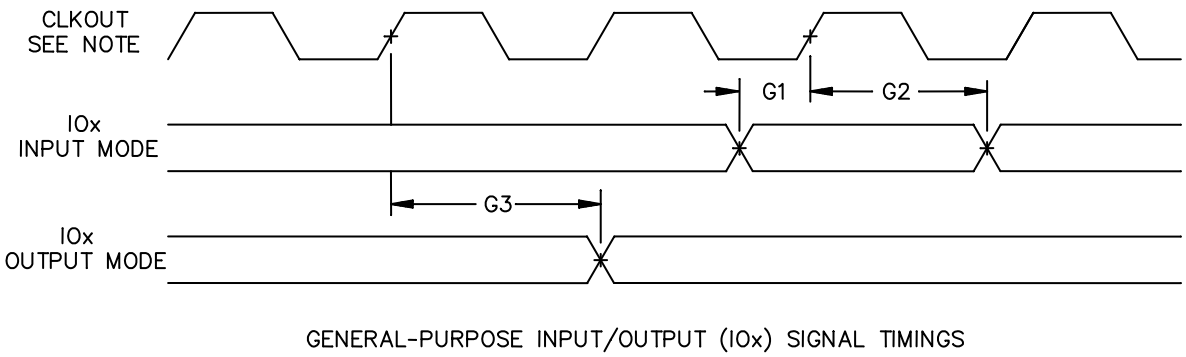


FIGURE 20 Timing waveforms.



NOTES:
1. CLKOUT reflects the CPU clock.

FIGURE 21 Timing waveforms.



NOTES:
1. CLKOUT reflects the CPU clock.

FIGURE 22 Timing waveforms.

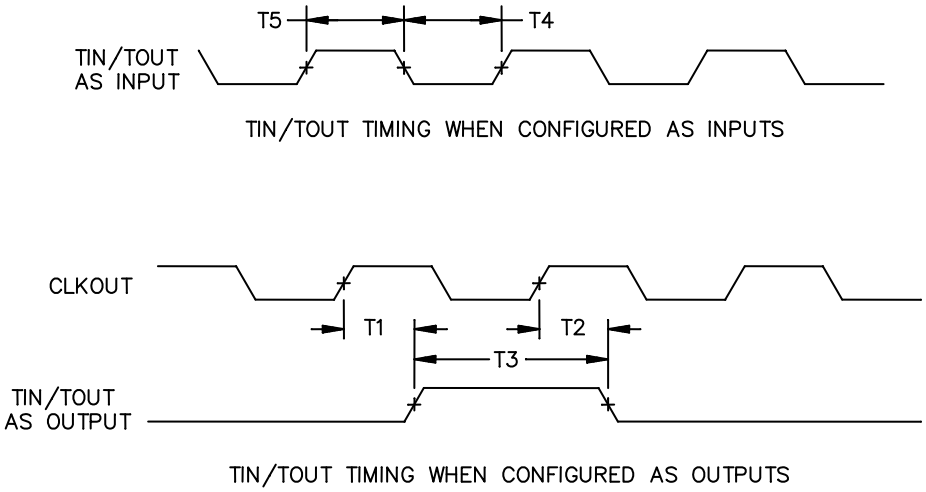


FIGURE 23 Timing waveforms.

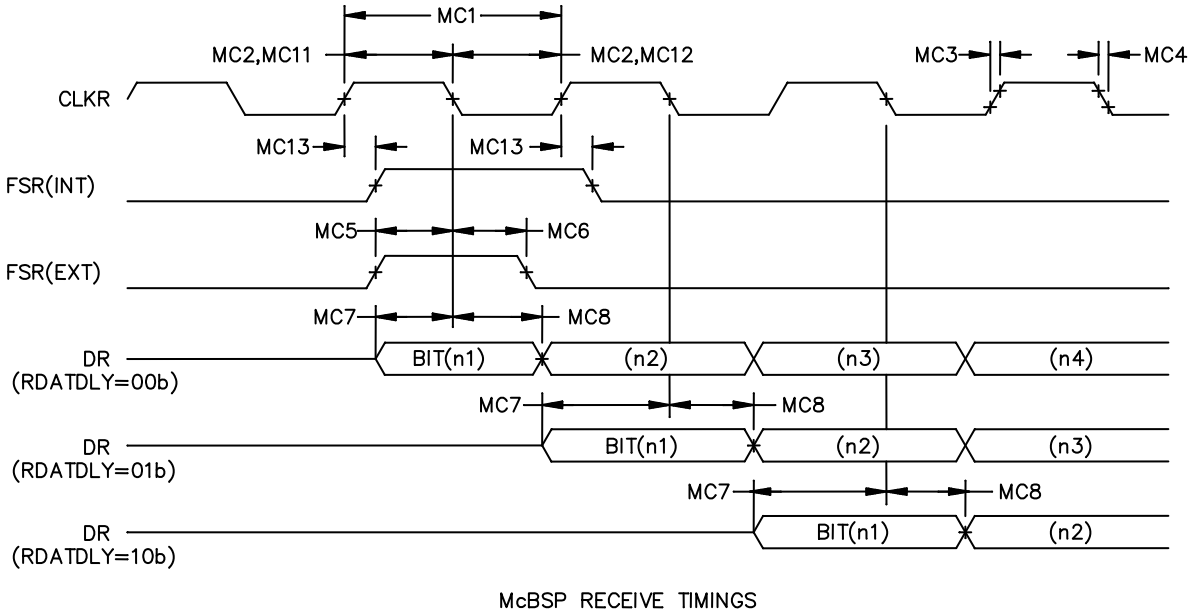


FIGURE 24. Timing waveforms.

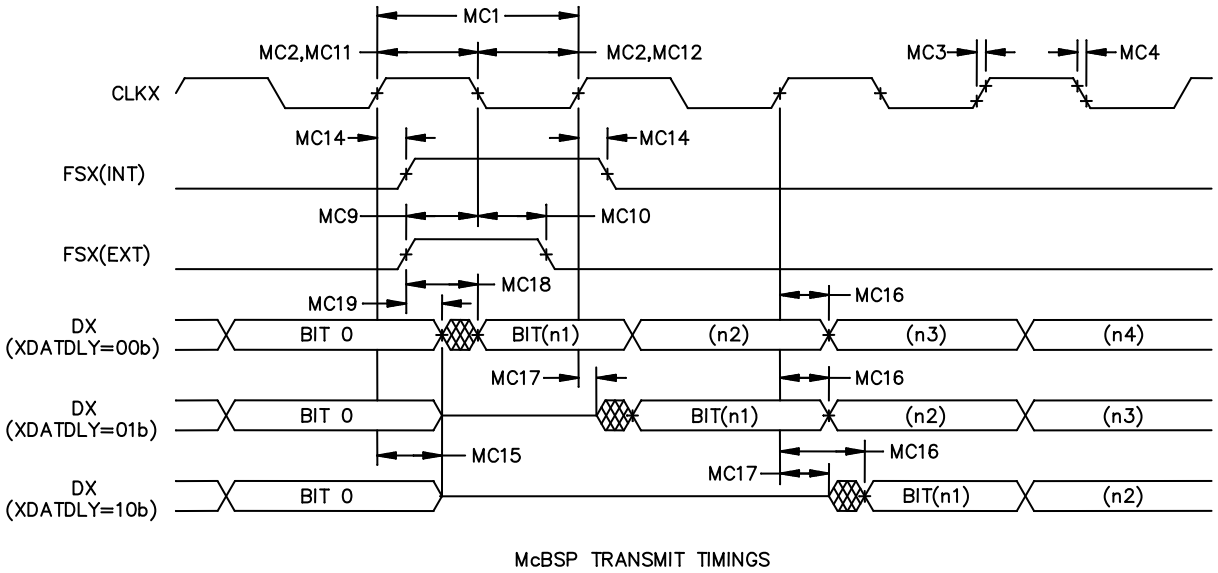


FIGURE 25. Timing waveforms.

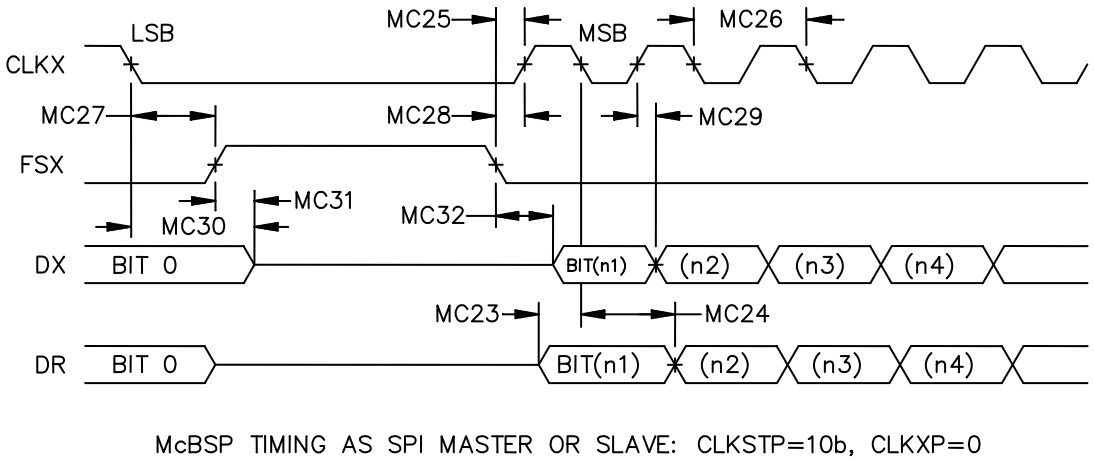


FIGURE 26. Timing waveforms.

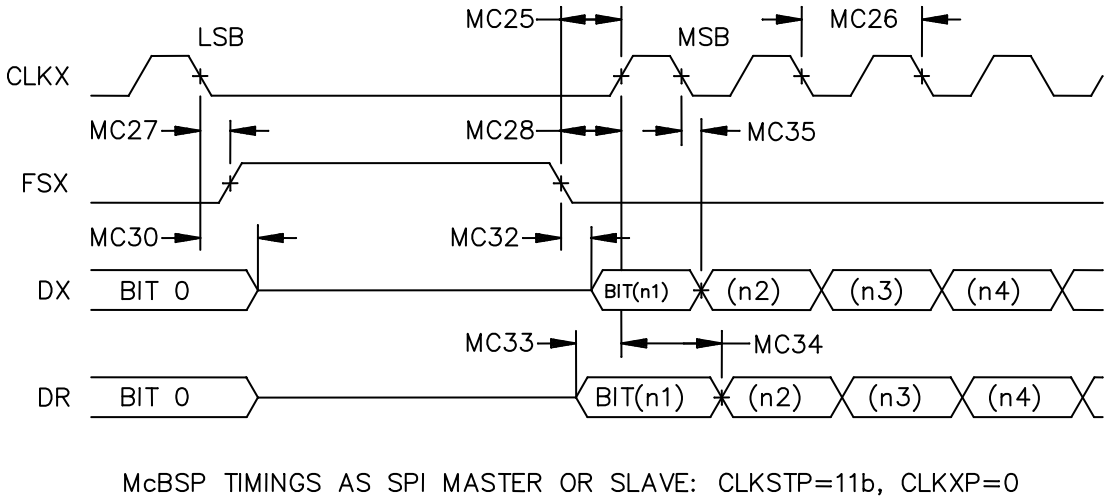


FIGURE 27. Timing waveforms.

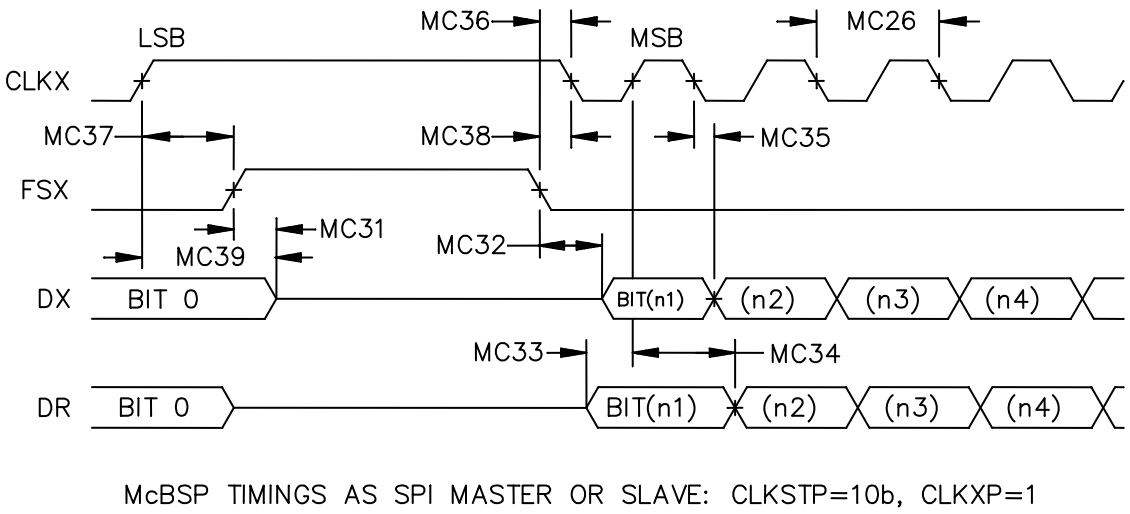


FIGURE 28. Timing waveforms.

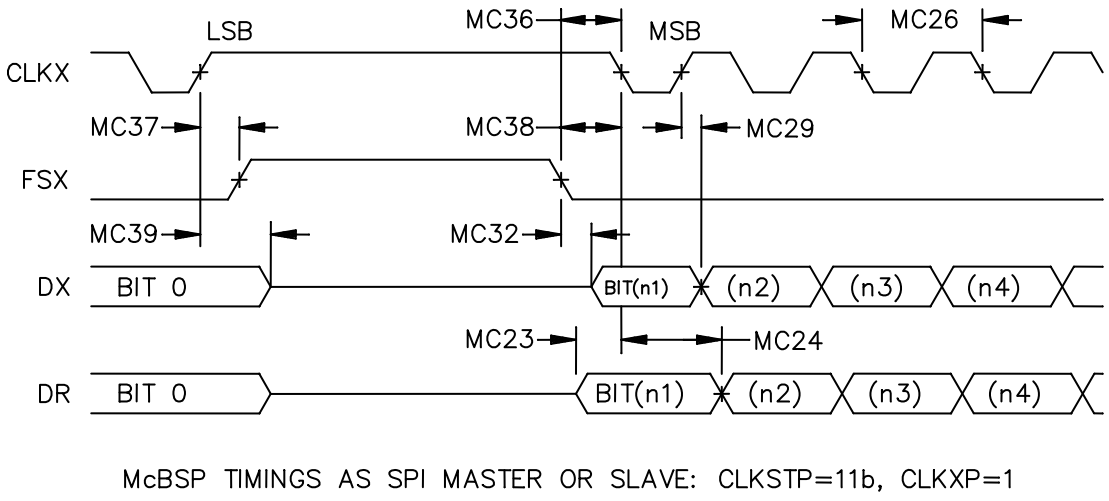
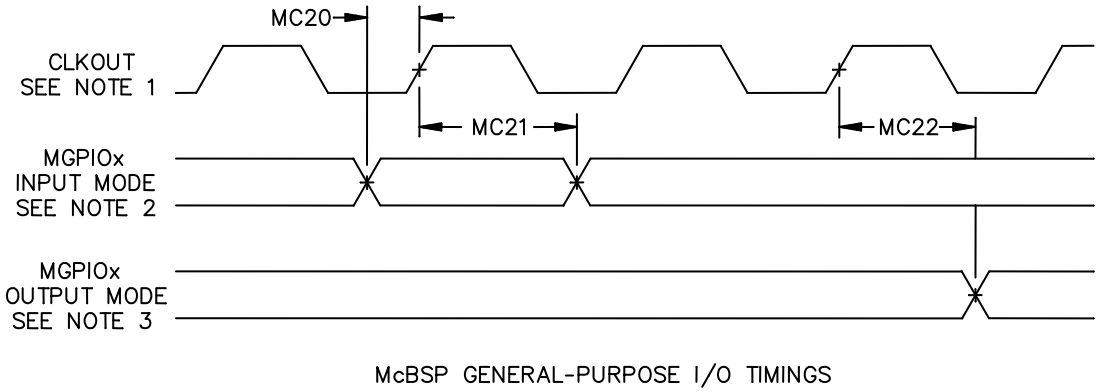


FIGURE 29. Timing waveforms.



NOTES:
1. CLKOUT reflects the CPU clock.
2. MGPIOx refers to CLKRx, FSRx, DRx, CLKXx, or FSXx when configured as a general purpose input.
3. MGPIOx refers to CLKRx, FSRx, CLKXx, FSXx, or DXx when configured as a general purpose output

FIGURE 30. Timing waveforms.

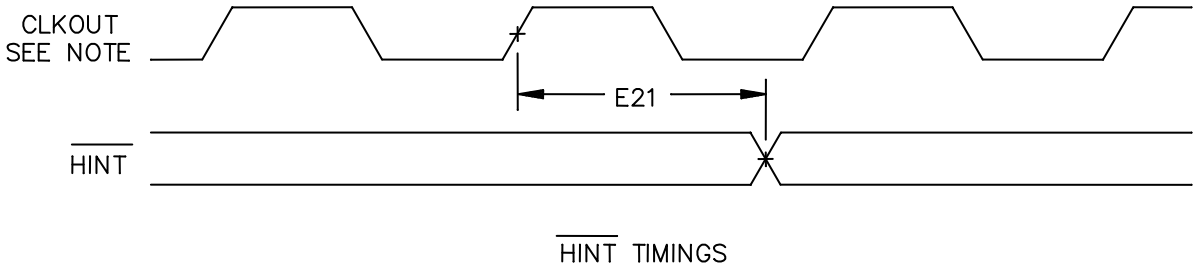
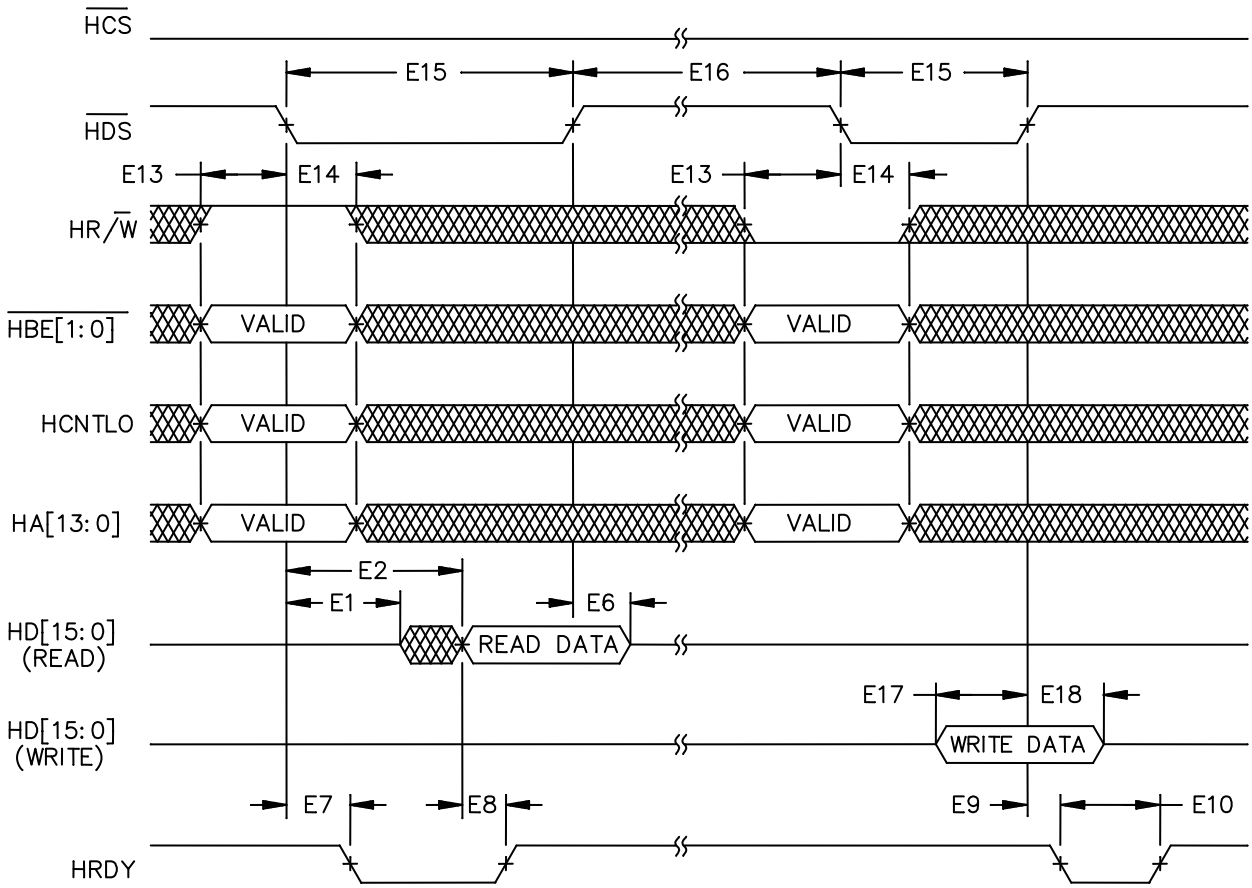


FIGURE 31. Timing waveforms.

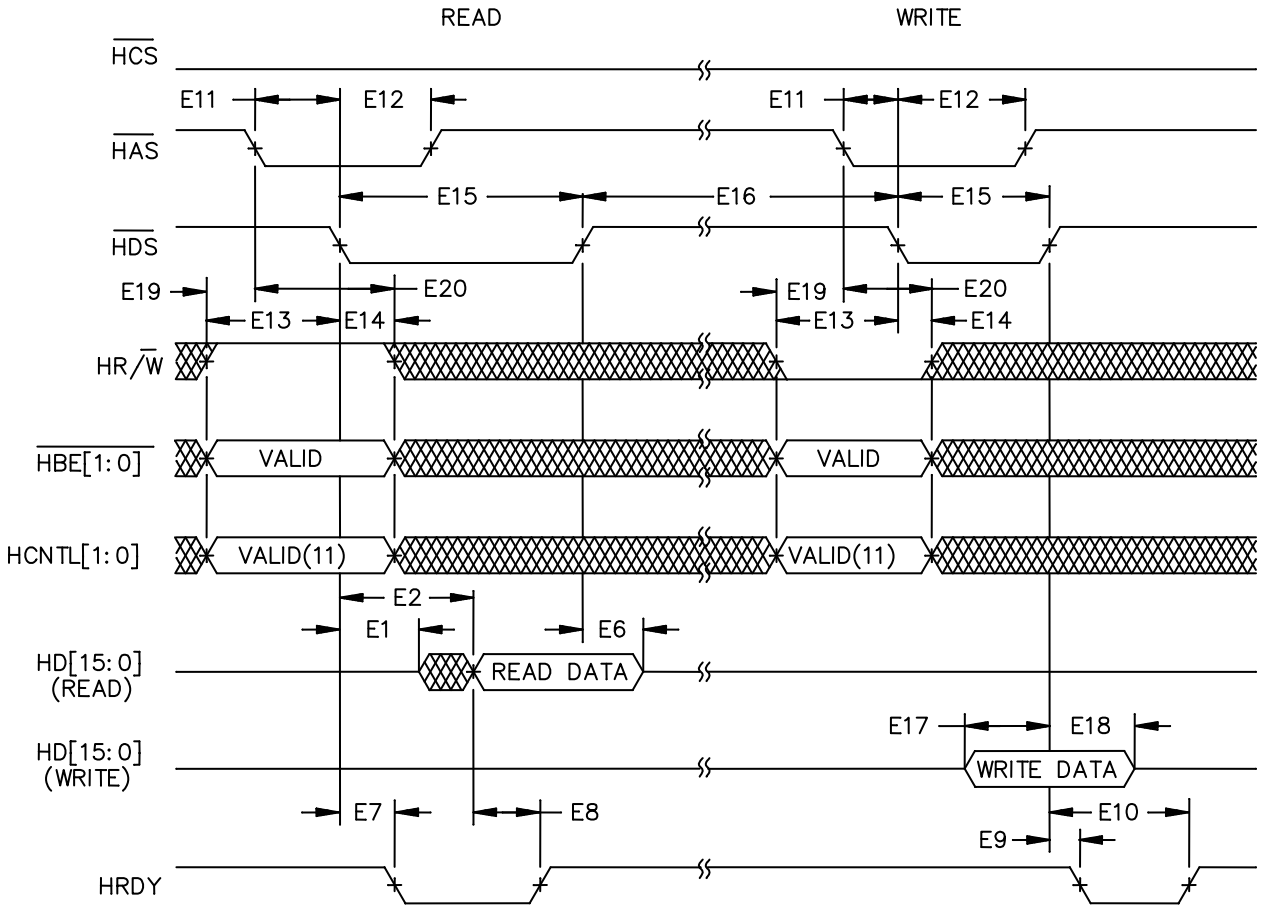


EHPI NONMULTIPLEXED READ/WRITE TIMINGS

NOTES:

1. Any non-multiplexed access with HCNTL0 low will result in HPIC register access. For data read or write, HCNTL0 must stay high during the EHPI access.
2. The falling edge of $\overline{\mathrm{HCS}}$ must occur concurrent with or before the falling edge of $\overline{\mathrm{HDS}}$. The rising edge of $\overline{\mathrm{HCS}}$ must occur concurrent with or after the rising edge of $\overline{\mathrm{HDS}}$. If $\overline{\mathrm{HDS1}}$ and/or $\overline{\mathrm{HDS2}}$ are tied permanently active and $\overline{\mathrm{HCS}}$ is used as a strobe, the timing requirements shown for $\overline{\mathrm{HDS}}$ apply to $\overline{\mathrm{HCS}}$. HRDY is always driven to the same value as its internal state.

FIGURE 32. Timing waveforms.

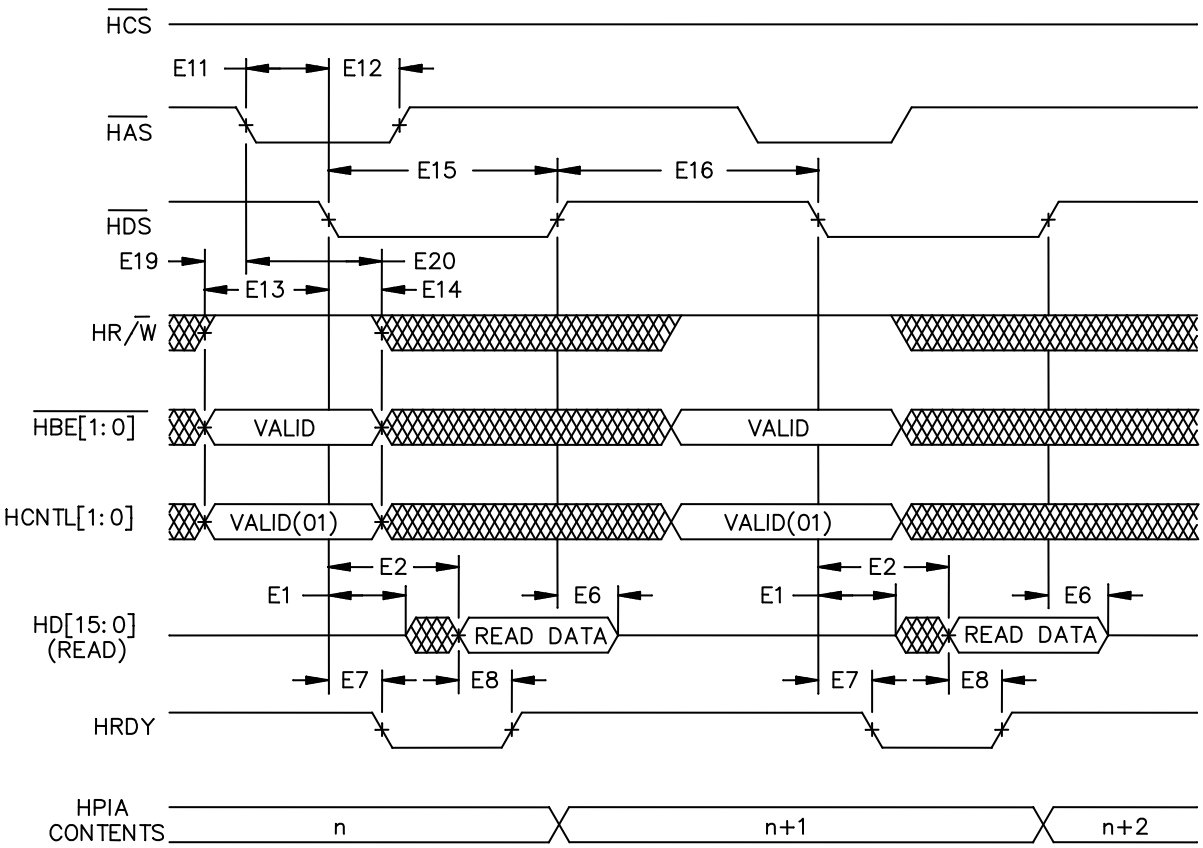


EHPI MULTIPLEXED MEMORY (HPID) READ/WRITE TIMINGS WITHOUT AUTOINCREMENT

NOTES:

1. The falling edge of $\overline{HCS}$ must occur concurrent with or before the falling edge of $\overline{HDS}$. The rising edge of $\overline{HCS}$ must occur concurrent with or after the rising edge of $\overline{HDS}$. If $\overline{HDS1}$ and/or $\overline{HDS2}$ are tied permanently active and $\overline{HCS}$ is used as a strobe, the timing requirements shown for $\overline{HDS}$ apply to $\overline{HCS}$. HRDY is always driven to the same value as its internal state.

FIGURE 33. Timing waveforms.

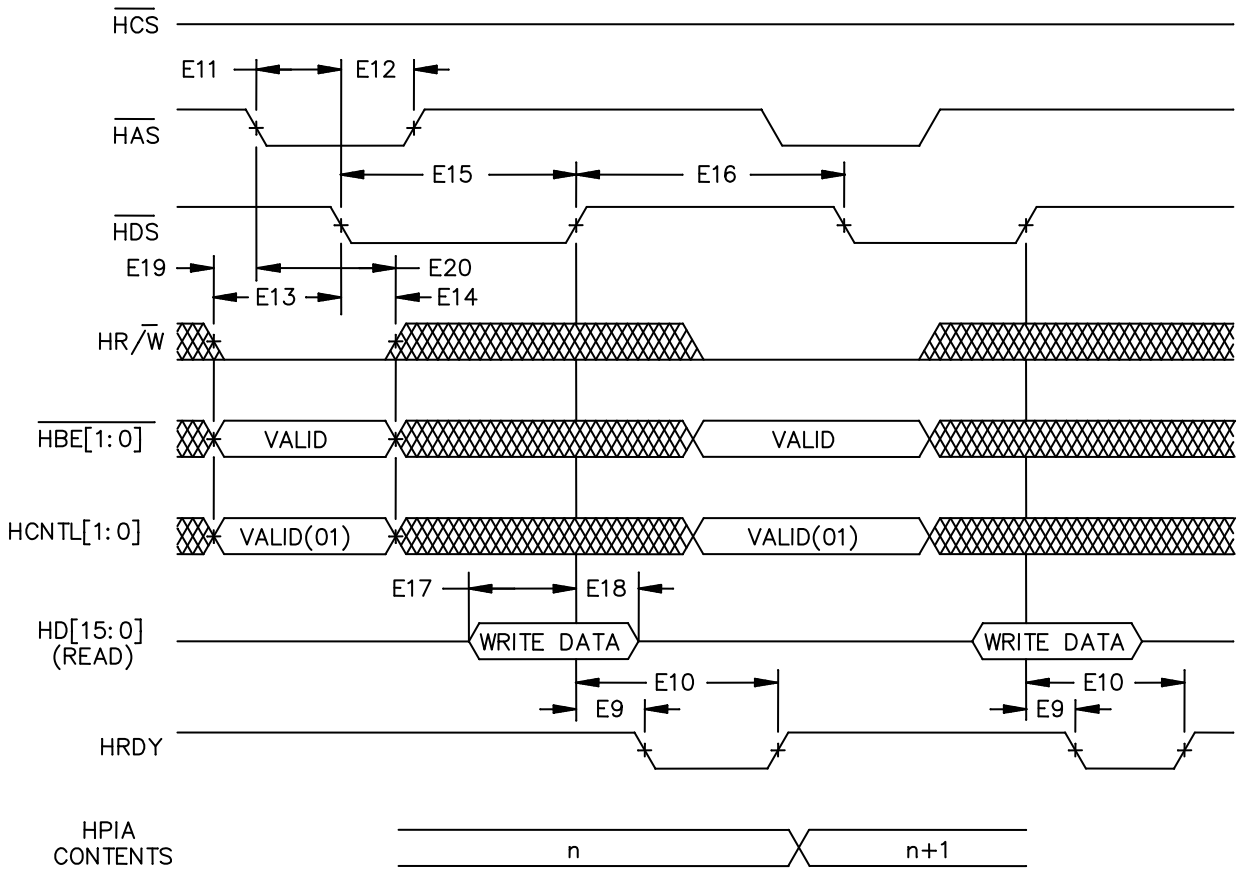


EHPI MULTIPLEXED MEMORY (HPID) READ TIMINGS WITH AUTOINCREMENT

NOTES:

1. During autoincrement mode, although the EHPI internally increments the memory address, reads of the HPIA register by the host will always indicate the base address.
2. In autoincrement mode, if $\overline{\mathrm{HBE}[1:0]}$ are used to access the data as 8 bit wide units, the HPIA increments only following each high byte ($\overline{\mathrm{HBE1}}$ low) access.
3. The falling edge of $\overline{\mathrm{HCS}}$ must occur concurrent with or before the falling edge of $\overline{\mathrm{HDS}}$. The rising edge of $\overline{\mathrm{HCS}}$ must occur concurrent with or after the rising edge of $\overline{\mathrm{HDS}}$. If $\overline{\mathrm{HDS1}}$ and/or $\overline{\mathrm{HDS2}}$ are tied permanently active and $\overline{\mathrm{HCS}}$ is used as a strobe, the timing requirements shown for $\overline{\mathrm{HDS}}$ apply to $\overline{\mathrm{HCS}}$. HRDY is always driven to the same value as its internal state.

FIGURE 34. Timing waveforms.

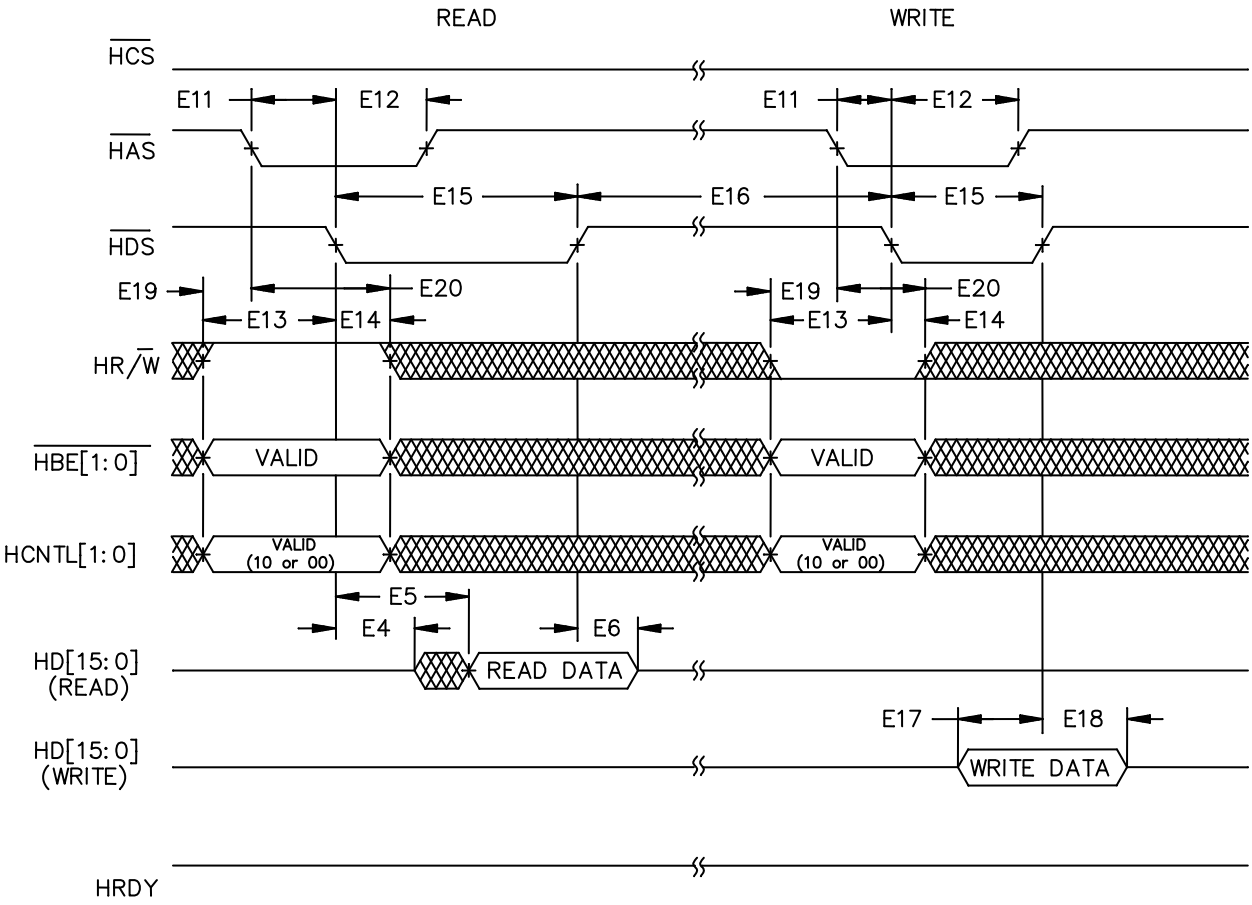


EHPI MULTIPLEXED MEMORY (HPID) WRITE TIMINGS WITH AUTOINCREMENT

NOTES:

1. During autoincrement mode, although the EHPI internally increments the memory address, reads of the HPIA register by the host will always indicate the base address.
2. The falling edge of $\overline{\text{HCS}}$ must occur concurrent with or before the falling edge of $\overline{\text{HDS}}$. The rising edge of $\overline{\text{HCS}}$ must occur concurrent with or after the rising edge of $\overline{\text{HDS}}$. If $\overline{\text{HDS1}}$ and/or $\overline{\text{HDS2}}$ are tied permanently active and $\overline{\text{HCS}}$ is used as a strobe, the timing requirements shown for $\overline{\text{HDS}}$ apply to $\overline{\text{HCS}}$. HRDY is always driven to the same value as its internal state.

FIGURE 35. Timing waveforms.



EHPI MULTIPLEXED REGISTER READ/WRITE TIMINGS

NOTES:

1. During autoincrement mode, although the EHPI internally increments the memory address, reads of the HPIA register by the host will always indicate the base address.
2. The falling edge of $\overline{HCS}$ must occur concurrent with or before the falling edge of $\overline{HDS}$. The rising edge of $\overline{HCS}$ must occur concurrent with or after the rising edge of $\overline{HDS}$. If $\overline{HDS1}$ and/or $\overline{HDS2}$ are tied permanently active and $\overline{HCS}$ is used as a strobe, the timing requirements shown for $\overline{HDS}$ apply to $\overline{HCS}$. HRDY is always driven to the same value as its internal state.

FIGURE 36. Timing waveforms.

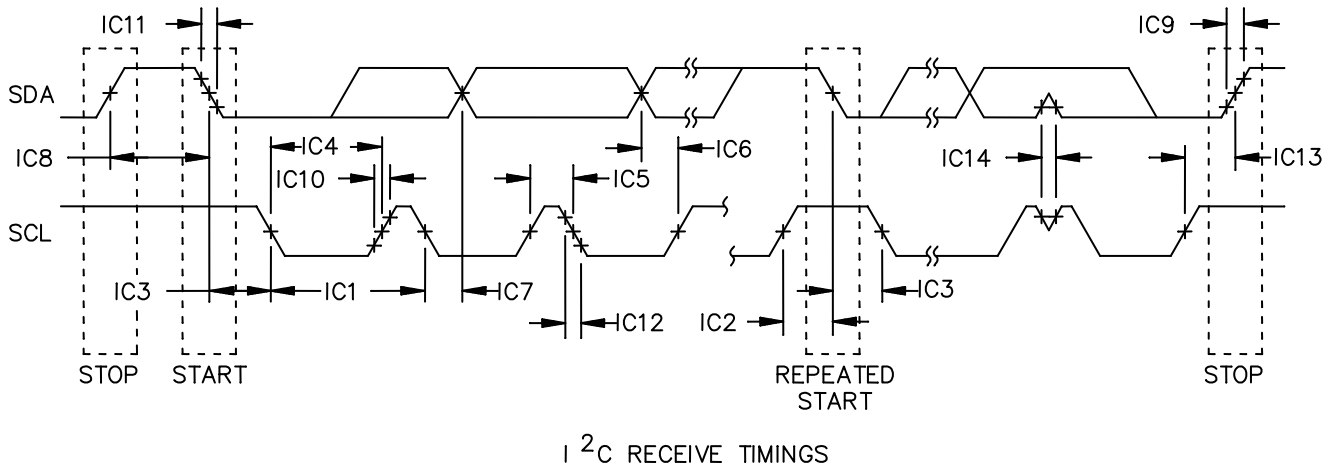


FIGURE 37. Timing waveforms.

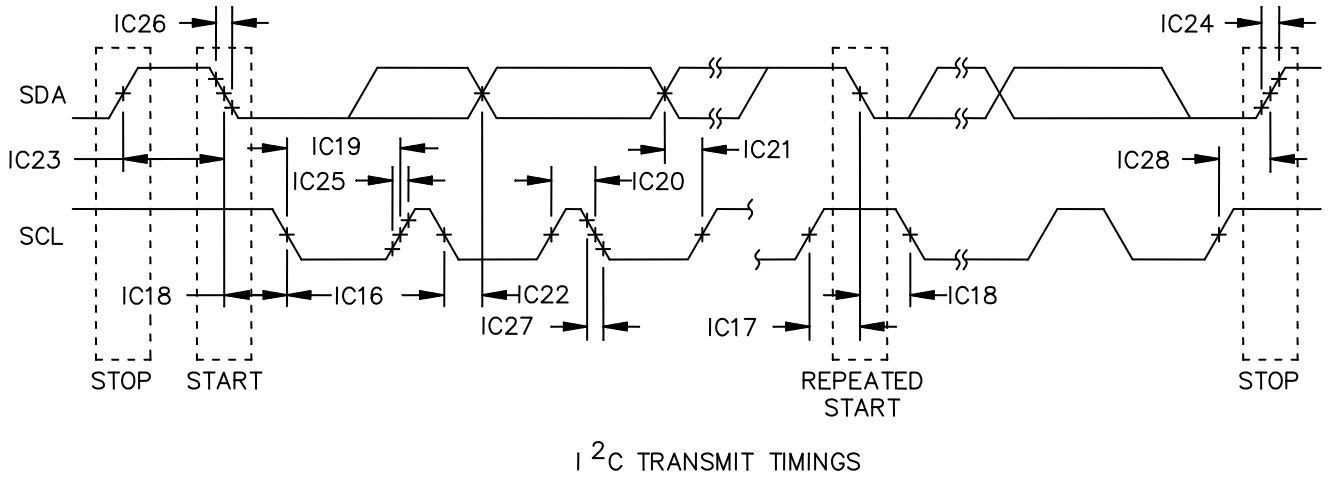


FIGURE 38. Timing waveforms.

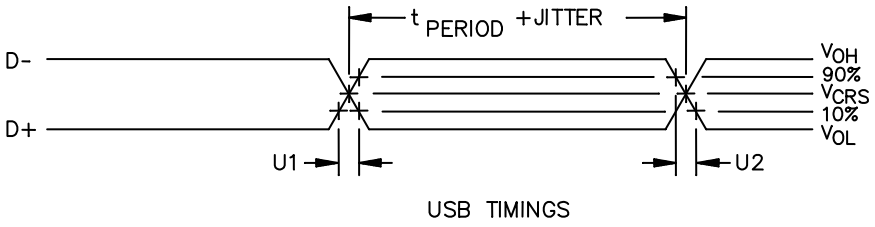
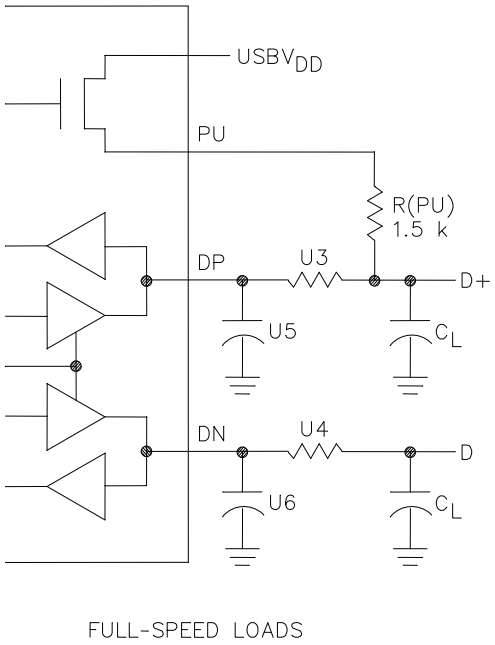


FIGURE 39. Timing waveforms.



NOTES:
1. A full speed buffer is measured with the load shown.
2. C_L = 50 pF

FIGURE 40. Timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/09647-01XA	01295	SM320VC5507PGESEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493