REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add typical limits to Table I parameters. Make correction to note 2 as specified under figure 1. Add top side marking under paragraph 6.3. Update document paragraphs to current requirements. - ro	15-08-06	C. SAFFLE

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**			A	A	A	A	A	A	A	A	A	A	A								
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PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 09-09-29	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** CHARLES F. SAFFLE	**TITLE** MICROCIRCUIT, LINEAR, 1 A, HIGH OUTPUT CURRENT PULSE WIDTH MODULATION CONVERTER, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/09645**
	REV **A**	**PAGE** 1 **OF** 11

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a 1 A, high output current pulse width modulation converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/09645	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TPS5410-EP	1 A, high output current pulse width modulation converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MS-012-AA	Plastic surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

Input voltage range (V_{IN}):

V_{IN} pin ..... -0.3 V to 40 V 3/
BOOT pin ..... -0.3 V to 50 V
PH pin (steady state) ..... -0.6 V to 40 V 3/
ENA pin ..... -0.3 V to 7 V
VSENSE pin ..... -0.3 V to 3 V
BOOT-PH pin ..... 10 V
PH pin (transient < 10 ns) ..... -1.2 V

Source current (I_O) (PH pin) ..... Internally limited

Leakage current (I_{ILK}) (PH pin) ..... 10 μA
Operating virtual junction temperature range ..... -55°C to +150°C
Storage temperature range ..... -65°C to +150°C

1.4 Recommended operating conditions. 4/

Input voltage range (V_{IN}) ..... 5.5 V to 36 V
Operating junction temperature range (T_J) ..... -55°C to +125°C

1.5 Dissipation ratings table. 5/ 6/

Package	Thermal impedance junction to ambient
Case outline X 7/	75°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ All voltage values are with respect to network ground terminal.
3/ Approaching the absolute maximum rating for the V_{IN} pin may cause the voltage on the PH pin to exceed the absolute maximum rating.
4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
5/ Maximum power dissipation may be limited by overcurrent protection.
6/ Power rating at a specific ambient temperature T_A should be determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final printed circuit board (PCB) should strive to keep the junction temperature at or below 125°C for best performance and long term reliability. See thermal calculations in the application section of the manufacturer’s datasheet for more information.
7/ Test board conditions:
3 inch x 3 inch, two layers, thickness: 0.062 inch (1.57 mm). 2 ounce copper traces located on the top and bottom of the PCB.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions V_{IN} = 5.5 V to 36 V unless otherwise specified	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Supply voltage (V_{IN} pin) section							
Quiescent current	I_Q	VSENSE = 2 V, not switching, PH pin open	-55°C to +125°C	01		4.4	mA
					3 typical		
		Shutdown, ENA = 0 V				50	µA
					18 typical		
Undervoltage lockout (UVLO) section							
Start threshold voltage, UVLO	V_{TH}		-55°C to +125°C	01	5.3 typical		V
Hysteresis voltage, UVLO	V_{HYS}		-55°C to +125°C	01	330 typical		mV
Voltage reference section							
Voltage reference accuracy	V_{RA}		25°C	01	1.202	1.239	V
					1.221 typical		
		I_O = 0 A - 1 A	-55°C to +125°C		1.192	1.245	
					1.221 typical		
Oscillator section							
Internally set free running frequency	f_{ISFR}		+25°C	01	400	600	kHz
					500 typical		
			-55°C to +125°C		380	600	
Minimum controllable on time	tc_{min}		-55°C to +125°C	01		210	ns
					150 typical		
Maximum duty cycle	DC_{MAX}		-55°C to +125°C	01	87		%
					89 typical		

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{IN} = 5.5 V to 36 V unless otherwise specified	Temperature, T_J	Device type	Limits		Unit
					Min	Max	
Enable (ENA pin) section							
Start threshold voltage, ENA	V_{START}		-55°C to +125°C	01		1.3	V
Stop threshold voltage, ENA	V_{STOP}		-55°C to +125°C	01	0.5		V
Hysteresis voltage, ENA	V_{HYS}		-55°C to +125°C	01	450 typical		mV
Internal slow start time	t_{ISS}	(0 ~ 100%)	-55°C to +125°C	01	5.35	10	ms
					8 typical		
Current limit section							
Current limit	I_L		+25°C	01	1.2	1.8	A
					1.5 typical		
			-55°C to +125°C		0.45	4.6	
Current limit hiccup time	t_{CL}		-55°C to +125°C	01	13	22.5	ms
					16 typical		
Thermal shutdown section							
Thermal shutdown trip point	T_{TSTP}		-55°C to +125°C	01	135		°C
					162 typical		
Thermal shutdown hysteresis	T_{TSH}		-55°C to +125°C	01	14 typical		°C
Output MOSFET section							
High side power MOSFET switch	$r_{DS(on)}$	V_{IN} = 5.5 V	-55°C to +125°C	01	150 typical		mΩ
		V_{IN} = 10 V – 36 V			110 typical		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

Case X

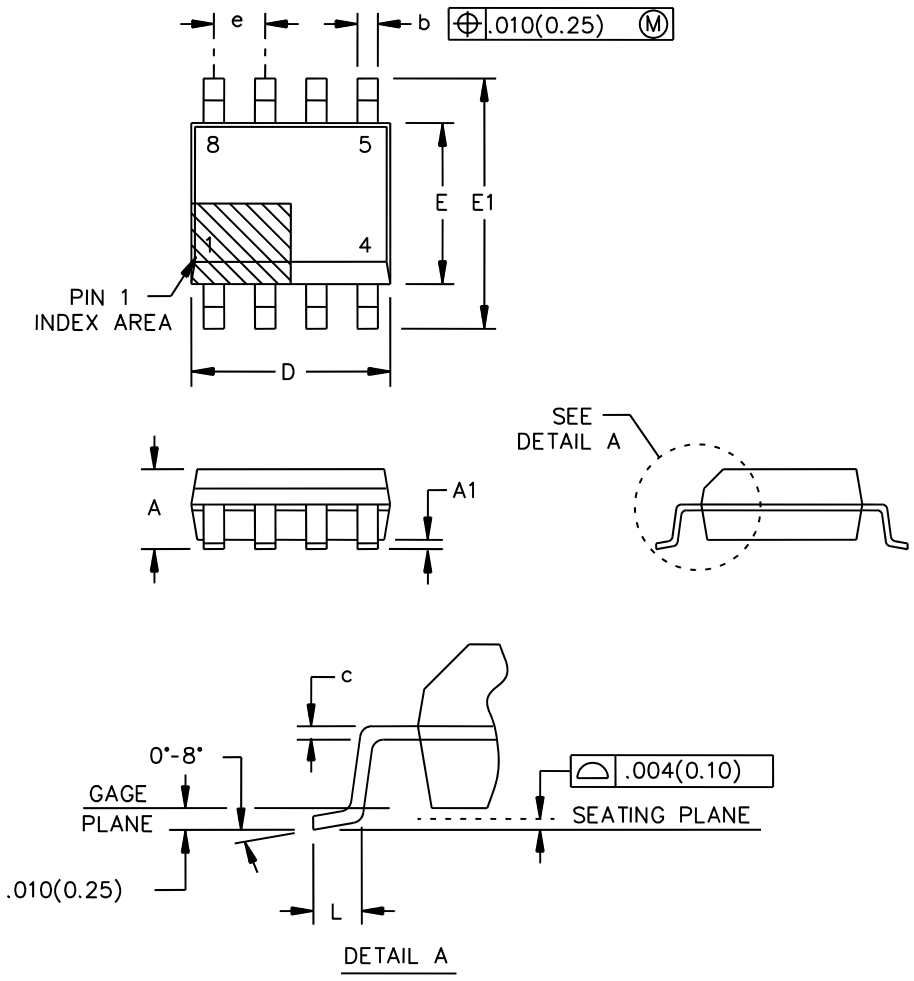

FIGURE 1. Case outline.

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Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.069	---	1.75
A1	0.004	0.010	0.10	0.25
b	0.012	0.020	0.31	0.51
c	0.005	0.010	0.13	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
E1	0.228	0.244	5.80	6.20
e	0.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27
n	8		8	

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) per side.
4. Falls within reference to JEDEC MS-012-AA.

FIGURE 1. Case outline – continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	BOOT	Boost capacitor for the high side field effect transistor (FET) gate driver. Connect 0.01 μF low equivalent series resistance (ESR) capacitor from BOOT pin to PH pin.
2	NC	Not connected internally.
3	NC	Not connected internally.
4	VSENSE	Feedback voltage for the regulator. Connect to output voltage divider.
5	ENA	On/off control. Below 0.5 V, the device stops switching. Float the pin to enable.
6	GND	Ground.
7	V_{IN}	Input supply voltage. Bypass V_{IN} pin to GND pin close to device package with a high quality low ESR ceramic capacitor.
8	PH	Source of the high side power metal oxide semiconductor field effect transistor (MOSFET). Connected to external inductor and diode.

FIGURE 2. Terminal connections.

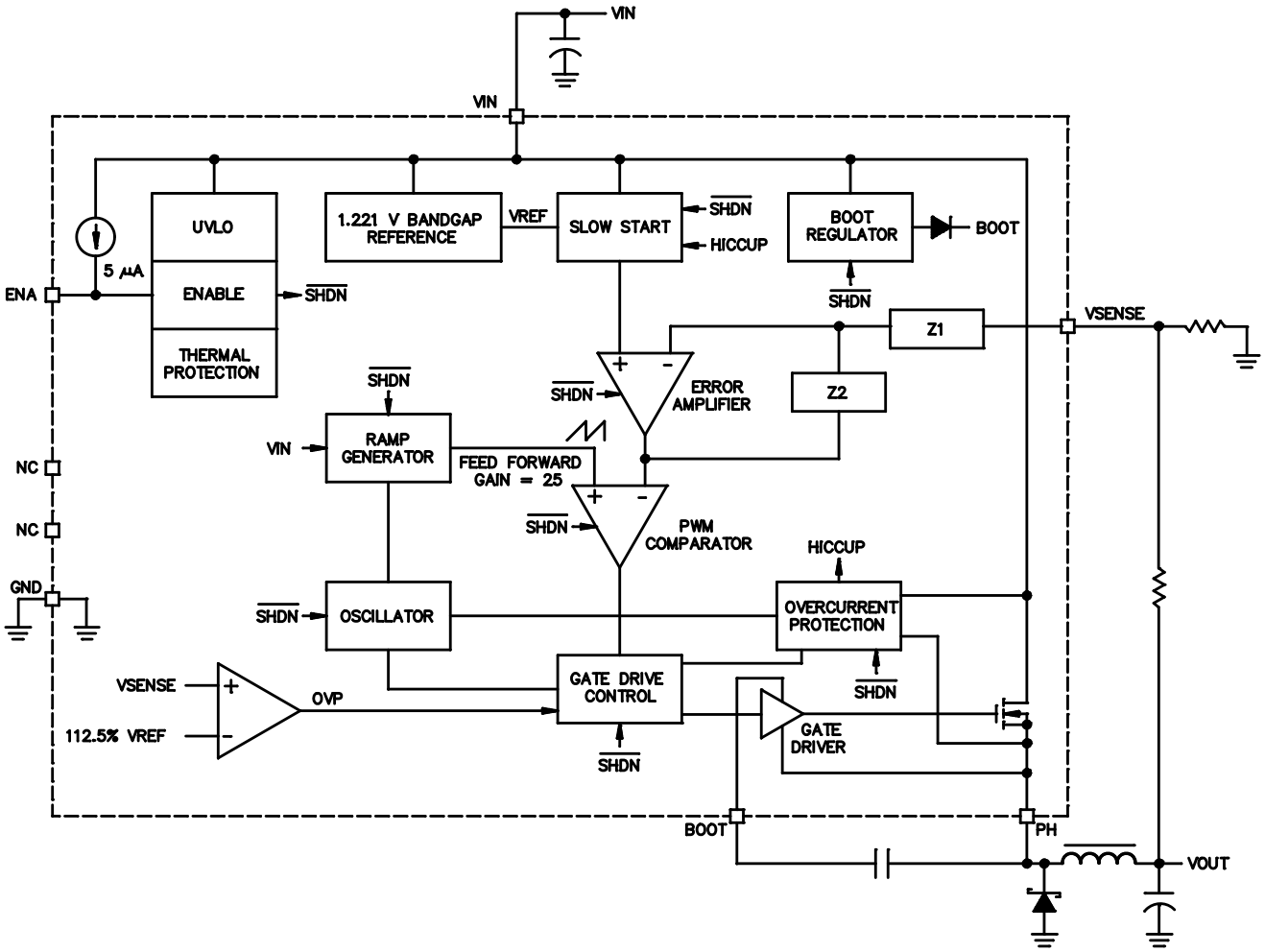

FIGURE 3. Block diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/ 2/	Device manufacturer CAGE code	Input voltage	Output voltage	Device marking	Vendor part number
V62/09645-01XE	01295	5.5 V to 36 V	Adjustable to 1.22 V	5410EP	TPS5410MDREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493