

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Make changes to paragraph 1.2.2. Under figure 1, make changes to the "A", "A1", "c", and "L" dimensions and add note 4. Update document paragraphs to current requirements. - ro	15-08-04	C. SAFFLE
B	Update document paragraphs to current requirements. - ro	21-01-20	J. ESCHMEYER



CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	REV	B	B	B	B	B	B	B	B	B	B	B	B	B						
	PAGE	1	2	3	4	5	6	7	8	9	10	11								

PMIC N/A	PREPARED BY RICK OFFICER	DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990
Original date of drawing YY-MM-DD 09-08-18	CHECKED BY RAJESH PITHADIA	TITLE MICROCIRCUIT, LINEAR, 5 A, HIGH OUTPUT CURRENT PULSE WIDTH MODULATION CONVERTER, MONOLITHIC SILICON
	APPROVED BY CHARLES F. SAFFLE	
	SIZE A	CODE IDENT. NO. 16236
REV	B	PAGE 1 OF 11

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a 5 amp, high output current pulse width modulation converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/09644</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	TPS5450-EP	5 A, high output current pulse width modulation converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	8	MS-012-BA	Plastic surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/09644
		REV B	PAGE 2

1.3 Absolute maximum ratings. 1/ 2/

Input voltage range (VIN):

VIN pin	-0.3 V to 40 V 3/
BOOT pin	-0.3 V to 50 V
PH pin (steady state)	-0.6 V to 40 V 3/
ENA pin	-0.3 V to 7 V
BOOT-PH pin	10 V
VSENSE pin	-0.3 V to 3 V
PH pin (transient < 10 ns)	-1.2 V
Source current (IO) (PH pin)	Internally limited
Leakage current (IILK) (PH pin)	10 μA
Operating virtual junction temperature range	-55°C to +150°C
Storage temperature range	-65°C to +150°C

1.4 Recommended operating conditions. 4/

Input voltage range (VIN)	5.5 V to 36 V
Operating junction temperature range (TJ)	-55°C to +125°C

1.5 Dissipation ratings table. 5/ 6/

Package	Thermal impedance junction to ambient
4 layer board with solder 7/	30°C/W

-
- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
 - 2/ All voltages are within respect to network ground terminal.
 - 3/ Approaching the absolute maximum rating for the VIN pin may cause the voltage on the PH pin to exceed the absolute maximum rating.
 - 4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
 - 5/ Maximum power dissipation may be limited by overcurrent protection.
 - 6/ Power rating at a specific ambient temperature TA should be determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final printed circuit board (PCB) should strive to keep the junction temperature at or below 125°C for performance and long term reliability. See thermal calculations in the application section of the manufacturer’s datasheet for more information.
 - 7/ Test board conditions:
2 inch x 1.85 inch, four layers, 0.062 inch (1.57 mm) thickness. 2 ounce copper traces located on the top and bottom of the PCB. 2 ounce copper ground planes on the two internal layers. Four thermal vias in the thermal pad area under the device package.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/09644
		REV B	PAGE 3

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/09644
		REV B	PAGE 4

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions VIN = 5.5 V to 36 V unless otherwise specified	Temperature, TJ	Device type	Limits		Unit
					Min	Max	
Supply voltage (VIN pin) section							
Quiescent current	IQ	VSENSE = 2 V, not switching, PH pin open	-55°C to +125°C	01		4.4	mA
		Shutdown, ENA = 0 V				60	µA
Undervoltage lockout (UVLO) section							
Start threshold voltage, UVLO	VTH		-55°C to +125°C	01	5.3 typical		V
Hysteresis voltage, UVLO	VHYS		-55°C to +125°C	01	330 typical		mV
Voltage reference section							
Voltage reference accuracy	VRA		25°C	01	1.202	1.239	V
		IO = 0 A to 5 A	-55°C to +125°C		1.193	1.245	
Oscillator section							
Internally set free running frequency	fiSFR		+25°C	01	400	600	kHz
			-55°C to +125°C		375	600	
Minimum controllable on time	tcmín		-55°C to +125°C	01		220	ns
Maximum duty cycle	DCMAX		-55°C to +125°C	01	87		%
Enable (ENA pin) section							
Start threshold voltage, ENA	VSTART		-55°C to +125°C	01		1.3	V
Stop threshold voltage, ENA	VSTOP		-55°C to +125°C	01	0.5		V
Hysteresis voltage, ENA	VHYS		-55°C to +125°C	01	450 typical		mV
Internal slow start time	tISS	(0 ~ 100%)	-55°C to +125°C	01	5.4	10	ms

See footnote at end of table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/09644
		REV B	PAGE 5

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions VIN = 5.5 V to 36 V unless otherwise specified	Temperature, TJ	Device type	Limits		Unit
					Min	Max	
Current limit section							
Current limit	IL		+25°C	01	6.0	9.0	A
			-55°C to +125°C		4.4	11.7	
Current limit hiccup time	tCL		+25°C	01	13	20	ms
			-55°C to +125°C		13	22.5	
Thermal shutdown section							
Thermal shutdown trip point	TTSTP		-55°C to +125°C	01	135		°C
Thermal shutdown hysteresis	TTSH		-55°C to +125°C	01	14 typical		°C
Output MOSFET section							
High side power MOSFET switch	rDS(on)	VIN = 5.5 V	-55°C to +125°C	01	150 typical		mΩ
					110 typical		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/09644
		REV B	PAGE 6

Case X

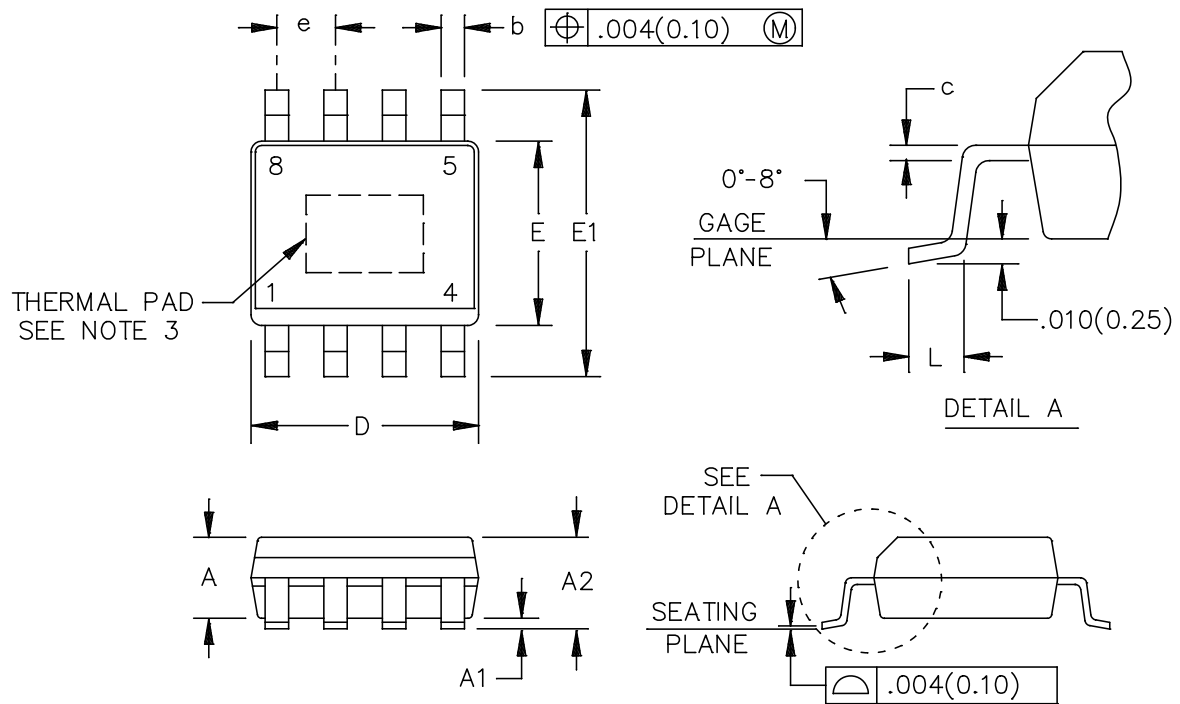


FIGURE 1. Case outline.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/09644</p>
		<p>REV B</p>	<p>PAGE 7</p>

Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.053	0.068	1.35	1.75
A1	0.004	0.009	0.10	0.25
A2	---	0.066	---	1.68
b	0.013	0.019	0.35	0.49
c	.006	.009	0.17	0.25
D	0.188	0.196	4.80	4.98
E	0.149	0.157	3.81	3.99
E1	0.229	0.244	5.84	6.20
e	0.049 BSC		1.27 BSC	
L	0.015	0.050	0.40	1.27
n	8		8	

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.15 mm (0.006 inch).
3. This package is designed to be soldered to a thermal pad on the board. Refer to technical brief, power pad thermally enhanced package, manufacturer's literature number SLMA002 for information regarding recommended board layout. A copy of the manufacturer's datasheet is available from the manufacturer.
4. Falls within reference to JEDEC MS-012-BA.

FIGURE 1. Case outline – continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/09644
		REV B	PAGE 8

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	BOOT	Boost capacitor for the high side field effect transistor (FET) gate driver. Connect 0.01 μ F low equivalent series resistance (ESR) capacitor from BOOT pin to PH pin.
2	NC	Not internal connection.
3	NC	Not internal connection.
4	VSENSE	Feedback voltage for the regulator. Connect to output voltage divider.
5	ENA	On/off control. Below 0.5 V, the device stops switching. Float the pin to enable.
6	GND	Ground. Connect to thermal pad.
7	VIN	Input supply voltage. Bypass VIN pin to GND pin close to device package with a high quality low ESR ceramic capacitor.
8	PH	Source of the high side power metal oxide semiconductor field effect transistor (MOSFET). Connected to external inductor and diode.
9	POWER PAD	GND pin must be connected to the exposed pad for proper operation.

FIGURE 2. Terminal connections.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/09644
		REV B	PAGE 9

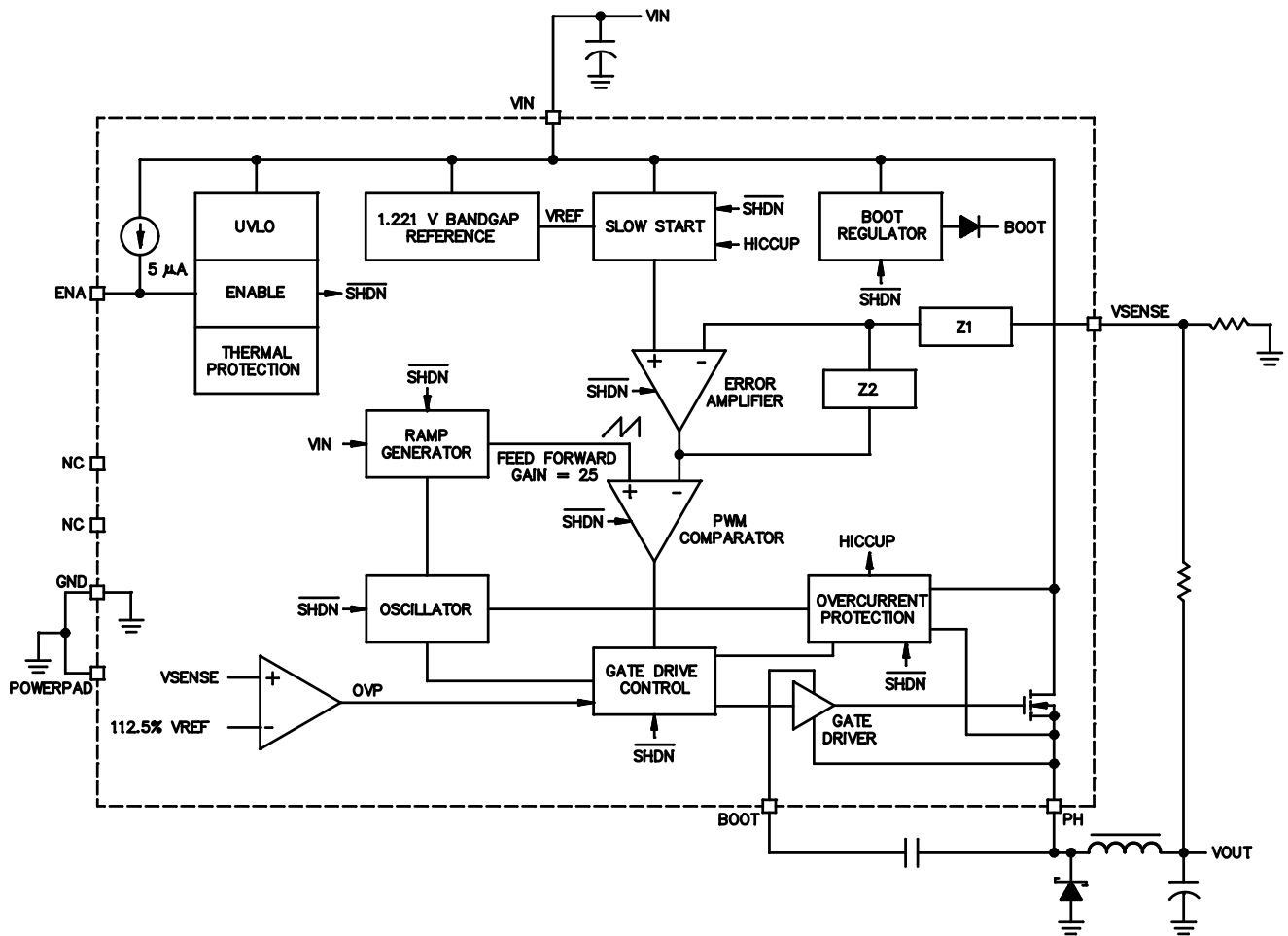


FIGURE 3. Block diagram.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/09644</p>
		<p>REV B</p>	<p>PAGE 10</p>

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/ 2/</u>	Device manufacturer CAGE code	Top side marking	Package <u>3/</u>		Vendor part number
V62/09644-01XE	01295	5450EP	Thermally enhanced	Reel of 2500	TPS5450MDDAREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet.

3/ Package drawings, thermal data, and symbolization are available from the manufacturer.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/09644
		REV B	PAGE 11