REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
PAGE	40	41	42	43	44	45	46	47	48	49												
REV																						
PAGE	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39

REV STATUS OF PAGES	REV																		
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

PMIC N/A	PREPARED BY Phu H. Nguyen	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**
Original date of drawing YY MM DD 10-04-06	CHECKED BY Phu H. Nguyen APPROVED BY Thomas M. Hess	TITLE MICROCIRCUIT, DIGITAL, DIGITAL MEDIA SYSTEM ON CHIP (DMSoC), MONOLITHIC SILICON
	SIZE: A CODE IDENT. NO.: 16236	DWG NO. **V62/09643**
	REV	PAGE 1 OF 49

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance Digital Media System on Chip (DMSoC) microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/09643	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s). 1/

Device type	Generic	Clock Rate	Circuit function
01	SM32DM355-EP	216 MHz	Digital Media System on Chip (DMSoC)

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	Package style
X	337	Plastic ball grid array

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1/ Users are cautioned to review the manufacturers data manual for additional user information relating to this device.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage ranges:
- All 1.3 V supplies ..... -0.5 V to 1.7 V
- All digital 1.8 V supplies ..... -0.5 V to 2.8 V
- All analog 1.8 V supplies ..... -0.5 V to 1.89 V
- All 3.3 V supplies ..... -0.5 V to 4.4 V

Input voltage ranges, (V_I):
- All 1.8 V I/Os ..... -0.5 V to 2.3 V
- All 3.3 V I/Os ..... -0.5 V to 3.8 V
- VBUS ..... 0.0 V to 5.5 V

Clamp current for input or output, (I_{clamp}) ..... -20 mA to +20 mA 4/

Operating case temperature ranges, (T_C):
- Device type: 01 ..... -55°C to +125°C

Storage temperature range, (T_{STG}) ..... -65°C to +150°C

1.4 Recommended operating conditions. 5/

Supply voltage:
- Supply voltage, Core (CV_{DD}) ..... 1.235 V to 1.365 V
- Supply voltage, PLL1 (V_{DDA_PLL1}) ..... 1.235 V to 1.365 V
- Supply voltage, PLL2 (V_{DDA_PLL2}) ..... 1.235 V to 1.365 V
- Supply voltage, USB digital (V_{DDD13_USB}) ..... 1.235 V to 1.365 V
- Supply voltage, USB analog (V_{DDA13_USB}) ..... 1.235 V to 1.365 V
- Supply voltage, USB analog (V_{DDA33_USB}) ..... 3.135 V to 3.465 V
- Supply voltage, USB common PLL ($V_{DDA33_USB_PLL}$) ..... 3.135 V to 3.465 V
- Supply voltage, DDR2/MDDR (V_{DD_DDR}) ..... 1.71 V to 1.89 V
- Supply voltage, DDR DLL Analog (V_{DDA33_DDRDLL}) ..... 3.135 V to 3.465 V
- Supply voltage, Digital video in (V_{DD_VIN}) ..... 3.135 V to 3.465 V
- Supply voltage, Digital video out (V_{DD_VOUT}) ..... 3.135 V to 3.465 V
- Supply voltage, DAC analog (V_{DDA18_DAC}) ..... 1.71 V to 1.89 V
- Supply voltage, I/Os (V_{DD}) ..... 3.135 V to 3.465 V

Supply ground:
- Supply ground, Core, USB digital (V_{SS}) ..... 0 V
- Supply ground, PLL1 (V_{SSA_PLL1}) ..... 0 V
- Supply ground, PLL2 (V_{SSA_PLL2}) ..... 0 V
- Supply ground, USB (V_{SS_USB}) ..... 0 V
- Supply ground, DLL (V_{SSA_DLL}) ..... 0 V
- Supply ground, DAC analog (V_{SSA_DAC}) ..... 0 V
- MXI1 osc ground, (V_{SS_MX1}) ..... 0 V
- MXI2 osc ground, (V_{SS_MX2}) ..... 0 V 6/
- Supply ground, (V_{SS}) ..... 0 V 6/

2/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3/ All voltage values are with respect to V_{SS}.

4/ Clamp current flows from an input or putput pad to a supply rail through a clamp circuit or an intrinsic diode. Positive current results from an applied input or output voltage that is more than 0.5 V higher (more positive) than the supply voltage, $V_{DD}/V_{DDA_PLL1/2}/V_{DD_USB}/V_{DD_DDR}$ for dual supply macros. Negative results from an applied voltage that is more than 0.5 V less (more negative) than the V_{SS} voltage.

5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

6/ Oscillator ground must be kept separate from other grounds and connected directly to the crystal load capacitor ground (see manufacturer data for more details).

1.4 Recommended operating conditions - Continued.

Minimum high level input voltage, (V_{IH}) ..... 2.0 V 7/
Maximum low level input voltage, (V_{IL}) ..... 0.8 V 7/
DAC: 8/
DAC reference voltage, (V_{REF}) ..... 450 TYP mV
DAC full scale current adjust resistor, (R_{BIAS}) ..... 2550 TYP Ω
Output resistor, (R_{LOAD}) ..... 499 TYP Ω
Bypass capacitor, (C_{BG}) ..... 0.1 TYP µF
Video buffer 8/
Output resistor (ROUT), between TVOUT and VFB pins (R_{OUT}) ..... 1070 TYP Ω
Feed back resistor, between VFB and IOUT pins, (R_{FB}) ..... 1000 TYP Ω
DAC full scale current adjust resistor, (R_{BIAS}) ..... 2550 TYP Ω
Bypass capacitor, (C_{BG}) ..... 0.1 µF
USB:
USB external charge pump input (USB_VBUS) ..... 4.85 V to 5.25 V
USB reference resistor, (R1) ..... 9.9 kΩ to 10.1 kΩ 9/
Operating case temperature (T_C): 10/
Device type 01 ..... -55°C to +125°C
Thermal resistance characteristics for case outline X

		°C/W 11/
Junction to case	$R\theta_{JC}$	7.2
Junction to board	$R\theta_{JB}$	11.4
Junction to free air	$R\theta_{JA}$	27.0
Junction to package top	PsiJT	0.1
Junction to board	PsiJB	11.3

2. APPLICABLE DOCUMENTS

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
EIA/JESD51-2 – Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still air).
EIA/JESD51-3 – Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.
EIA/JESD51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org)

7/ These I/O specifications apply to regular 3.3 V I/Os and do not apply to DDR2/mDDR, USB I/Os are 1.8 V I/Os and adhere to USB2.0 spec.
8/ See manufacturer data for more information. Also, resistors should be E-96 spec line (3 digits with 1% accuracy).
9/ Connect USB_R1 to VSS_USB_REF via 10 KΩ, 1% resistor placed as close to the device as possible.
10/ To avoid frequency performance device degradation, limit the total device power on hours to less than 16500 hrs at T_C = 125°C.
11/ The junction to case measurement was conducted in a JDEC defined 2S2P system and will change based on environment as well as application. For more information, see three EIA/JEDEC standards: EIA/JEDEC standards: 51-2, 51-3, 51-7.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as specified in figure 3.

3.5.4 Test load circuit for AC timing measurement. The test load circuit for AC timing measurements shall be as specified in figure 4.

3.5.5 Timing waveforms. The timing waveforms shall be as shown in figures 4-48.

TABLE I. Electrical performance characteristics. 1/

Test		Symbol	Test condition 2/ Device type: All	Limits Min	Limits Max	Unit
Voltage output	High level output voltage 3/	V_{OH}	DV_{DD} = MIN, I_{OH} = MAX	2.4		V
	Low level output voltage 3/	V_{OL}	DV_{DD} = MIN, I_{OL} = MAX		0.6	
Current Input/Output	Input current for I/O without internal pull-up/pull-down	I_I	$V_I = V_{SS}$ to V_{DD}	-1	1	µA
	Input current for I/O with internal pull-up 4/ 5/	$I_{I(pullup)}$	$V_I = V_{SS}$ to V_{DD}	40	190	
	Input current for I/O with internal pull-down 4/ 5/	$I_{I(pulldown)}$	$V_I = V_{SS}$ to V_{DD}	-190	-40	
	High level output current	I_{OH}			-100	
	Low level output current	I_{OL}			4000	
	I/O off state output current	I_{OZ}	$V_O = V_{DD}$ or V_{SS}, Internal pull disabled	±10 TYP		
Capacitance	Input capacitance	C_I			4	pF
	Output capacitance	C_O			4	
DAC	Resolution	Resolution		10 TYP		Bits
	Integral non-linearity, best fit	INL	R_{LOAD} = 499 Ω, Video buffer disabled	1 TYP		LSB
	Differential non-linearity	DNL		0.5 TYP		
	Output compliance range	Compliance	R_{LOAD} = 499 Ω, IFS = 1.4 mA	0	0.700	V
Video buffer	Output high voltage (top of 75% NTSC or PAL colorbar) 6/	$V_{OH(VIDBUF)}$		1.55 TYP		V
	Output low voltage (bottom of sync tip)	$V_{OL(VIDBUF)}$		0.470 TYP		

RESET

Timing requirements for Reset 7/ 8/ (See figure 5)

No	Test	Symbol	Test condition 2/ Device type: All	Limits Min	Limits Max	Unit
1	Active low width of the $\overline{RESET}$ pulse	$t_{w(RESET)}$		12C		ns
2	Setup time, boot configuration pins valid before $\overline{RESET}$ rising edge	$t_{su(BOOT)}$		12C		
3	Hold time, boot configuration pins valid after $\overline{RESET}$ rising edge	$t_{h(BOOT)}$		12C		

OSCILLATORS AND CLOCKS

Switching characteristics for 24 MHz system

	Start up time (from power up until oscillating at stable frequency)				4	ms
	Oscillation frequency			24 or 36 TYP		MHz
	ESR	24 MHz			60	Ω
		36 MHz			30	
	Frequency stability				±50	ppm

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/ Device type: All	Limits Min	Limits Max	Unit
	OSCILLATORS AND CLOCKS - Continued					
Switching characteristics for 27 MHz system						
	Start up time (from power up until oscillating at stable frequency)				4	ms
	Oscillation frequency			27 TYP		MHz
	ESR				50	Ω
	Frequency stability				±50	ppm
	CLOCK PLL ELECTRICAL DATA/TIMING (Input and output clocks)					
Timing requirements for MXI1/CLKIN1 9/ 10/						
1	Cycle time, MXI1/CLKIN1	$t_{c(MXI1)}$	See figure 6	27.7 11/	41.6 11/	ns
2	Pulse duration, MXI1/CLKIN1 high	$t_{w(MXI1H)}$		0.45C	0.55C	
3	Pulse duration, MXI1/CLKIN1 low	$t_{w(MXI1L)}$		0.45C	0.55C	
4	Transition time, MXI1/CLKIN1	$t_{t(MXI1)}$			0.05C	
5	Period jitter, MXI1/CLKIN1	$t_{J(MXI1)}$			0.02C	
Timing requirements for MXI2/CLKIN2 9/ 12/						
1	Cycle time, MXI2/CLKIN2	$t_{c(MXI2)}$	See figure 7	37.037 13/	37.037 13/	ns
2	Pulse duration, MXI2/CLKIN2 high	$t_{w(MXI2H)}$		0.45C	0.55C	
3	Pulse duration, MXI2/CLKIN2 low	$t_{w(MXI2L)}$		0.45C	0.55C	
4	Transition time, MXI2/CLKIN2	$t_{t(MXI2)}$			0.05C	
5	Period jitter, MXI2/CLKIN2	$t_{J(MXI2)}$			0.02C	
Switching characteristics for CLKOUT1 9/ 14/						
1	Cycle time CLKOUT1	$t_{c(CLKOUT1)}$	See figure 8	$t_{c(MXI1)}$		ns
2	Pulse duration, CLKOUT1 high	$t_{w(CLKOUT1H)}$		0.45P	0.55P	
3	Pulse duration, C:LKOUT1 low	$t_{w(CLKOUT1L)}$		0.45P	0.55P	
4	Transition time, CLKOUT1	$t_{t(CLKOUT1)}$			0.55P	
5	Delay time, MXI1/CLKIN1 high to CLKOUT1 high	$t_{d(MXI1H-CLKOUT1H)}$		1	8	
6	Delay time, MXI1/CLKIN1 low to CLKOUT1 low	$t_{d(MXI1L-CLKOUT1L)}$		1	8	
Switching characteristics for CLKOUT2 9/ 15/						
1	Cycle time CLKOUT2	$t_{c(CLKOUT2)}$	See figure 9	$t_{c(MXI1)}/3$		ns
2	Pulse duration, CLKOUT2 high	$t_{w(CLKOUT2H)}$		0.45P	0.55P	
3	Pulse duration, C:LKOUT2 low	$t_{w(CLKOUT2L)}$		0.45P	0.55P	
4	Transition time, CLKOUT2	$t_{t(CLKOUT2)}$			0.05P	
5	Delay time, MXI1/CLKIN1 high to CLKOUT2 high	$t_{d(MXI1H-CLKOUT2H)}$		1	8	
6	Delay time, MXI1/CLKIN1 low to CLKOUT2 low	$t_{d(MXI1L-CLKOUT2L)}$		1	8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/ Device type: All	Limits Min	Limits Max	Unit
	CLOCK PLL ELECTRICAL DATA/TIMING (Input and output clocks) - Continued					
Switching characteristics for CLKOUT3 9/ 16/						
1	Cycle time CLKOUT3	$t_{c(CLKOUT3)}$	See figure 10	$t_{c(MXI1)}/8$		ns
2	Pulse duration, CLKOUT3 high	$t_{w(CLKOUT3H)}$		0.45P	0.55P	
3	Pulse duration, C:LKOUT3 low	$t_{w(CLKOUT3L)}$		0.45P	0.55P	
4	Transition time, CLKOUT3	$t_{t(CLKOUT3)}$			0.05P	
5	Delay time, CLKIN/MXI high to CLKOUT3 high	$t_{d(MXI2H-CLKOUT3H)}$		1	8	
6	Delay time, CLKIN/MXI low to CLKOUT3 low	$t_{d(MXI2L-CLKOUT3L)}$		1	8	
	GPIO PERIPHERAL INPUT/OUTPUT ELECTRICAL DATA/TIMING					
Timing requirements for GPIO inputs						
1	Pulse duration, GPIx high	$t_{w(GPIH)}$	See figure 10	52		ns
2	Pulse duration, GPIx high	$t_{w(GPIL)}$		52		
Switching characteristics for GPIO outputs						
3	Pulse duration, GPOx high	$t_{w(GPOH)}$	See figure 11	26 17/		ns
4	Pulse duration, GPOx low	$t_{w(GPOL)}$		26 17/		
	GPIO PERIPHERAL EXTERNAL INTERRUPTS ELECTRICAL DATA/TIMING					
Timing requirements for external interrupts/EDMA events 18/						
1	Width of the external interrupt pulse low	$t_{w(ILOW)}$	See figure 12	52		ns
2	Width of the external interrupt pulse high	$t_{w(IHIGH)}$		52		
	AEMIF ELECTRICAL DATA/TIMING					
Timing requirements for Asynchronous Memory Cycles for AEMIF module 19/ See figure 13 and 14						
READS and WRITES						
2	Pulse duration, EM_WAIT assertion and deassertion	$t_{w(EM_WAIT)}$		2E		ns
READS						
12	Setup time, EM_D[15:0] valid before $\overline{EM_OE}$ high	$t_{su(EMDV-EMOEH)}$		5		ns
13	Hold time, EM_D[15:0] valid after $\overline{EM_OE}$ high	$t_{h(EMOEH-EMDIV)}$		0		
14	Setup time EM_WAIT asserted before $\overline{EM_OE}$ high 20/	$t_{su(EMOEL-EMWAIT)}$		4E TYP		
READS (OneNAND Synchrnous Burst Read)						
30	Setup time, EM_D[15:0] valid before $\overline{EM_CLK}$ high	$t_{su(EMDV-EMCLKH)}$		4		ns
31	Hold time, EM_D[15:0] valid after $\overline{EM_CLK}$ high	$t_{h(EMCLKH-EMDIV)}$		4		
WRITES						
28	Setup time, EM_WAIT asserted before valid before $\overline{EM_WE}$ high	$t_{su(EMWEL-EMWAIT)}$		4E TYP		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/ Device type: All	Limits			Unit
				Min	TYPICAL	Max	
	AEMIF ELECTRICAL DATA/TIMING – Continued						
	Switching characteristics for Asynchrnous Memory Cycles for AEMIF module 19/ 21/ 22/ See figure 13 and 14						
	READS and WRITES						
1	Turn around time	$t_{d(TURNAROUND)}$			(TA)*E		ns
	READS						
3	EMIF read cycle time (EW = 0)	$t_{c(EMRCYCLE)}$			(RS+RST+RH)*E		ns
	EMIF read cycle time (EW = 1)				(RS+RST+RH+(EWC*16))*E		
4	Output setup time, $\overline{EM_CE[1:0]}$ low to $\overline{EM_OE}$ low (SS = 0)	$t_{su(EMCEL-EMOEL)}$			(RS)*E		
	Output setup time, $\overline{EM_CE[1:0]}$ low to $\overline{EM_OE}$ low (SS = 1)				0		
5	Output hold time, $\overline{EM_OE}$ high to $\overline{EM_CE[1:0]}$ high (SS = 0)	$t_{h(EMOEH-EMCEH)}$			(RH)*E		
	Output hold time, $\overline{EM_OE}$ high to $\overline{EM_CE[1:0]}$ high (SS = 1)				0		
6	Output setup time, $\overline{EM_BA[1:0]}$ valid to $\overline{EM_OE}$ low	$t_{su(EMBAV-EMOEL)}$			(RS)*E		
7	Output hold time, $\overline{EM_OE}$ high to $\overline{EM_BA[1:0]}$ invalid	$t_{h(EMOEH-EMBAIV)}$			(RH)*E		
8	Output setup time, $\overline{EM_A[13:0]}$ valid to $\overline{EM_OE}$ low	$t_{h(EMOEH-EMBAIV)}$			(RS)*E		
9	Output hold time, $\overline{EM_OE}$ high to $\overline{EM_A[13:0]}$ invalid	$t_{su(EMBAV-EMOEL)}$			(RH)*E		
10	$\overline{EM_OE}$ active low width (EW = 0)	$t_{h(EMOEL)}$			(RST)*E		
	$\overline{EM_OE}$ active low width (EW = 1)				(RST+(EWC*16))*E		
11	Delay time from EM_WAIT deasserted to $\overline{EM_OE}$ high	$t_{d(EMWAITH-EMOEH)}$			4E		
	READS(OneNAND Synchronous Burst Read)						
32	Frequency, EM_CLK	$f_{c(EMWCYCLE)}$		1		66	MHz
33	Cycle time, EM_CLK	$t_{c(EM_CLK)}$		15		1000	ns
34	Output setup time, EM_ADV valid before EM_CLK high	$t_{su(EM_ADVV-EM_CLKH)}$		5			
35	Output hold time, EM_CLK high to EM_ADV invalid	$t_{h(EM_CLKH-EM_ADVIV)}$		6			
36	Output setup time, EM_A[13:0]/EM_BA[1] valid before EM_CLK high	$t_{su(EM_AV-EM_CLKH)}$		5			
37	Output hold time, EM_CLK high to EM_A[13:0]/EM_BA[1] invalid	$t_{h(EM_CLKH-EM_AIV)}$		6			
38	Pulse duration, EM_CLK high	$t_{w(EM_CLKH)}$		23/			
39	Pulse duration, EM_CLK low	$t_{w(EM_CLKL)}$		23/			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/ Device type: All	Limits			Unit
				Min	TYPICAL	Max	
	AEMIF ELECTRICAL DATA/TIMING – Continued						
	Switching characteristics for Asynchrnous Memory Cycles for AEMIF module 19/ 21/ 22/ See figure 13 and 14						
	WRITES						
15	EMIF write cycle time (EW = 0)	$t_{c(EMWCYCLE)}$			(WS+WST+WH)*E		ns
	EMIF write cycle time (EW = 1)				(WS+WST+WH+(EWC*16))*E		
16	Output setup time, $\overline{EM_CE[1:0]}$ low to $\overline{EM_WE}$ low (SS = 0)	$t_{su(EMCEL-EMWEL)}$			(WS)*E		
	Output setup time, $\overline{EM_CE[1:0]}$ low to $\overline{EM_WE}$ low (SS = 1)				0		
17	Output hold time, $\overline{EM_WE}$ high to $\overline{EM_CE[1:0]}$ high (SS = 0)	$t_{h(EMWEH-EMCEH)}$			(WH)*E		
	Output hold time, $\overline{EM_WE}$ high to $\overline{EM_CE[1:0]}$ high (SS = 1)				0		
20	Output setup time, $\overline{EM_BA[1:0]}$ valid to $\overline{EM_WE}$ low	$t_{su(EMBAV-EMWEL)}$			(WS)*E		
21	Output hold time, $\overline{EM_WE}$ high to $\overline{EM_BA[1:0]}$ invalid	$t_{h(EMWEH-EMBAIV)}$			(WH)*E		
22	Output setup time, $\overline{EM_A[13:0]}$ valid to $\overline{EM_WE}$ low	$t_{h(EMWEH-EMBAIV)}$			(WS)*E		
23	Output hold time, $\overline{EM_WE}$ high to $\overline{EM_A[13:0]}$ invalid	$t_{su(EMBAV-EMWEL)}$			(WH)*E		
24	$\overline{EM_WE}$ active low width (EW = 0)	$t_{h(EMWEL)}$			(WST)*E		
	$\overline{EM_WE}$ active low width (EW = 1)				(WST+(EWC*16))*E		
25	Delay time from EM_WAIT deasserted to $\overline{EM_WE}$ high	$t_{d(EMWAITH-EMWEH)}$			4E		
26	Output setup time, $\overline{EM_D[15:0]}$ valid to $\overline{EM_WE}$ low	$t_{su(EMDV-EMWEL)}$			(WS)*E		
27	Output hold time, $\overline{EM_WE}$ high to $\overline{EM_D[15:0]}$ invalid	$t_{h(EMWEH-EMDIV)}$			(WH)*E		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test		Symbol	Test condition 2/ Device type: All	Limits				Unit
				Fast mode		Standard mode		
				Min	Max	Min	Max	
MMC/SD ELECTRICAL DATA/TIMING								
Timing requirements for MMC/SD module (See figure 19 and 21)								
1	Setup time, SD_CMD valid before SD_CLK high	$t_{su(CMDV-CLKH)}$		6		5		ns
2	Hold time, SD_CMD valid after SD_CLK high	$t_{h(CLKH-CMDV)}$		2.5 24/		5		
3	Setup time, SD_DATx valid before SD_CLK high	$t_{su(DATV-CLKH)}$		6		5		
4	Hold time, SD_DATx valid after SD_CLK high	$t_{h(CLKH-DATV)}$		2.5		5		
Switching characteristics for MMC/SD module (See figure 18 - 21)								
7	Operating frequency, SD_CLK	$f_{(CLK)}$		0	50	0	25	ns
8	Identification mode frequency, SD_CLK	$f_{(CLK\ ID)}$		0	400	0	400	
9	Pulse width, SD_CLK low	$t_{w(CLKL)}$		7		10		
10	Pulse width, SD_CLK high	$t_{w(CLKH)}$		7		10		
11	Rise time, SD_CLK	$t_{r(CLK)}$			3		10	
12	Fall time, SD_CLK	$t_{f(CLK)}$			3		10	
13	Delay time, SD_CLK low to SD_CMD transition	$t_{d(CLKL-CMD)}$		-7.5	4	-7.5	14	
14	Delay time, SD_CLK low to SD_DATx transition	$t_{d(CLKL-DAT)}$		-7.5	4	-7.5	14	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/ Device type: All	Limits Min	Limits Max	Unit
	VPFE LECTRICAL DATA/TIMING					
Timing requiremenets for VPFE PCLK Master/Slave mode 25/ (See figure 22)						
1	Cycle time, PCLK	$t_{c(PCLK)}$	H3A not used	13.33 or P 26/	100	ns
			H3A used	2P + 1	100	
2	Pulse duration, PCLK high	$t_{w(PCLKH)}$		5.7		
3	Pulse duration, PCLK low	$t_{w(PCLKL)}$		5.7		
4	Transition time, UXCLK	$t_{t(PCLK)}$			3	
Timing requirements for VPFE(CCD) Slave mode (See figure 23)						
5	Setup time, CCD valid before PCLK edge	$t_{su(CCDV-PCLK)}$		3		ns
6	Hold time, CCD valid after PCLK edge	$t_{h(PCLK-CCDV)}$		2		
7	Setup time, HD valid before PCLK edge	$t_{su(HDV-PCLK)}$		3		
8	Hold time, HD valid after PCLK edge	$t_{h(PCLK-HDV)}$		2		
9	Setup time, VD valid before PCLK edge	$t_{su(VDV-PCLK)}$		3		
10	Hold time, VD valid after PCLK edge	$t_{h(PCLK-VDV)}$		2		
11	Setup time, CAM_WEN_FIELD valid before PCLK edge	$t_{su(CAM_WEN_FILELDV-PCLK)}$		3		
12	Hold time, CAM_WEN_FIELD valid after PCLK edge	$t_{h(PCLK-CAM_WEN_FIELDV)}$		2		
Timing requirements for VPFE(CCD) Master mode 27/ **(**See figure 24)						
15	Setup time, CCD valid before PCLK edge	$t_{su(CCDV-PCLK)}$		3		ns
16	Hold time, CCD valid after PCLK edge	$t_{h(PCLK-CCDV)}$		2		
23	Setup time, CAM_WEN_FIELD valid before PCLK edge	$t_{su(CAM_WEN_FILELDV-PCLK)}$		3		
24	Hold time, CAM_WEN_FIELD valid after PCLK edge	$t_{h(PCLK-CAM_WEN_FIELDV)}$		2		
Switching characteristics for VPFE(CCD) Master mode (See figure 25)						
18	Delay time, PCLK edge to HD invalid	$t_{d(PCLKL-HDIV)}$		3	11	ns
20	Delay time, PCLK edge to VD invalid	$t_{d(PCLKL-VDIV)}$		3	11	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/ Device type: All	Limits		Unit
				Min	Max	
	VPBE ELECTRICAL DATA/TIMING					
Timing requirements for VPBE CLK inputs						
1	Cycle time, PCLK 28/	$t_{c(PCLK)}$	See figure 26	13.33	160	ns
2	Pulse duration, PCLK high	$t_{w(PCLKH)}$		5.7		
3	Pulse duration, PCLK low	$t_{w(PCLKL)}$		5.7		
4	Transition time, PCLK	$t_{t(PCLK)}$			3	
5	Cycle time, EXTCLK	$t_{c(EXTCLK)}$		13.33	160	
6	Pulse duration, EXTCLK high	$t_{w(EXTCLKH)}$		5.7		
7	Pulse duration, EXTCLK low	$t_{w(EXTCLKL)}$		5.7		
8	Transition time, EXTCLK	$t_{t(EXTCLK)}$			3	
Timing requirements for VPBE control input with respect to PCLK and EXTCLK 27/ 29/ 30/						
9	Setup time, VCTL valid before VCLKIN edge	$t_{su(VCTLV-VCLKIN)}$	See figure 27	2		ns
10	Hold time, VCTL valid after VCLKIN edge	$t_{h(VCLKIN-VCTLV)}$		1		
Switching characteristics for VPBE control and data output with respect to PCLK and EXTCLK						
11	Delay time, VCLKIN edge to VCTL valid	$t_{d(VCLKIN-VCTLV)}$	See figure 28		13.3	ns
12	Delay time, VCLKIN edge to VCTL invalid	$t_{d(VCLKIN-VCTLIV)}$		2		
13	Delay time, VCLKIN edge to VDATA valid	$t_{d(VCLKIN-VDATAV)}$			13.3	
14	Delay time, VCLKIN edge to VDATA invalid	$t_{d(VCLKIN-VDATAIV)}$		2		
Switching characteristics for VPBE control and data output with respect to VCLK 27/ 32/						
17	Cycle time, VCLK	$t_{c(VCLK)}$	See figure 29	13.33	160	ns
18	Pulse duration, VCLK high	$t_{w(VCLKH)}$		5.7		
19	Pulse duration, PCLK low	$t_{w(VCLKL)}$		5.7		
20	Transition time, VCLK	$t_{t(VCLK)}$			3	
21	Delay time, VCLKIN high to VCLK high	$t_{d(VCLKINH-VCLKH)}$		2	12	
22	Delay time, VCLKIN low to VCLK low	$t_{d(VCLKINL-VCLKL)}$		2	12	
23	Delay time, VCLK edge to VCTL valid	$t_{d(VCLK-VCTLV)}$			4	
24	Delay time, VCLK edge to VCTL invalid	$t_{d(VCLK-VCTLIV)}$		0		
25	Delay time, VCLK edge to VDATA valid	$t_{d(VCLK-VDATAV)}$			4	
26	Delay time, VCLK edge to VDATA invalid	$t_{d(VCLK-VDATAIV)}$		0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No	Test	Symbol	Test condition 2/ Device type: All	Limits						Unit
				Low speed 1.5 Mbps		Full speed 12 Mbps		High speed 33/ 480 Mbps		
				Min	Max	Min	Max	Min	Max	
USB2.0 ELECTRICAL DATA/TIMING										
Switching chrasteristics for USB2.0										
1	Rise time, USB_DP and USB_DM signals 34/	$t_{r(D)}$	See figure 30	75	300	4	20	0.5		ns
2	Fall time, USB_DP and USB_DM signals 34/	$t_{f(D)}$		75	300	4	20	0.5		ns
3	Rise/Fall time, matching 35/	t_{frfm}		80	125	90	111.11			%
4	output signal cross over voltage 34/	V_{CRS}		1.3	2	1.3	2			V
5	Source (Host) driver jitter, next transaction	$t_{jr(source)NT}$			2		2			ns
	Function driver jitter, next transaction	$t_{jr(FUNC)NT}$			25		2			
6	Source (Host) driver jitter, paired transaction 36/	$t_{jr(source)PT}$			1		1			
	Function driver jitter, next transaction	$t_{jr(FUNC)PT}$			10		1			
7	Pulse duration, EOP transmitter	$t_{w(EOPT)}$		1250	1500	160	175			
8	Pulse duration, EOP receiver	$t_{w(EOPR)}$		670		82				
9	Data rate	$t_{(DRATE)}$			1.5		12		480	Mb/s
10	driver output resistance	Z_{DRV}				28	49.5	40.5	49.5	Ω

No	Test	Symbol	Test condition 2/ Device type: All	Limits		Unit
				Min	Max	
UART ELECTRICAL DATA/TIMING						
Timing requirements for UARTx receiver						
4	Pulse duration, receive data bit (RXDn)	$t_{w(URXDB)}$	See figure 31	0.99U 37/	1.05U 37/	ns
5	Pulse duration, receive start bit	$t_{w(URXSB)}$		0.99U 37/	1.05U 37/	
Switching characteristic for UARTx transmit						
1	UART0/1 maximun programmable baud rate	$f_{(baud)}$	See figure 31		1.5	MHz
	UART2 maximum programmable baud rate				5	
2	Pulse duration, transmit data bit (TXDn)	$t_{w(UTXDB)}$		U-2 37/	U+2 37/	ns
3	Pulse duration, transmit start bit	$t_{w(UTXSB)}$		U-2 37/	U+2 37/	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

	Test	Symbol	Test condition 2/ Device type: All	Limits Min	Limits Max	Unit
	SPI ELECTRICAL DATA/TIMING					
Timing requirements for SPI (All modes)						
1	Cycle time, SPI_CLK	$t_{c(CLK)}$	See figure 32	37.037		ns
2	Pulse duration, SPI_CLK high (All master Modes)	$t_{w(CLKH)}$		0.45*T	0.55*T	
3	Pulse duration, SPI_CLK low (All master Modes)	$t_{w(CLKL)}$		0.45*T	0.55*T	
Timing requirements for SPI master mode [Clock phase = 0] 39/ See figure 33						
4	Setup time, SPI_DI (input) valid before SPI_CLK (output) falling edge	$t_{su(DIV_CLKL)}$	Clock polarity = 0	.5P+3		ns
5	Setup time, SPI_DI (input) valid before SPI_CLK (output) rising edge	$t_{su(DIV_CLKH)}$	Clock polarity = 1	.5P+3		
6	Hold time, SPI_DI (input) valid after SPI_CLK (output) falling edge	$t_{h(CLKL-DIV)}$	Clock polarity = 0	.5P+3		
7	Setup time, SPI_DI (input) valid after SPI_CLK (output) rising edge	$t_{h(CLKH-DIV)}$	Clock polarity = 1	2.5P+3		
Switching characteristics for SPI master mode [Clock phase = 0] See figure 33						
8	Delay time, SPI_CLK (output) rising edge to SPI_DO (output) transition	$t_{d(CLKH_DOV)}$	Clock polarity = 0	-4	5	ns
9	Delay time, SPI_CLK (output) falling edge to SPI_DO (output) transition	$t_{d(CLKL_DOV)}$	Clock polarity = 1	-4	5	
10	Delay time, SPI_EN[1:0] (output) falling edge to first SPI_CLK (output) rising or falling edge	$t_{d(ENL_CLKH/L)}$		2P 40/	40/	
11	Delay time, SPI_CLK (output) rising or falling edge e to SPI_EN[1:0] (output) rising edge	$t_{d(CLKH/L-ENH)}$		P+.5C 41/	41/	
Timing requirements for SPI master mode [Clock phase = 1] 39/ See figure 34						
13	Setup time, SPI_DI (input) valid before SPI_CLK (output) riing edge	$t_{su(DIV_CLKL)}$	Clock polarity = 0	.5P+3		ns
14	Setup time, SPI_DI (input) valid before SPI_CLK (output) falling edge	$t_{su(DIV_CLKH)}$	Clock polarity = 1	.5P+3		
15	Hold time, SPI_DI (input) valid after SPI_CLK (output) rising edge	$t_{h(CLKL-DIV)}$	Clock polarity = 0	.5P+3		
16	Setup time, SPI_DI (input) valid after SPI_CLK (output) falling edge	$t_{h(CLKH-DIV)}$	Clock polarity = 1	.5P+3		
Switching characteristics for SPI master mode [Clock phase = 1] See figure 34						
17	Delay time, SPI_CLK (output) falling edge to SPI_DO (output) transition	$t_{d(CLKH_DOV)}$	Clock polarity = 0	-4	5	ns
18	Delay time, SPI_CLK (output) rising edge to SPI_DO (output) transition	$t_{d(CLKL_DOV)}$	Clock polarity = 1	-4	5	
19	Delay time, SPI_EN[1:0] (output) falling edge to first SPI_CLK (output) rising or falling edge	$t_{d(ENL_CLKH/L)}$		2P 40/	40/	
20	Delay time, SPI_CLK (output) rising or falling edge to SPI_DO (output) high impedance	$t_{d(CLKH/L-DOHz)}$		P+.5C 41/	41/	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

	Test	Symbol	Test condition 2/ Device type: All	Limits				Unit
				Standard mode		Fast mode		
				Min	Max	Min	Max	
	I2C ELECTRICAL DATA/TIMING							
Timing requirements for I2C timings								
1	Cycle time, SCL	$t_{c(SCL)}$	See figure 35	10		2.5		µs
2	Setup time, SCL high before SDA low (for a repeated START condition)	$t_{su(SCLH-SDAL)}$		4.7		0.6		
3	Hold time, SCL low after SDA low (for a START and a repeated START condition)	$t_{h(SCLL-SDAL)}$		4		0.6		
4	Pulse duration, SCL low	$t_{w(SCLL)}$		4.7		1.3		
5	Pulse duration, SCL high	$t_{w(SCLH)}$		4		0.6		
6	Setup time, SDA valid before SCL high	$t_{su(SDAV-SCLH)}$		250		100 43/		ns
7	Hold time, SDA valid after SCL low (For I2C bus device)	$t_{h(SDA-SCLL)}$		0 44/		0 44/	0.9 45/	µs
8	Pulse duration, SDA high between STOP and Start conditions	$t_{w(SDAH)}$		4.7		1.3		µs
9	Rise time, SDA	$t_{r(SDA)}$			1000	46/ 47/	300	ns
10	Rise time, SCL	$t_{r(SCL)}$			1000	46/ 47/	300	
11	Fall time, SDA	$t_{f(SDA)}$			300	46/ 47/	300	
12	Fall time, SCL	$t_{f(SCL)}$			300	46/ 47/	300	
13	Setup time, SCL high before SDA high (for STOP condition)	$t_{su(SCLH-SDAH)}$		4		0.6		µs
14	Pulse duration, spike (must be suppressed)	$t_{w(SP)}$				0	50	ns
15	Capacitive load for each bus line	C_b 47/			400		400	pF
Switching characteristics for I2C timings 47/								
16	Cycle time, SCL	$t_{c(SCL)}$	See figure 36	10		2.5		µs
17	Delay time, SCL high to SDA low (for a repeated START condition)	$t_{d(SCLH-SDAL)}$		4.7		0.6		
18	Delay time, SDA low to SCL low (for a START and a repeated START condition)	$t_{d(SDAL-SCLL)}$		4		0.6		
19	Pulse duration, SCL low	$t_{w(SCLL)}$		4.7		1.3		
20	Pulse duration, SCL high	$t_{w(SCLH)}$		4		0.6		
21	Dealy time, SDA valid to SCL high	$t_{d(SDAV-SCLH)}$		250		100		
22	Valid time, SDA valid after SCL low (For I2C devices)	$t_{v(SCLL-SDAV)}$		0		0	0.9	
23	Pulse duration, SDA high between STOP and START conditions	$t_{w(SDAH)}$		4.7		1.3		
28	Delay time, SCL high to SDA high (for STOP condition)	$t_{d(SCLH-SDAH)}$		4		0.6		
29	Capacitance for each I2C pin	C_p			10		10	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test condition 2/ Device types: All		Limits Min	Limits Max	Unit
	ASP ELECTRICAL DATA/TIMING						
Timing requirements for ASP 44/ See figure 37							
15	Cycle time, CLKR/X	$t_{c(CKRX)}$		CLK ext	38.5 or 2P 49/ 50/		ns
16	Pulse duration, CLKR/X high or CLKR/X low	$OTG_{(CLKS)}$		CLKS ext	19.25 or P 49/ 50/ 51/		
5	Setup time, external FSR high before CLKR low	$t_{su(FRH-CKRL)}$		CLKR int	21		
				CLKR ext	6		
6	Hold time, external FSR high after CLKR low	$t_{h(CKRL-FRH)}$		CLKR int	0		
				CLKR ext	6		
7	Setup time, DR valid before CLKR low	$t_{su(DRV-CKRL)}$		CLKR int	21		
				CLKR ext	6		
8	Hold time, DR valid after CLKR low	$t_{h(CKRL-DRV)}$		CLKR int	0		
				CLKR ext	6		
10	Setup time, external FSX high before CLKX low	$t_{su(FXH-CKXL)}$		CLKR int	21		
				CLKR ext	6		
11	Hold time, external FSX high after CLKX low	$t_{h(CKXL-FXH)}$		CLKR int	0		
				CLKR ext	10		
Switching characteristics for McBSP 44/ 47/ See figure 37							
2	Cycle time, CLKR/X	$t_{c(CKRX)}$		CLKR/X int	6P or 1 49/ 50/ 53/		ns
17	Delay time, CLKS high to internal CLKR/X	$t_{d(CLKS-CLKRX)}$		CLKR/X int	1	24	
3	Pulse duration, CLKR/X high or CLKR/X low	$t_{w(CKRX)}$		CLKR/X int	C-1 54/	C+1 54/	
4	Delay time, CLKR high to internal FSR valid	$t_{d(CKRH-FRV)}$		CLKR int	3	25	
				CLKX ext	3	25	
9	Delay tine, CLKR high to internal FSX valid	$t_{d(CKXH-FXV)}$		CLKX int	-4	8	
				CLKX ext	3	25	
12	Disable time, DX high impedance following last data bit from CLKX high	$t_{dis(CKXH-DXHZ)}$		CLKX int		12	
				CLKX ext		12	
13	Delay time, CLKX high to DX valid	$t_{d(CKXH-DXV)}$		CLKX int	-5	12	
				CLKX ext	3	25	
14	Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode	$t_{d(FXH-DXV)}$		FSX int		14	
				FSX ext		25	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

	Test	Symbol	Test condition 2/ Device type: All	Master		Unit
				Min	Max	
	ASP TIMING					
ASP as SPI timing requirements CLKSP = 10b, CLKXP = 0						
M30	Setup time, DR valid before CLKX low	$t_{su(DRV-CKXL)}$	See figure 38	11		ns
M31	Hold time, DR valid after CLKX low	$t_{h(CKXL-DRV)}$		0		
ASP as SPI switching characteristics CLKSP = 10b, CLKXP = 0						
M33	Cycle time, CLKX	$t_{c(CKX)}$	See figure 38	38.4 or 2P 49/ 50/		ns
M24	Delay time, CLKX low to FSX high 55/	$t_{d(CKXL-FXH)}$		T-2	T+3	
M25	Delay time, FSX low to CLKX high 56/	$t_{d(FXL-CKXH)}$		L_1-2	L_1+2	
M26	Delay time, CLKX high to DX valid	$t_{d(CKXH-DXV}$		-2	6	
M27	Disable time, DX high impedance following last data bit from CLKX low	$t_{dis(CKXL-DXHZ)}$		L_1-3	L_1+3	
ASP as SPI timing requirements CLKSP = 11b, CLKXP = 0						
M39	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$		11		ns
M40	Hold time, DR valid after CLKX high	$t_{h(CKXH-DRV)}$		1		
ASP as SPI switching characteristics CLKSP = 11b, CLKXP = 0						
M42	Cycle time, CLKX	$t_{c(CKX)}$	See figure 39	38.5 or 2P 49/ 50/		ns
M34	Delay time, CLKX low to FSX high 57/	$t_{d(CKXL-FXH)}$		L_1-2	L_1+3	
M35	Delay time, FSX low to CLKX high 56/	$t_{d(FXL-CKXH)}$		T-2	T+2	
M36	Delay time, CLKX low to DX valid	$t_{d(CKXL-DXV}$		-2	6	
M37	Disable time, DX high impedance following last data bit from CLKX low	$t_{dis(CKXL-DXHZ)}$		-3	3	
M38	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$		H_1- 2	H_1+ 10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

	Test	Symbol	Test condition 2/ Device type: All	Master		Unit
				Min	Max	
	ASP TIMING - Continued					
ASP as SPI timing requirements CLKSP = 10b, CLKXP = 1						
M49	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	See figure 40	11		ns
M50	Hold time, DR valid after CLKX high	$t_{h(CKXH-DRV)}$		0		
ASP as SPI switching characteristics CLKSP = 10b, CLKXP = 1						
M52	Cycle time, CLKX	$t_{c(CKX)}$	See figure 40	38.5 or 2P 49/ 50/		ns
M43	Delay time, CLKX HIGH to FSX high 51/	$t_{d(CKXH-FXH)}$		T-1	T+3	
M44	Delay time, FSX low to CLKX low 56/	$t_{d(FXL-CKXL)}$		H_1-2	H_1+2	
M45	Delay time, CLKX low to DX valid	$t_{d(CKXL-DXV}$		-2	6	
M46	Disable time, DX high impedance following last data bit from CLKX high	$t_{dis(CKXH-DXHZ)}$		H_1-3	H_1+3	
ASP as SPI timing requirements CLKSP = 11b, CLKXP = 1						
M58	Setup time, DR valid before CLKX low	$t_{su(DRV-CKXL)}$	See figure 41	11		ns
M59	Hold time, DR valid after CLKX low	$t_{h(CKXL-DRV)}$		0		
ASP as SPI switching characteristics CLKSP = 11b, CLKXP = 1						
M62	Cycle time, CLKX	$t_{c(CKX)}$	See figure 41	38.5 or 2P 49/ 50/		ns
M53	Delay time, CLKX high to FSX high 51/	$t_{d(CKXH-FXH)}$		H_1-1	H_1+3	
M54	Delay time, FSX low to CLKX low 58/	$t_{d(FXL-CKXL)}$		T-2	T+2	
M55	Delay time, CLKX low to DX valid	$t_{d(CKXL-DXV}$		-2	6	
M56	Disable time, DX high impedance following last data bit from CLKX high	$t_{dis(CKXH-DXHZ)}$		-3	3	
M57	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$		L_1- 1	L_1+ 10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

	Test	Symbol	Test condition 2/ Device type: All	Limits Min	Limits Max	Unit
	TIMER ELECTRICAL DATA/TIMING					
Timing requirements for Timer input 59/ 60/ 61/						
1	Cycle time, TIM_IN	$t_{c(TIN)}$	See figure 42	4P		ns
2	Pulse duration, TIM_IN high	$t_{w(TINPH)}$		0.45C	0.55C	
3	Pulse duration, TIM_IN low	$t_{w(TINPL)}$		0.45C	0.55C	
4	Transition time, YTIM_IN	$t_{t(TIN)}$			0.05C	
	PULSE WIDTH MODULA (PWM)0/1/2/3 LECETRICAL TIMING DATA					
Switching characteristics forPWM0/1/2/3 outputs						
1	Pulse duration, PWMx high	$t_{w(PWMH)}$	See figure 43 and 44	P		ns
2	Pulse duration, PWMx low	$t_{w(PWML)}$		P		
3	Transition time, PWMx	$t_{t(PWM)}$			.05P	
4	Delay time, CCDC(VD) trigger event to PWMx valid	$t_{d(CCDC-PWMV)}$			10	
	REAL TIME OUT (RTO) ELECTRICAL/TIMING DATA					
Switching characteristics for RTO outputs						
1	Pulse duration, RTOx high	$t_{w(RTOH)}$	See figure 45 and 46	P		ns
2	Pulse duration, RTOx low	$t_{w(RTOL)}$		P		
3	Transition time, RTOx	$t_{t(RTO)}$			.1P	
4	Delay time, Timer 3 (TINT 12 or TINT34) trigger event to RTOx valid	$t_{d(TIMER3-RTOV)}$			10	
	JTAG TEST PORT ELECTRICAL DATA/TIMING					
Timing requirements for JTAG test port						
1	Cycle time, TCK	$t_{c(TCK)}$	See figure 47	20		ns
2	Pulse duration, TCK high	$t_{w(TCKH)}$		8		
3	Pulse duration, TCK low	$t_{w(TCKL)}$		8		
4	Setup time, TDI valid before RTCK high	$t_{su(TDIV-RTCKH)}$		10		
5	Hold time, TDI valid after RTCK high	$t_{h(RTCKH-TDIV)}$		9		
6	Setup time, TMS valid before RTCK high	$t_{su(TMSV-RTCKH)}$		2		
7	Hold time, TMS valid after RTCK high	$t_{h(RTCKH-TMSIV)}$		5		
Switching characteristics for JTAG test port						
8	Cycle time, TCK	$t_{c(TCK)}$	See figure 47	20		ns
9	Pulse duration, TCK high	$t_{w(TCKH)}$		10		
10	Pulse duration, TCK low	$t_{w(TCKL)}$		10		
11	Rise time, all JTAG outputs	$t_{r(all\ JTAG\ outputs)}$			1.3	
12	Fall time, all JTAG outputs	$t_{f(all\ JTAG\ outputs)}$			1.3	
13	Delay time, TCK low to TDO valid	$t_{d(RTCKL-TDOV)}$			$0.25*t_{c(RTCK)}$	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ Over recommended ranges of supply voltage and operating temperature in the recommended operating conditions table. For test conditions shown as MIN, MAX, or TYP, use the appropriate value specified in the recommended operating conditions table. (Unless otherwise noted.)
3/ These I/O specifications apply to regular 3.3 V I/Os and do not apply to DDR2/mDDR, USB I/Os are 1.8 V I/Os and adhere to USB2.0 spec.
4/ This specifications applies only to pins with an internal pullup (PU) or pulldown (PD). See manufacturer data for more information.
5/ To pull up a signal to the opposite supply rail, a 1 kΩ resistor is recommended.
6/ 100% color bar are not supported. 100% color bar require 1.2 V peal-to peak. The video buffer only provides 1.0 V peak-to-peak.
7/ BTSEL[1:0] and AECFG[4:0] are the boot configuration pins during device reset.
8/ C = MXI/CLKIN cycle time in ns. For example, when MXI/CLKIN frequency is 24 MHz use C = 41.6 ns
9/ The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.
10/ C= MXI1/CLKIN1 cycle time in ns. For example, when MXI1/CLKIN1 frequency is 24 MHz use C = 41.6 ns
11/ tc(MXI1) = 41.6 ns and tc(MXI1) = s7.7 ns are the only supported cycle times for MXI1/CLKIN1.
12/ C = MXI2/CLKIN2 cycle time in ns. For example, when MXI2/CLKIN2 frequency is 24 MHz use C = 41.6 ns
13/ tc(MXI2) = 37.037 ns is the only supported cycle times for MXI2/CLKIN2.
14/ P = 1/CLKOUT1 clock frequency in nanoseconds (ns). For example, when CLKOUT1 frequency is 24 MHz use P = 41.6 ns.
15/ P = 1/CLKOUT2 clock frequency in nanoseconds (ns). For example, when CLKOUT2 frequency is 8 MHz use P = 125 ns.
16/ P = 1/CLKOUT3 clock frequency in nanoseconds (ns). For example, when CLKOUT3 frequency is 3 MHz use P = 333.3 ns.
17/ This parameter value should not be used as a maximum performance specification. Actual performance of back-to-back accesses of the GPIO is dependent upon internal bus activity.
18/ The pulse width given is sufficient to generate an interrupt or an EDMA event. However, if a user wants to have DM355 to recognize the GPIO changes through software polling of the GPIO register, the GPIO duration must be extended to allow DM355 enough time to access the GPIO register through the internal bus.
19/ E = PLLC1 SYSCLK2 period in ns. SYSCLK2 is the EMIF peripheral clock. SYSCLK2 is one-fourth the PLLC output clock. For Example when PLLC output clock = 432 MHz, E = 9.259 ns. See manufacturer for more information.
20/ Set up before end of STROBE phase (if no extended wait states are inserted) by which EM_WAIT must be asserted to add extended wait states. Figure 15 and 16 describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the $E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.
21/ TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write stobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed via the Asynchronous Bank and Asynchronous Wait cycle Configuration registers. These support the following range of values: TA[4-1], RS[16-1], RH[8-1], WS[16-1], WST[64-1], WH[8-1], and MEW[1-256].
22/ EWC = external wait cycles determined by EM_WAIT input signal. EWC supports the following range of values EWC[256-1]. Note that the maximum wait time before timeout is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration register.
23/ $t_{c(EM_CLK)}/3$
24/ For this parameter, you may include margin in your board design so that the toh = 2.5 ns of the MMC/SD device is not degraded at the DM355 input pin.
25/ P = 1/SYSCLK4 in ns. For example, if SYSCLK4 frequency is 135 MHz, use P = 7.41 ns.
26/ Use whichever value is greater.
27/ The VPFE may be configured to operate in either positive or negative edge clocking mode. When in positive edge clocking mode the rising edge of PCLK is referenced. When in negative edge clocking mode the failing edge of PCLK is referenced.
28/ For timing specifications relating to PCLK see manufacturer for more information.
29/ VCTL = HSYNC, VSYNC, and FIELD
30/ VCLKIN = PCLK or EXTCLK

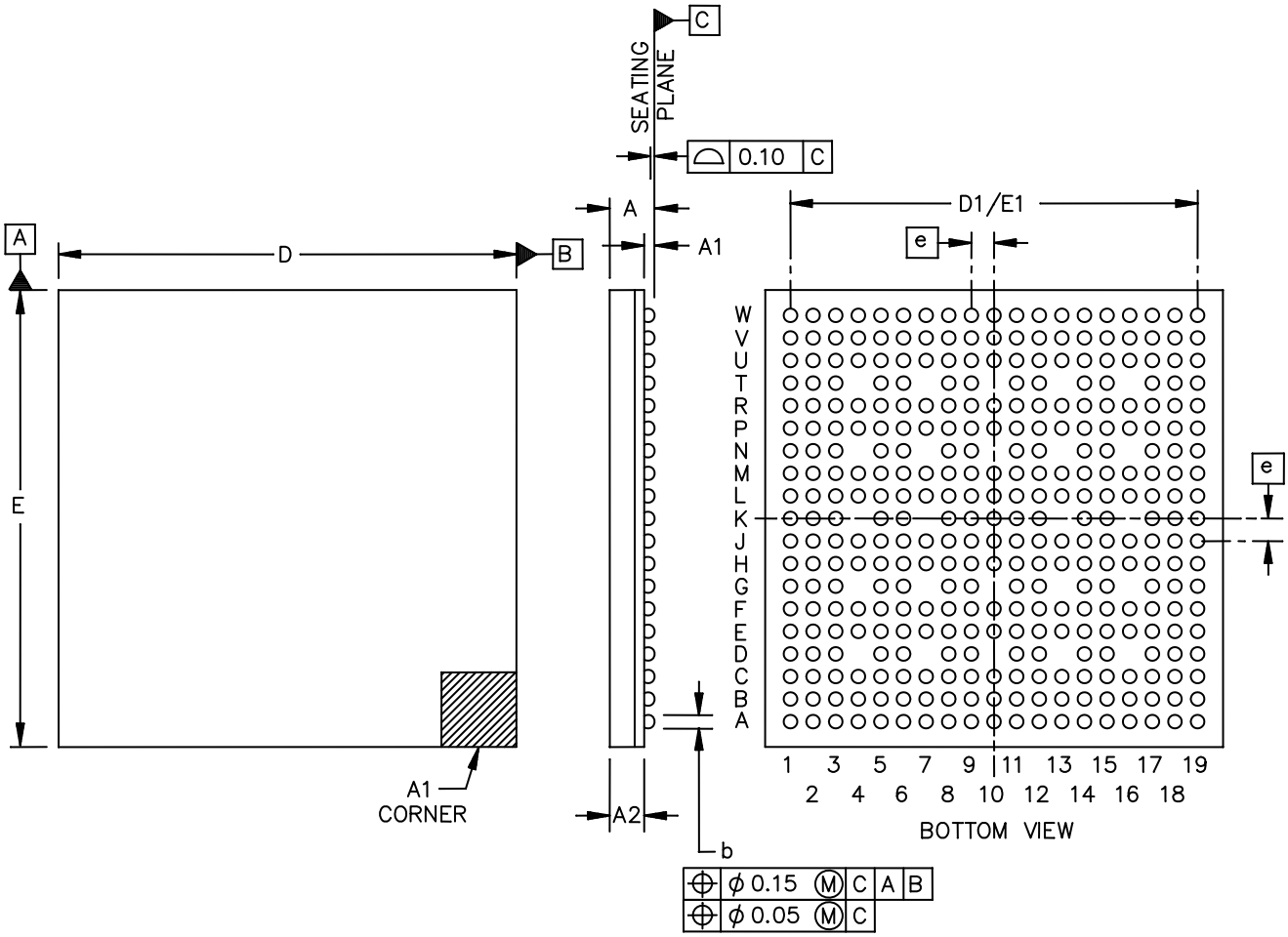
TABLE I. Electrical performance characteristics - Continued.

31/ VCTL = HSYNC, VSYNC, FIELD and LCD_OE
32/ VCLKIN = PCLK or EXTCLK. for timing specifications relating to PCLK see manufacturer data for more information.
33/ For more detailed specification, see manufacturer data for more information.
34/ Low speed: C_L = 200 pF, Full speed: C_L = 50 pF, High speed: C_L = 50 pF
35/ $t_{frfm} = (t_r/t_f) \times 100$. [Excluding the first transaction from the idle state.]
36/ $t_{jr} = t_{px}(1) - t_{px}(0)$
37/ U = UART baud time = 1/programmed baud rate.
38/ T = tc(CLK) = SPI_CLK period is equal to the SPI module clock divided by a configurable divider.
39/ P = 1/SYSCLK2 in ns. For example, if SYSCLK2 frequency is 135 MHz, use P = 7.41 ns.
40/ The delay time can be adjusted using the SPI module register C2TDELAY.
41/ The delay time can be adjusted using the SPI module register T2CDELAY.
42/ The I^2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
43/ A fast mode I^2C bus device can be used in a standard mode I^2C bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r max + $t_{su(SDA-SCLH)}$ = 1000 + 250 = 1250 ns (according to the standard mode I^2C bus specification) before the SCL line is released.
44/ A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL
45/ The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the low period [$t_{w(SCLL)}$] of the SCL signal.
46/ $20 + 0.1C_b$
47/ C_b = total capacitance of one bus line in pF. If mixed with HS mode devices, faster fall time are allowed.
48/ CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
49/ P = (1/SYSCLK2), where SYSCLK2 is an output clock of PLLC1
50/ Use whichever value is greater.
51/ The ASP does not have a duty cycle specification, just ensure that the minimum pulse duration specification is met.
52/ Minimum delay times also represent minimum output hold times.
53/ Minimum CLKR/X cycle times must be met, even when CLKR/X is generated by an internal clock source. Minimum CLRK/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.
54/ C = H or L
S = sample rate generator input clock = P if CLKSM = 1 (P = 1/SYSCLK2, where SYSCLK2 is an output of PLLC1)
S = sample rate generator input clock = CLKS if CLKSM = 0
H = CLKX high pulse width = (CLKGDV/2 + 1)*S if CLKGDV is even
H = (CLKGDV + 1)/2 * S if CLKGDV is odd or zero
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
L = (CLGKDV + 1)/2 * S if CLKGDV is odd or zero
CLKGDV should be set appropriately to ensure the ASP bit rate does not exceed the maximum limit
55/ T = CLKX period = (1 + CLKGDV) x 2P
L_1 = CLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) x 2P when CLKGVD is even
H1 = CLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) x 2P when CLKGDV is even
56/ FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).
57/ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active low slave enable output.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master ASP

TABLE I. Electrical performance characteristics - Continued.

58/ FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).
59/ GPIO000, GPIO001, GPIO002, and GPIO003 can be used as an external clock input for Timer 3.
60/ P = MXI1/CLKIN cycle time in ns. For example, when MXI1/CLKIN frequency is 24 MHz use P = 41.6 ns.
61/ C = TIM_IN ycle time in ns. For example, when TIM_IN frequency is 24 MHz use C = 41.6 ns.

Case X



Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.30	D/E	12.90	13.10
A1	0.23	0.33	D1/E1	11.70 TYP	
A2	0.84	0.94	e	0.65 BSC	
b	0.36	0.46			

Notes:
1. This drawing is subject to change without notice.
2. Dimensioning and tolerancing per ASME Y14.5M-1994

FIGURE 1. Case outline.

Case X

	1	2	3	4	5	6	7	8	9
J	RSV01	V_{SS}	CIN0	CIN3	CIN2	V_{SS}	VREF	V_{DDA33_USB}	V_{SSA_PLL2}
H	V_{SS}	V_{SS}	VCLK	FIELD	LCD_OE	V_{SS}	V_{DDA13_USB}	NC	V_{DDA_PLL2}
G	VFB	V_{SS}	EXTCLK		VSYNC	CV_{DD}		V_{DD}	V_{SS}
F	TVOUT	IBIAS	COUT1	COUT0	HSYNC	V_{DD_VOUT}	V_{DD_VOUT}	V_{DD_VOUT}	V_{DD}
E	IOUT	V_{SS}	COUT3	COUT2	USB_VBUS	V_{SS_USB}	EMU1	EMU0	TDO
D	V_{SS}	COUT6	COUT4		USB_ID	V_{SS_USB}		TMS	TDI
C	COUT5	COUT7	YOUT7	CV_{DD}	USB_DRV VBUS	V_{DDD13_USB}	USB_R1	$V_{SS_USB_REF}$	$\overline{TRST}$
B	YOUT0	YOUT3	YOUT4	YOUT5	V_{SS}	$V_{DDA33_USB_PLL}$	V_{SS_USB}	V_{SS}	MXO1
A	CV_{DD}	YOUT1	YOUT2	YOUT6	V_{SS}	USB_DM	USB_DP	V_{SS}	MXI1

FIGURE 2. Terminal connections.

Case X

	1	2	3	4	5	6	7	8	9
W	V_{SS}	DDR_A02	DDR_A03	DDR_A05	DDR_A08	DDR_A09	DDR_A11	$\overline{\text{DDR_CLK}}$	DDR_CLK
V	V_{SS}	DDR_A00	DDR_A01	DDR_A04	DDR_A07	DDR_A10	DDR_A12	DDR_BA[2]	$\overline{\text{DDR_CAS}}$
U	V_{SS}	V_{SS}	V_{SS}	V_{SS}	DDR_A06	DDR_A13	DDR_BA[1]	DDR_BA[0]	V_{SS}
T	MXO2	V_{SS}	PCLK		V_{SS}	$\overline{\text{DDR_RAS}}$		$\overline{\text{DDR_CS}}$	DDR_ZN
R	MXI2	V_{SS}	YIN3	CAM_VD	CAM_WEN_ FIELD	V_{SS}	CV_{DD}	CV_{DD}	V_{DD_DDR}
P	V_{SS_MX2}	YIN1	YIN4	YIN2	YIN0	V_{DD_VIN}	V_{DD_VIN}	V_{DD_VIN}	V_{DD_DDR}
N	V_{SS}	RSV05	CIN7		CAM_HD	CV_{DD}		V_{SS}	V_{SS}
M	RSV04	RSV06	CIN5	YIN6	YIN5	V_{SS}	V_{SS}	V_{SS}	V_{DD_DDR}
L	RSV03	V_{SS}	CIN1	CIN4	YIN7	V_{DD}	V_{DDA18V_DAC}	V_{SS_DAC}	V_{SS}
K	RSV02	RSV07	V_{SS}		CIN6	CV_{DD}		V_{DD}	V_{SS}

FIGURE 2. Terminal connections - Continued.

10	11	12	13	14	15	16	17	18	19	
$\overline{\text{DDR_WE}}$	DDR_DQ01	DDR_DQ05	DDR_DQ07	DDR_DQ10	DDR_DQ11	DDR_DQ13	DDR_DQ15	DDR_ DQGATE0	CV_{DD}	W
DDR_CKE	DDR_DQ00	DDR_DQS[0]	DDR_DQ06	DDR_DQ09	DDR_DQS[1]	DDR_DQ14	DDR_ DQGATE1	V_{SS}	EM_A13	V
DDR_VREF	DDR_DQ02	DDR_DQ04	DDR_DQ08	V_{SS}	DDR_DQM[1]	DDR_DQ12	V_{SS}	UART0_RXD	EM_A12	U
	DDR_DQ03	DDR_DQM[0]		V_{DD_DDR}	V_{SS}		CV_{DD}	UART0_TXD	EM_A08	T
V_{DDA33_DDRDLL}	V_{SSA_DLL}	V_{DD_DDR}	I2C_SDA	I2C_SCL	UART1_RXD	EM_A11	UART1_TXD	EM_A10	EM_A05	R
V_{DD_DDR}	V_{DD_DDR}	V_{DD_DDR}	V_{DD_DDR}	V_{DD_DDR}	EM_A04	EM_A07	EM_A09	EM_A06	EM_BA1	P
	V_{DD}	V_{DD}		V_{SS}	EM_A02		EM_A01	EM_A03	EM_BA0	N
V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{SS}	EM_D13	EM_A00	V_{SS}	EM_D15	EM_D14	M
V_{SS}	CV_{DD}	CV_{DD}	V_{DD}	V_{SS}	EM_D04	EM_D08	EM_D11	EM_D12	EM_D10	L
V_{SS}	CV_{DD}	CV_{DD}		V_{SS}	V_{DD}		EM_D06	EM_D09	EM_D07	K

FIGURE 2. Terminal connections - Continued.

V_{SS}	CV_{DD}	CV_{DD}	CV_{DD}	V_{SS}	EM_WE	EM_CE0	EM_D01	EM_D03	EM_D05	J
CV_{DD}	V_{SS}	V_{SSA_PLL1}	CV_{DD}	V_{SS}	ASP0_DX	EM_ADV	CV_{DD}	EM_D00	EM_D02	H
	CV_{DD}	V_{DDA_PLL1}		V_{DD}	GIO003		ASP0_FSX	EM_WAIT	EM_CE1	G
V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	GIO002	ASP0_FSR	ASP0_CLKR	ASP0_CLKX	EM_OE	F
TCK	RTCK	SPI1_SDO	SPI1_ SDENA[0]	GIO001	V_{SS}	ASP1_FSX	ASP1_FSR	ASP0_DR	EM_CLK	E
	$\overline{\text{RESET}}$	CLKOUT1		MMCSD0_ DATA1	GIO005		ASP1_CLKS	ASP1_CLKR	ASP1_CLKX	D
V_{SS_MX1}	CLKOUT3	SPI0_SCLK	SPI1_SCLK	MMCSD0_CMD	MMCSD1_CLK	GIO000	GIO007	ASP1_DX	ASP1_DR	C
V_{SS}	SPI0_SDO	SPI0_ SDENA[0]	MMCSD0_ DATA2	MMCSD0_ DATA0	MMCSD1_ DATA1	MMCSD1_ DATA3	GIO004	GIO006	CV_{DD}	B
CV_{DD}	CLKOUT2	SPI0_SDI	SPI1_SDI	MMCSD0_ DATA3	MMCSD0_ CLK	MMCSD1_ DATA2	MMCSD1_ CMD	MMCSD1_ DATA0	V_{SS}	A
10	11	12	13	14	15	16	17	18	19	

FIGURE 2. Terminal connections - Continued.

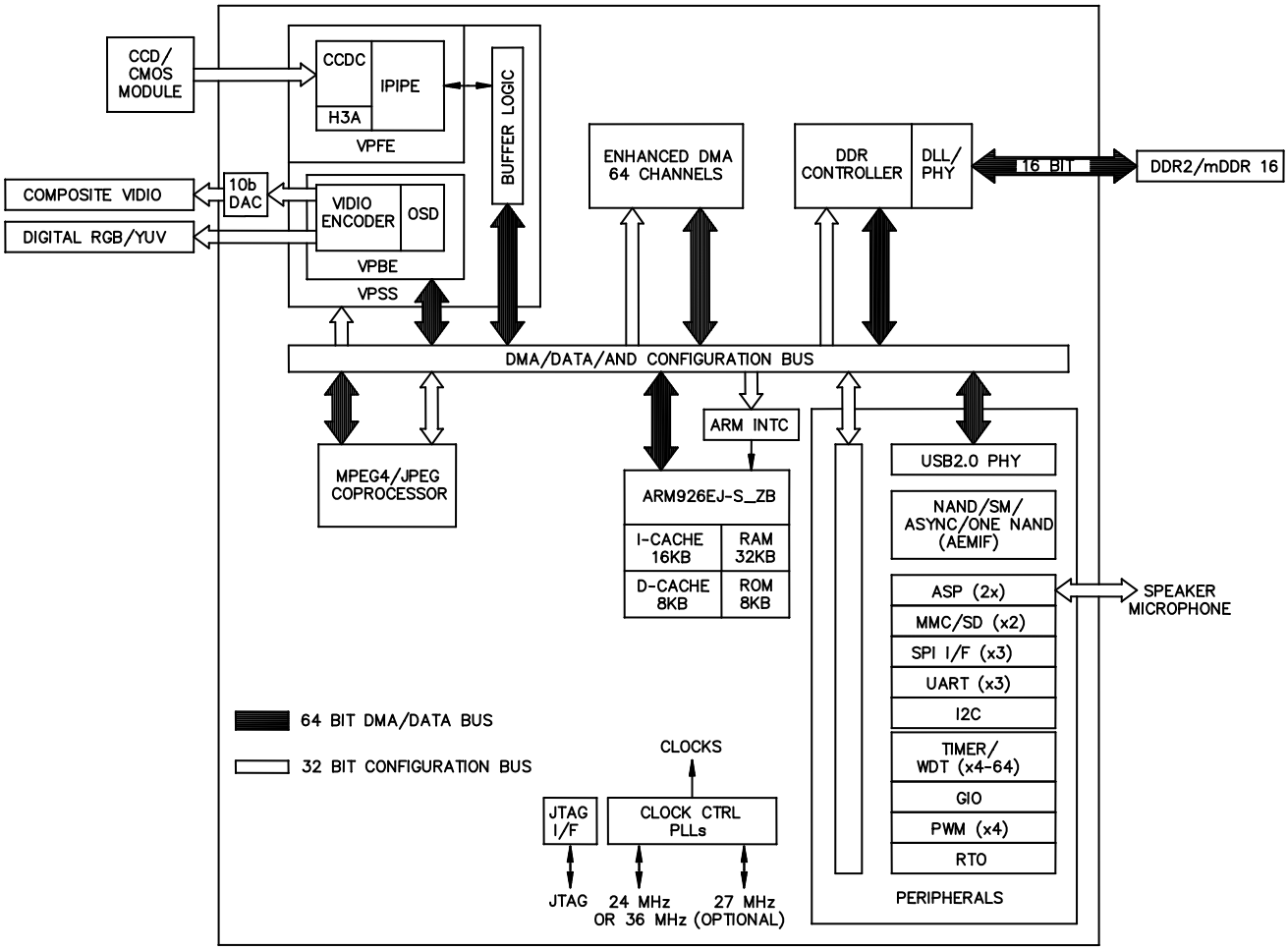
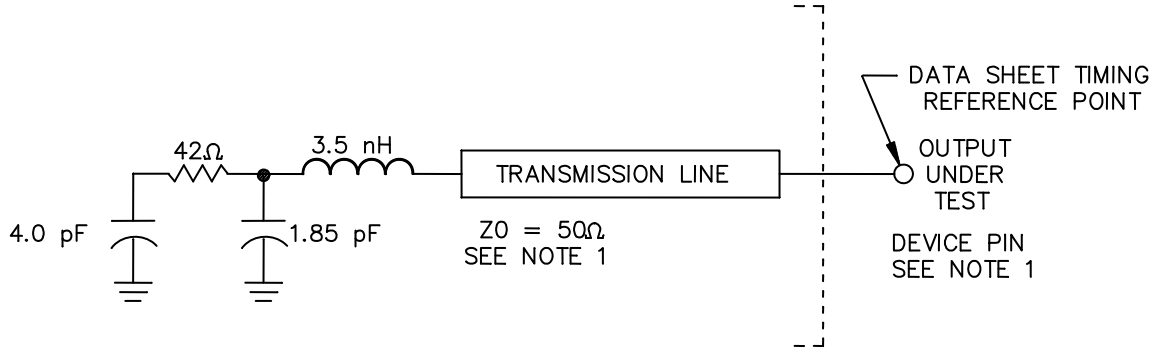
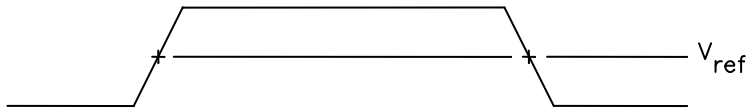


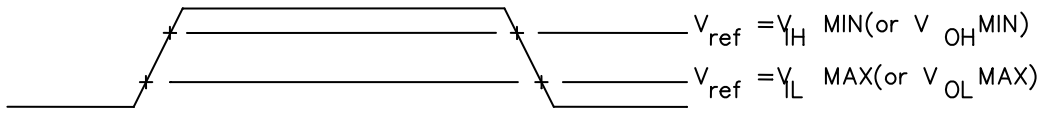
FIGURE 3. Block diagram - Continued.



TEST LOAD CIRCUIT FOR AC TIMING MEASUREMENTS



INPUT AND OUTPUT VOLTAGE REFERENCE LEVELS FOR AC TIMING MEASUREMENTS



RISE AND FALL TRANSITION TIME VOLTAGE REFERENCE LEVELS

Notes:

1. The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timings.
   Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

FIGURE 4. Test load circuit for AC timing measurements.

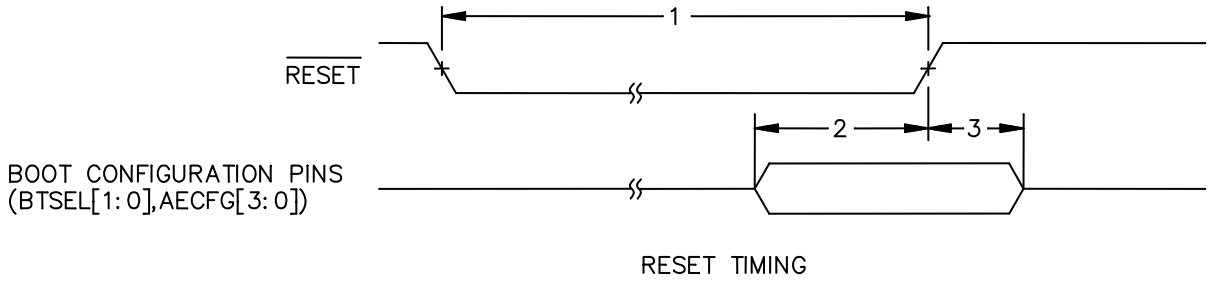


FIGURE 5. Timing waveforms.

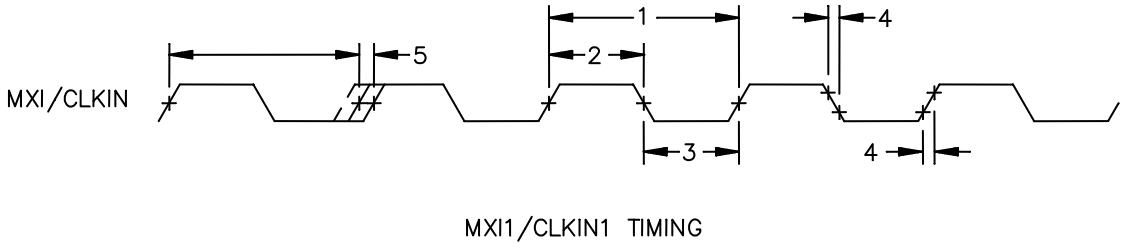


FIGURE 6. Timing waveforms.

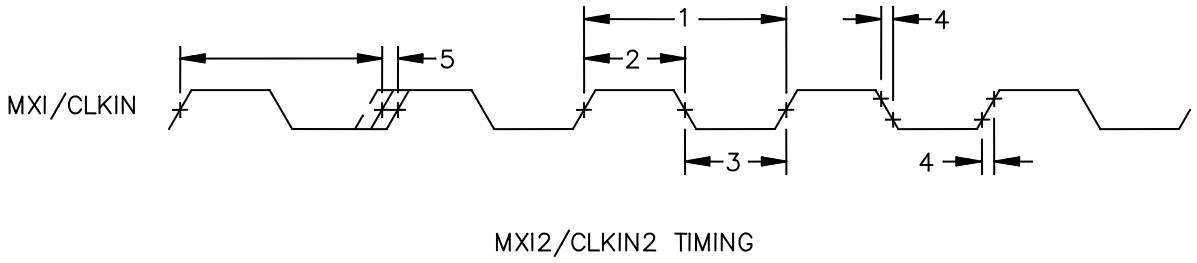


FIGURE 7. Timing waveforms.

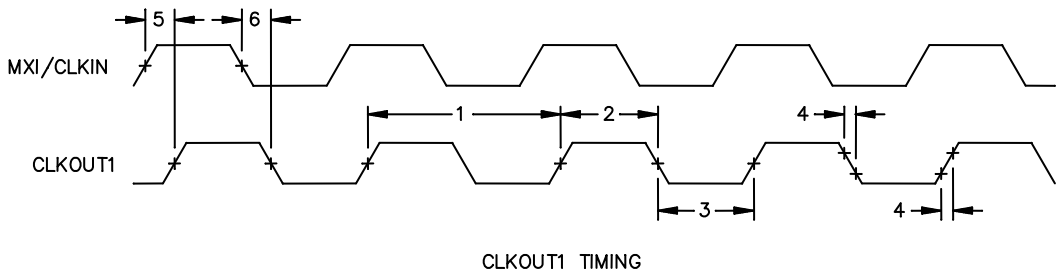


FIGURE 8. Timing waveforms.

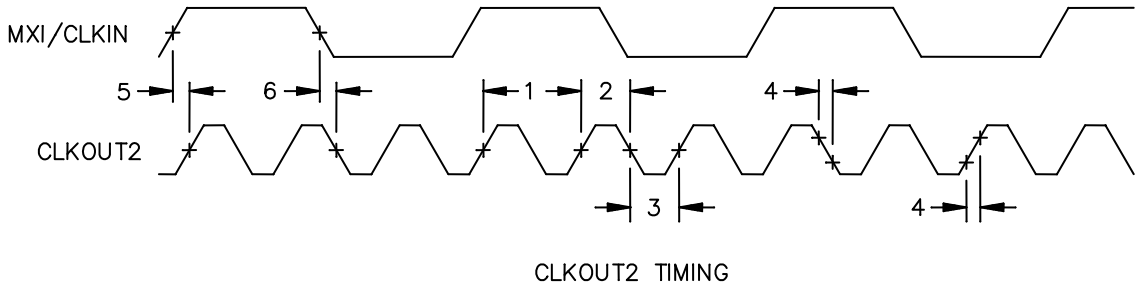


FIGURE 9. Timing waveforms.

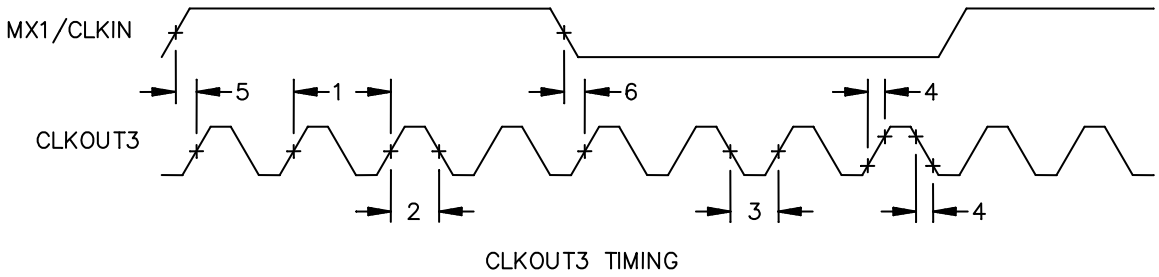


FIGURE10. Timing waveforms.

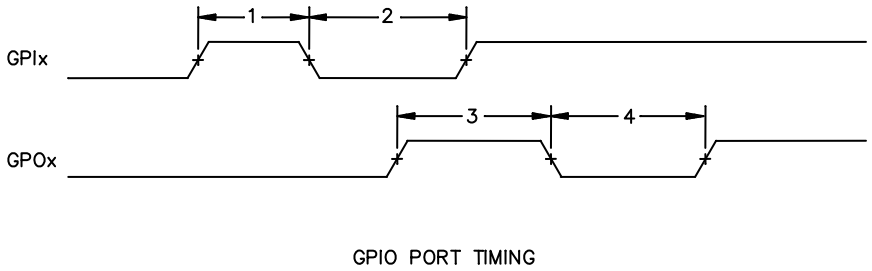


FIGURE 11. Timing waveforms.

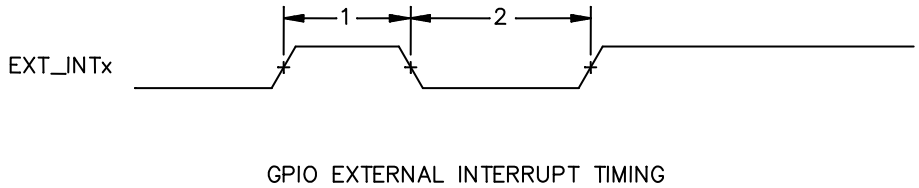


FIGURE12. Timing waveforms.

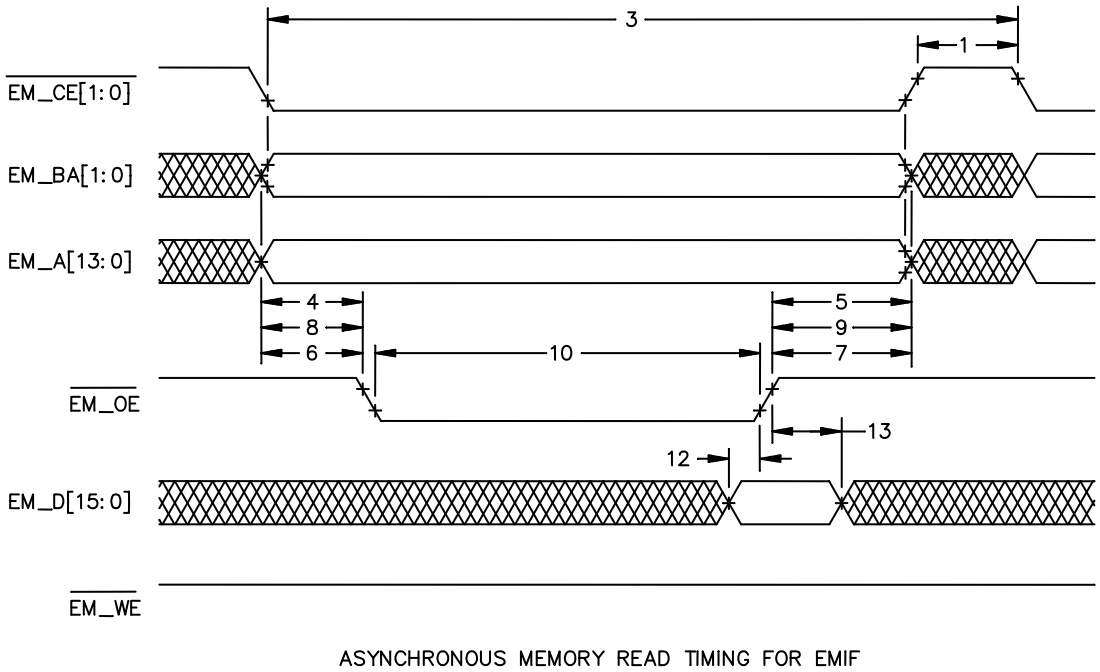
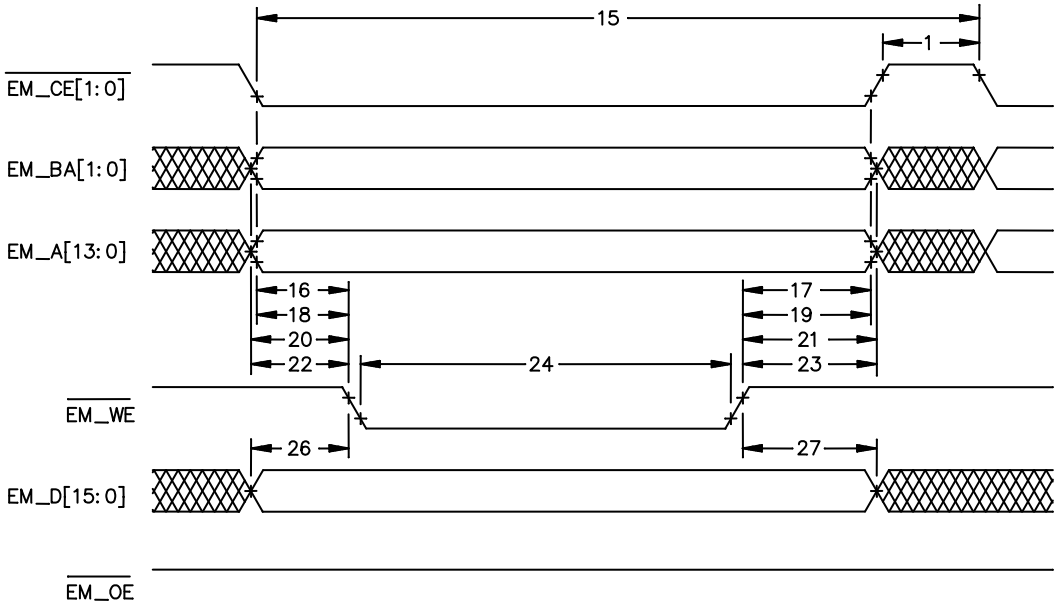
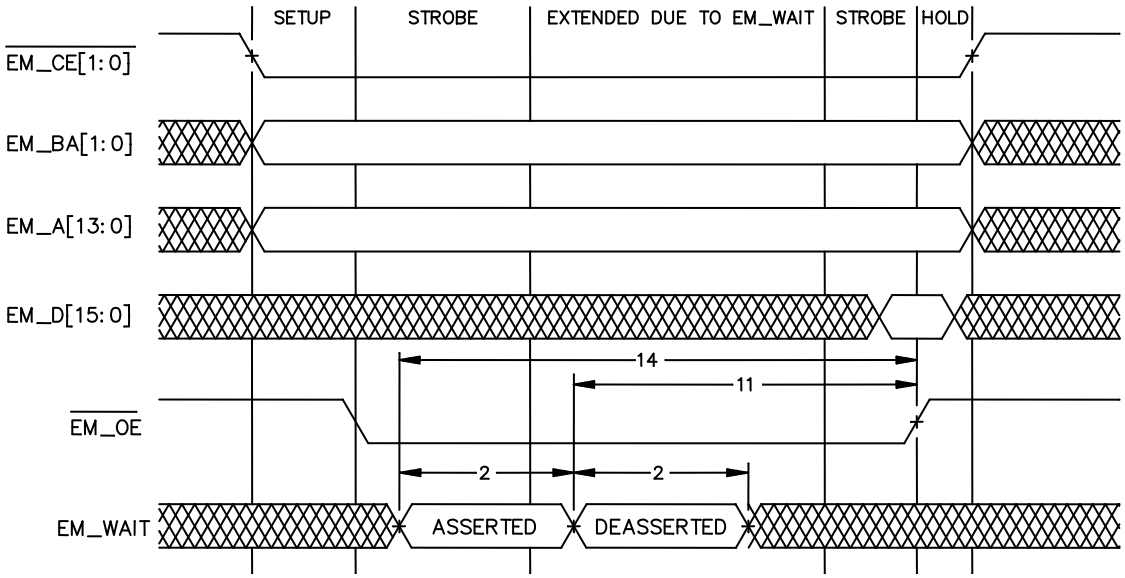


FIGURE 13. Timing waveforms.



ASYNCHRONOUS MEMORY WRITE TIMING FOR EMIF

FIGURE14. Timing waveforms.



EM_WAIT READ TIMING REQUIREMENTS

FIGURE15. Timing waveforms.

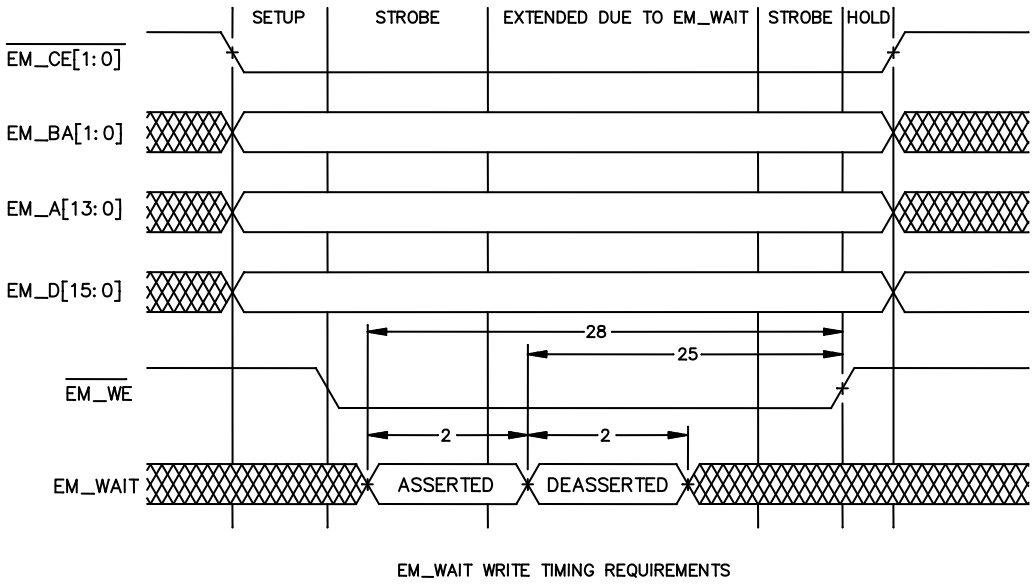


FIGURE 16. Timing waveforms.

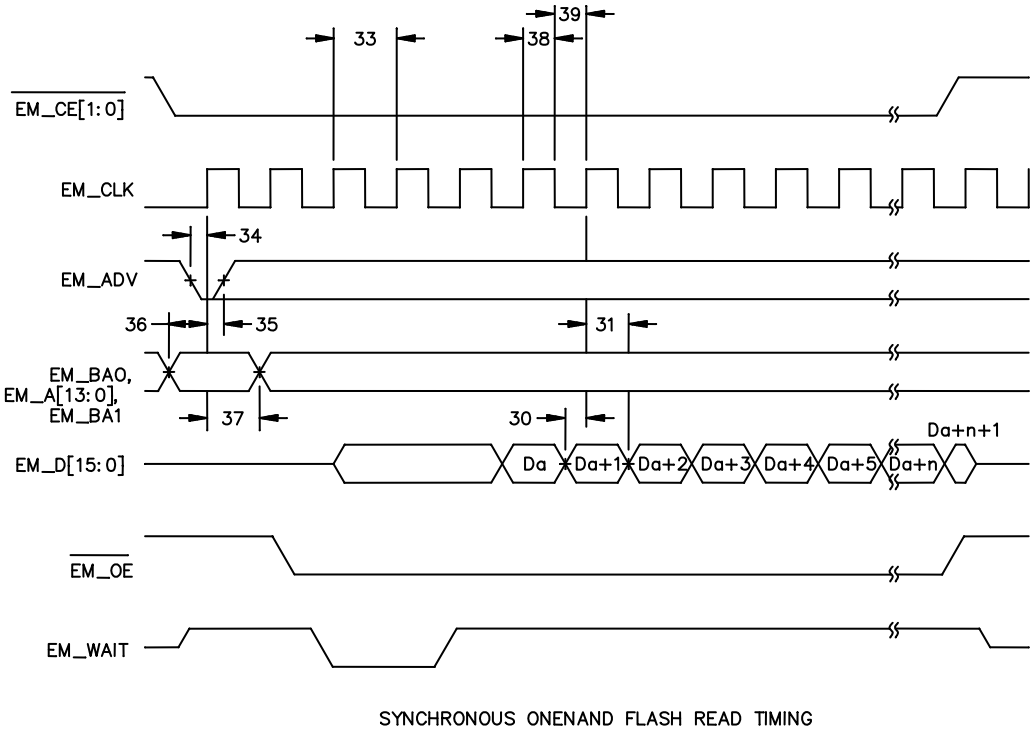


FIGURE 17. Timing waveforms.

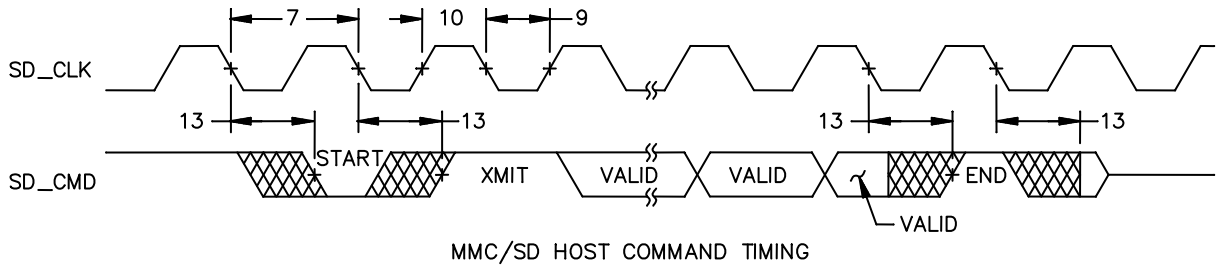


FIGURE 18. Timing waveforms.

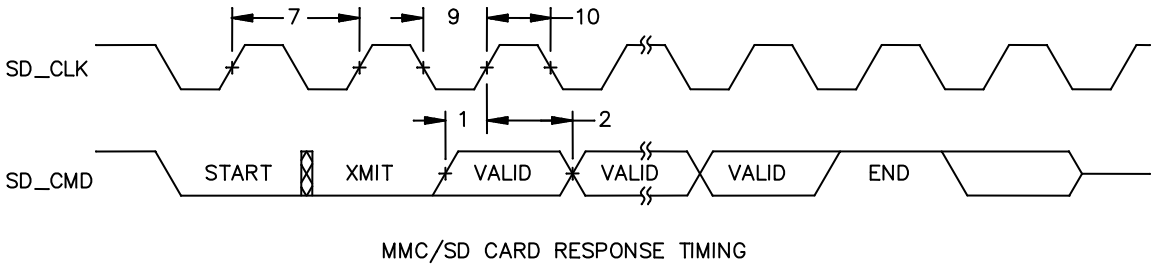


FIGURE 19. Timing waveforms.

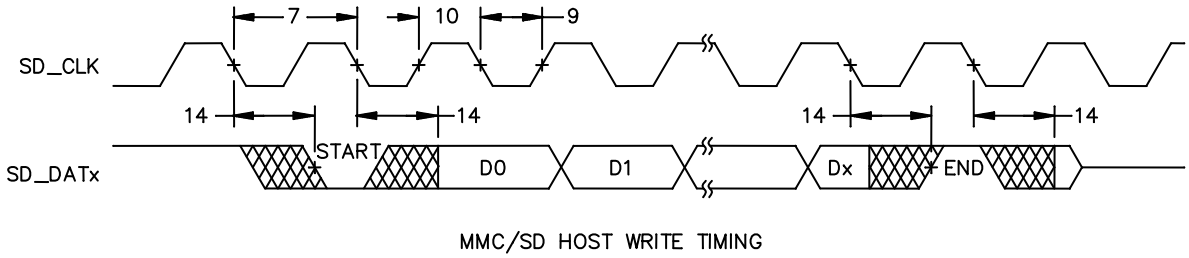


FIGURE 20. Timing waveforms.

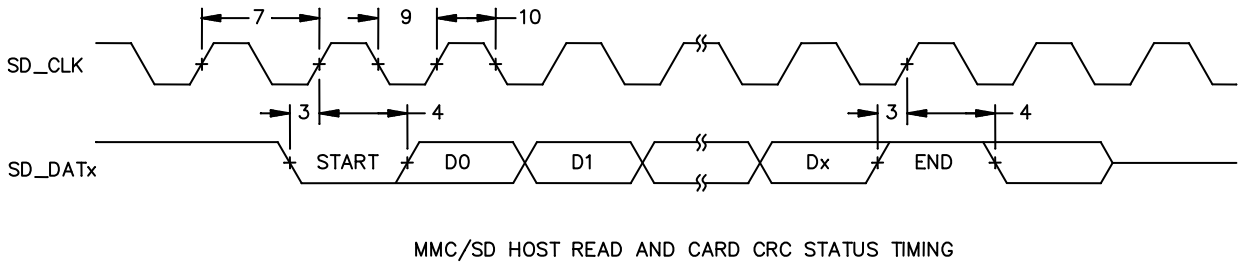


FIGURE 21. Timing waveforms.

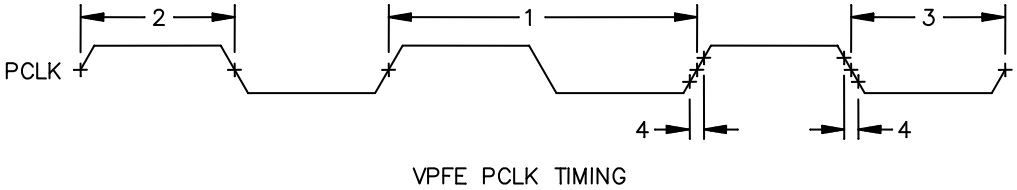


FIGURE 22. Timing waveforms.

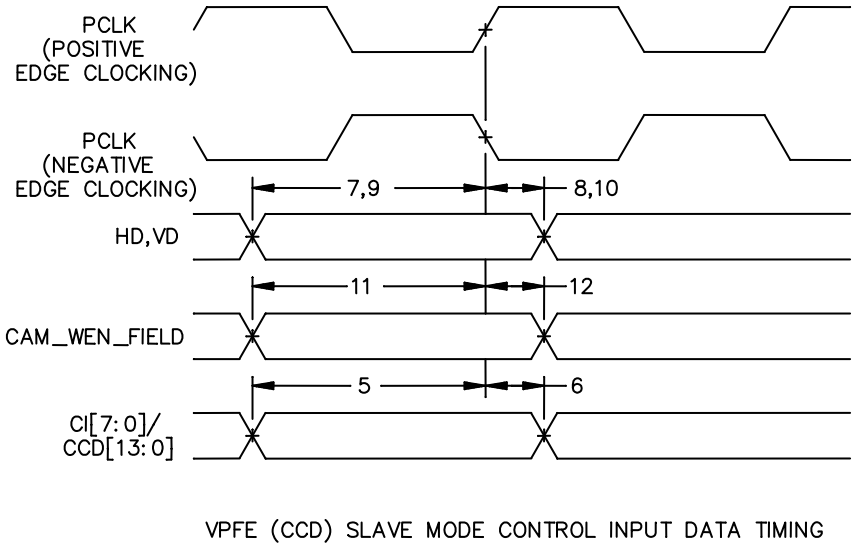


FIGURE 23. Timing waveforms.

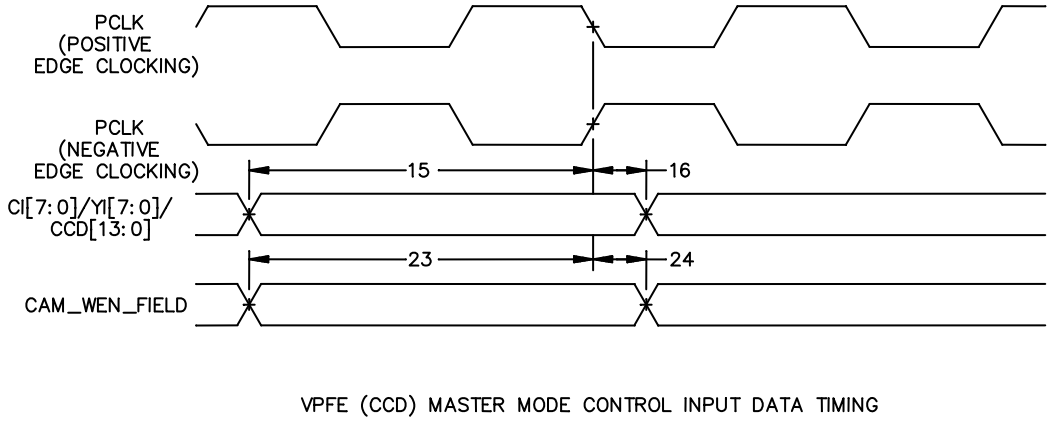


FIGURE 24. Timing waveforms.

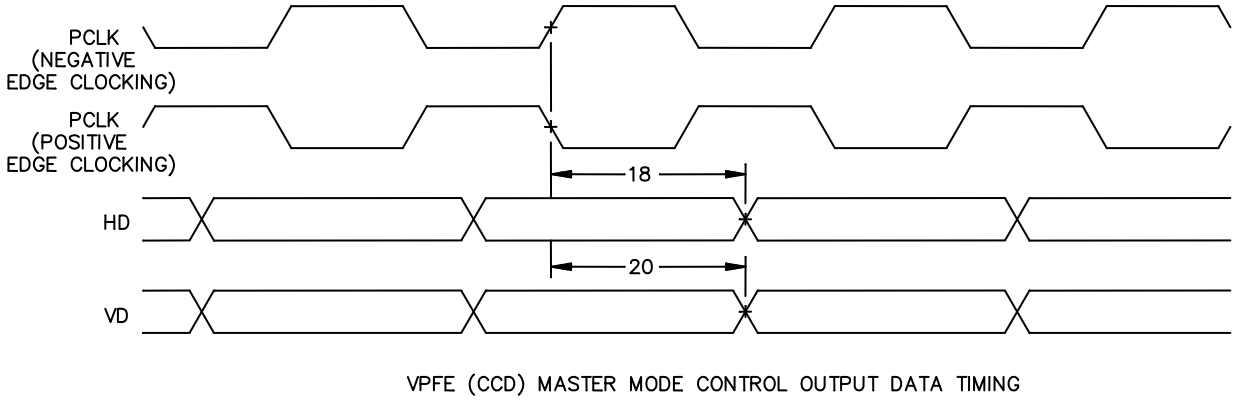


FIGURE 25. Timing waveforms.

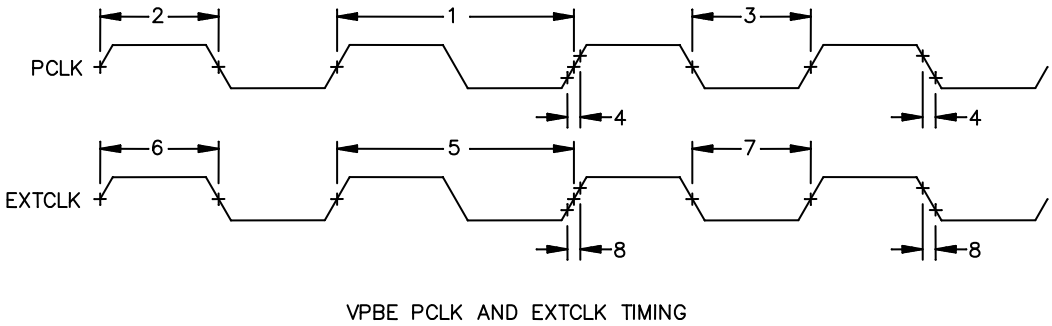
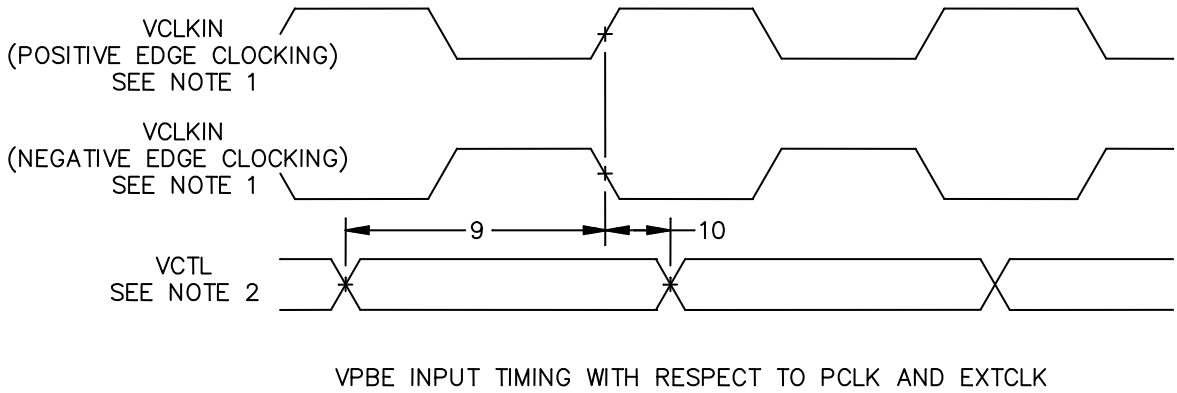
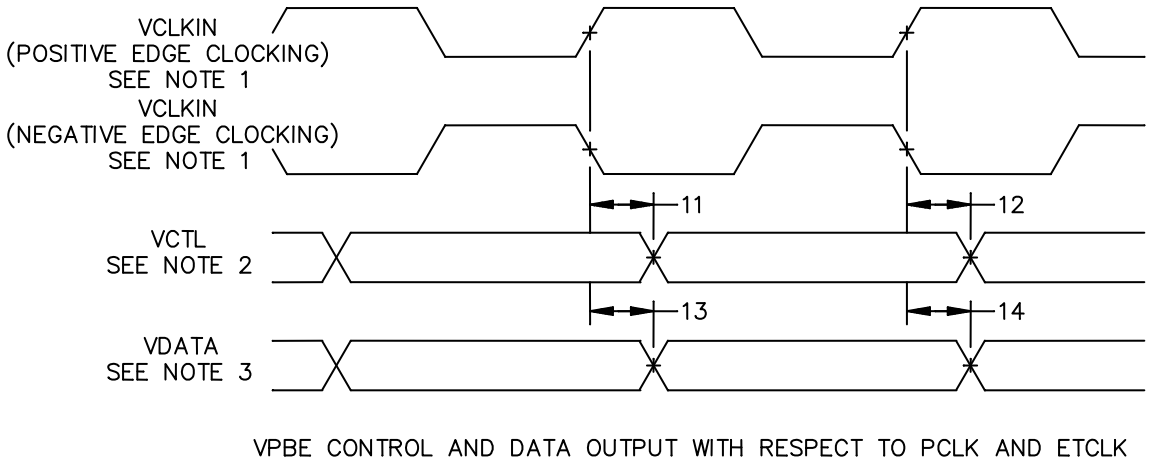


FIGURE 26. Timing waveforms.



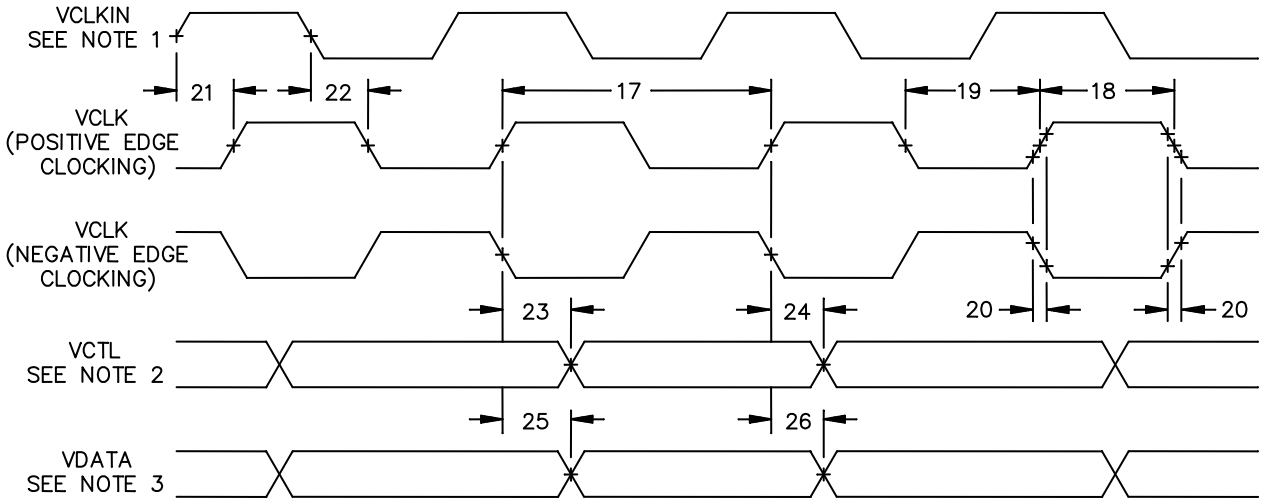
NOTES:
1. VCLKIN = PCLK or EXTCLK
2. VCTL = HSYNC, VSYNC, and FIELD

FIGURE 27. Timing waveforms.



NOTES:
1. VCLKIN = PCLK or EXTCLK
2. VCTL = HSYNC, VSYNC, FIELD, and LCD_OE
3.. VDATA = COUT[7:0], YOUT[7:0], R{7:3], G[7:2], and B[7:3]

FIGURE 28. Timing waveforms.

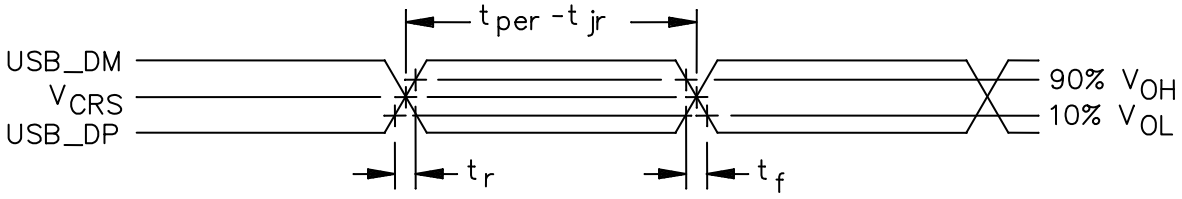


VPBE CONTROL AND DATA OUTPUT TIMING WITH RESPECT TO VCLK

NOTES:

1. VCLKIN = PCLK or EXTCLK
2. VCTL = HSYNC, VSYNC, FIELD, and LCD_OE
3.. VDATA = COUT[7:0], YOUT[7:0], R{7:3], G[7:2], and B[7:3]

FIGURE 29. Timing waveforms.



USB2.0 INTEGRATED TRANSCEIVER INTERFACE TIMING

FIGURE 30. Timing waveforms.

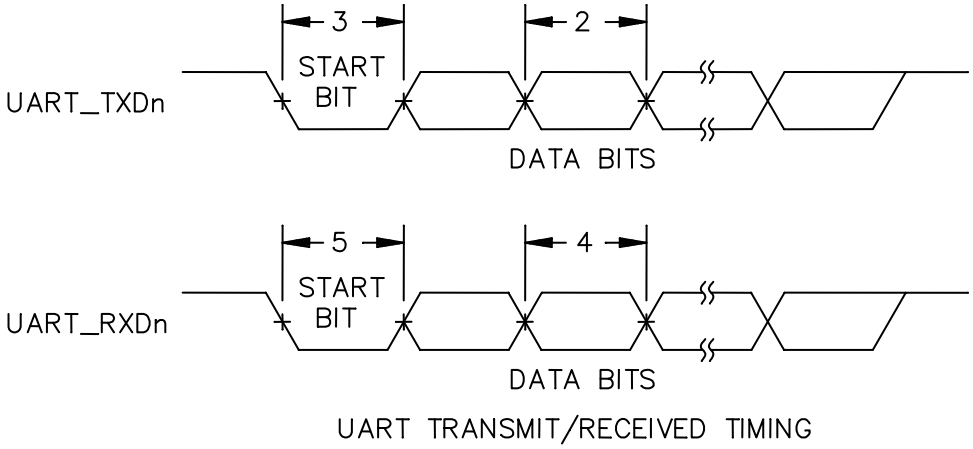


FIGURE 31. Timing waveforms.

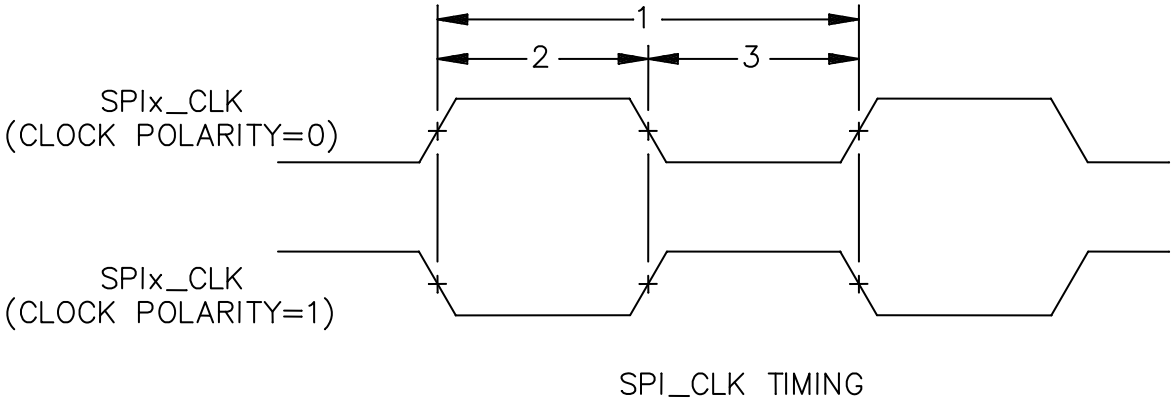
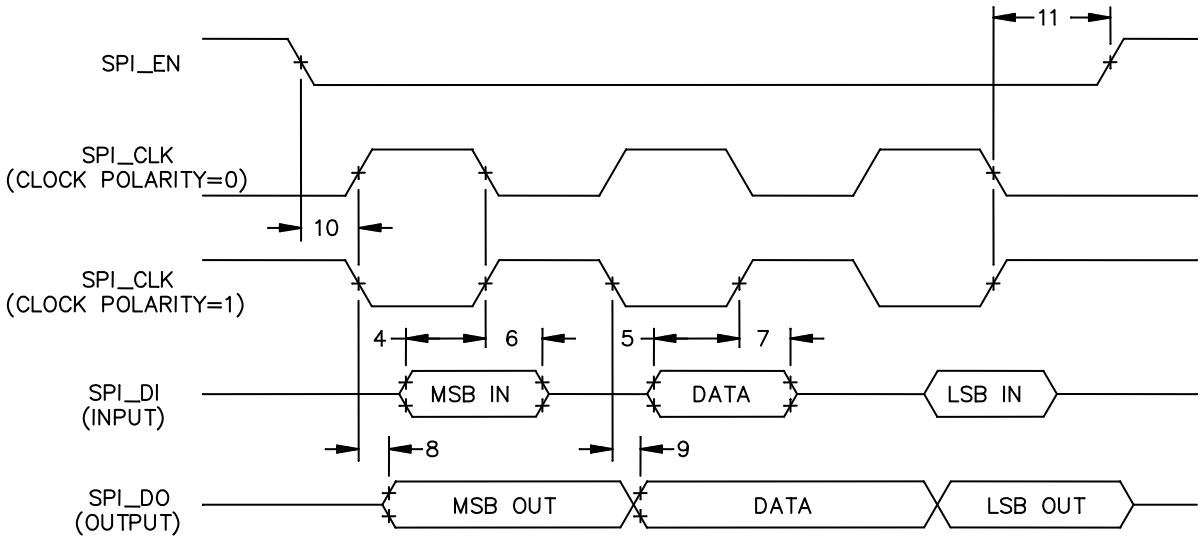
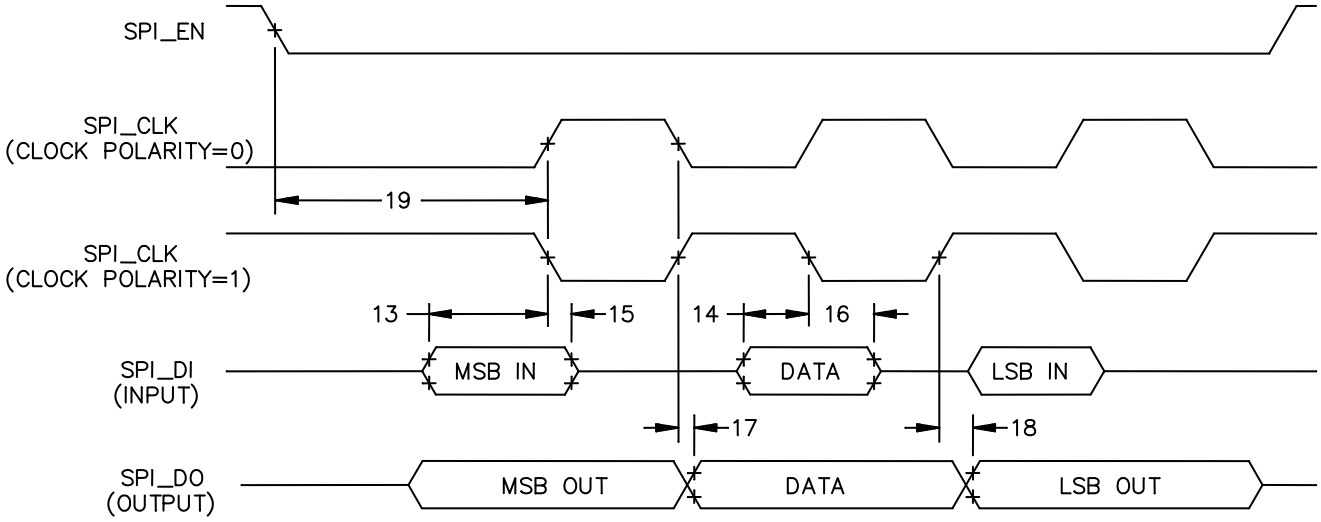


FIGURE 32. Timing waveforms.



SPI MASTER MODE EXTERNAL TIMING (CLOCK PHASE=0)

FIGURE 33. Timing waveforms.



SPI MASTER MODE EXTERNAL TIMING (CLOCK PHASE=1)

FIGURE 34. Timing waveforms.

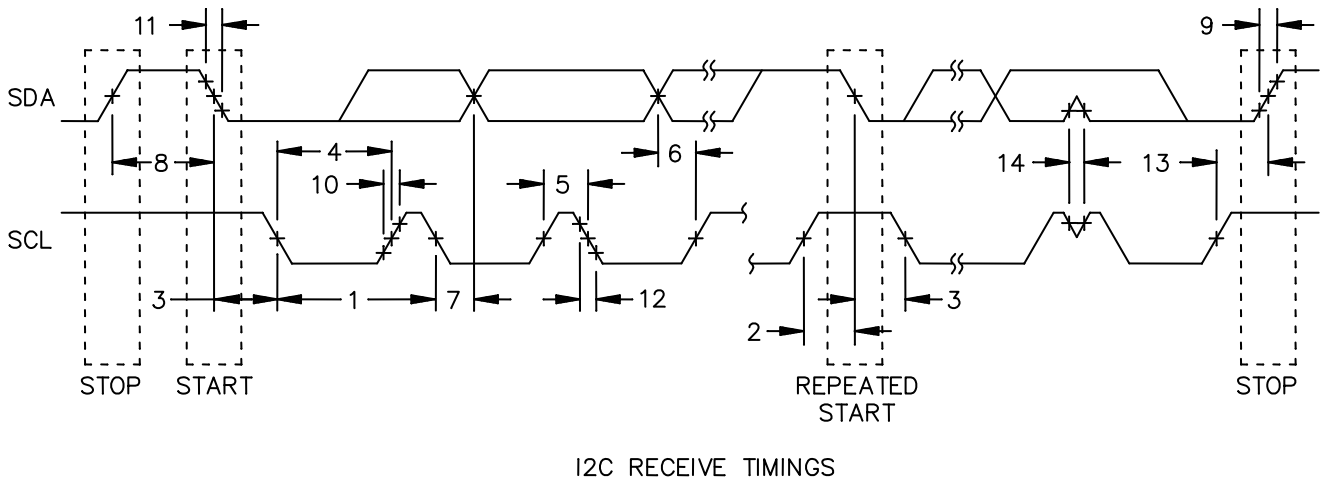


FIGURE 35. Timing waveforms.

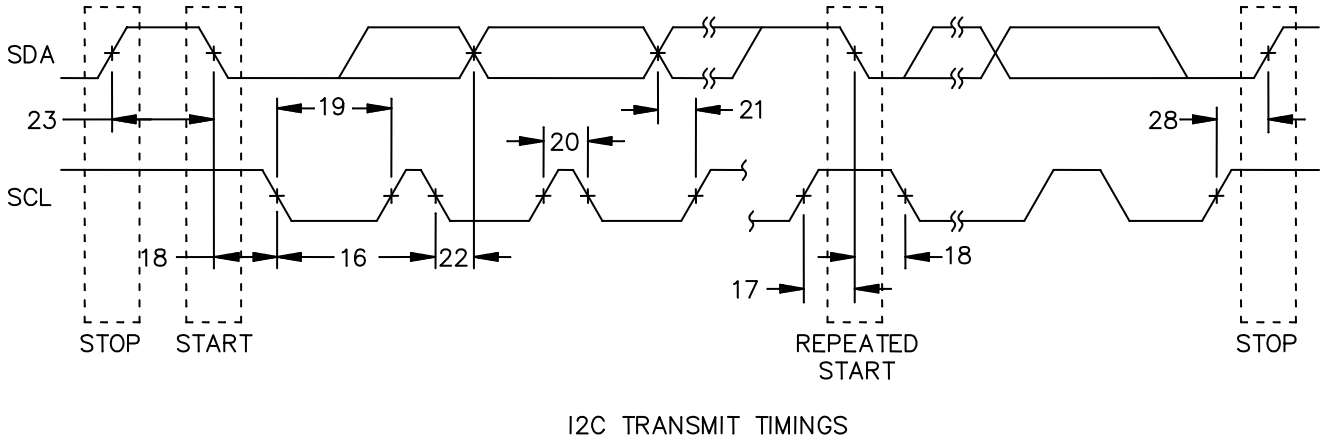


FIGURE 36. Timing waveforms.

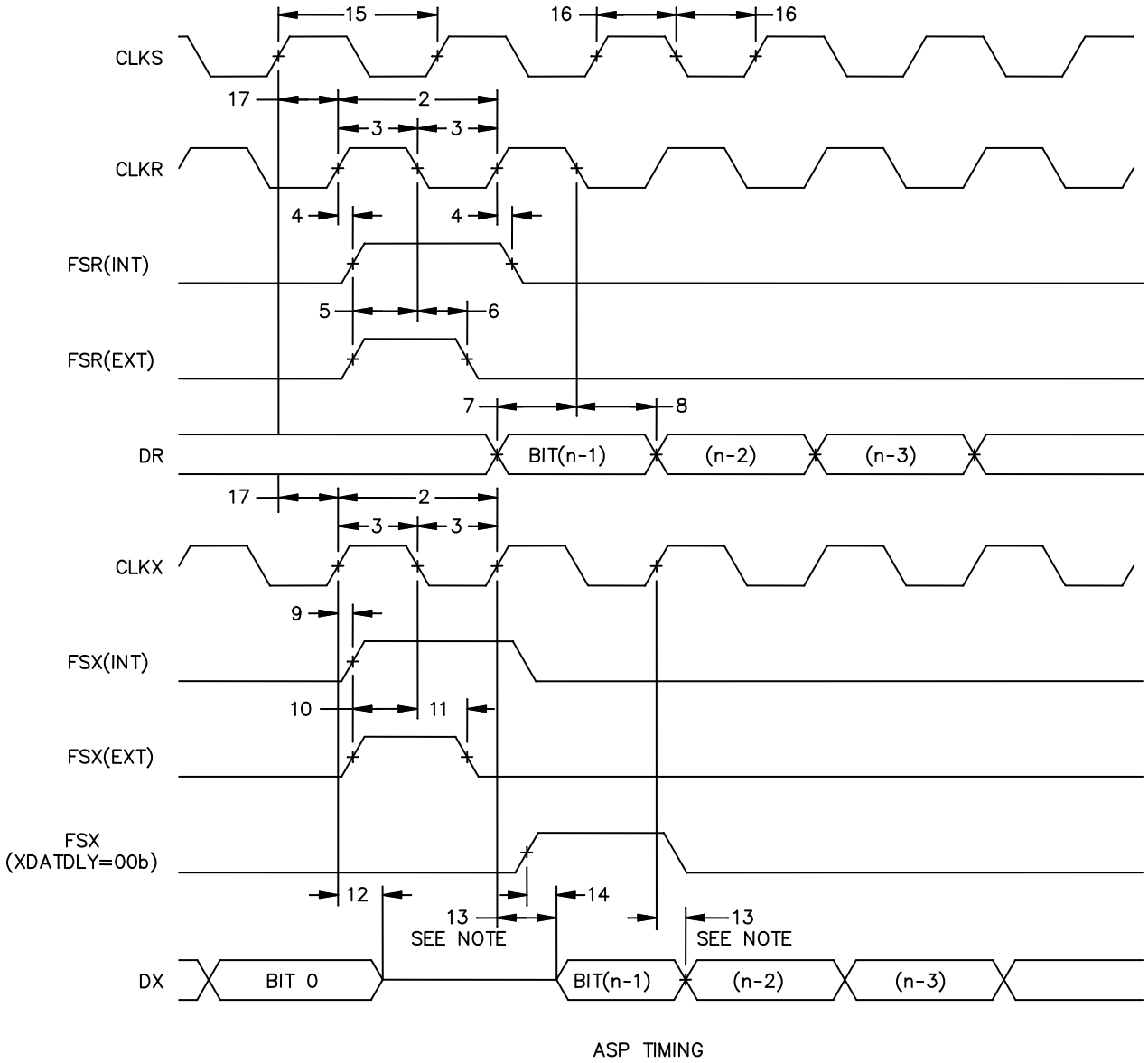
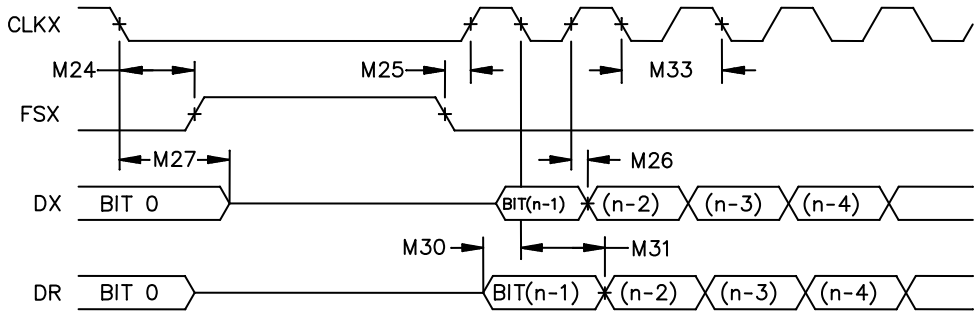
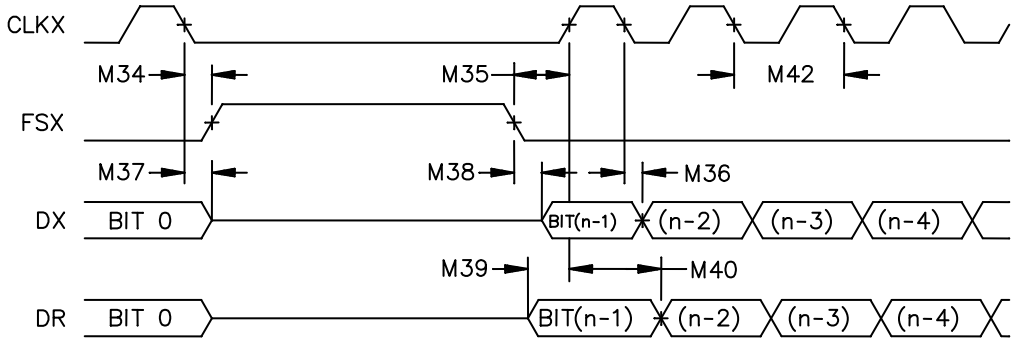


FIGURE 37. Timing waveforms.



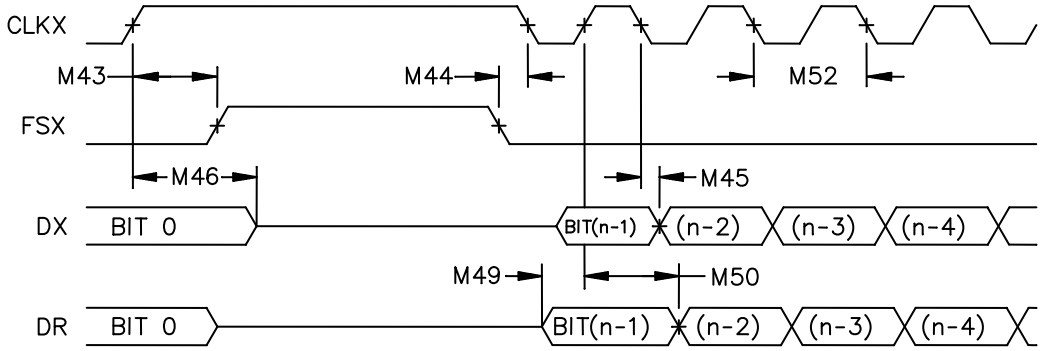
ASP AS SPI: CLKSTP=10b, CLKXP=0

FIGURE 38. Timing waveforms.



ASP AS SPI: CLKSTP=11b, CLKXP=0

FIGURE 39. Timing waveforms.



ASP AS SPI: CLKSTP=10b, CLKXP=1

FIGURE 40. Timing waveforms.

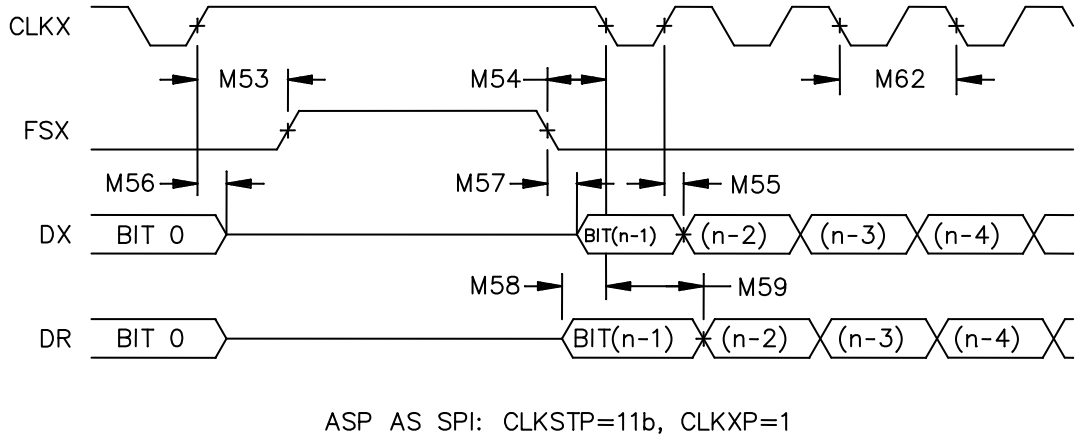


FIGURE 41. Timing waveforms.

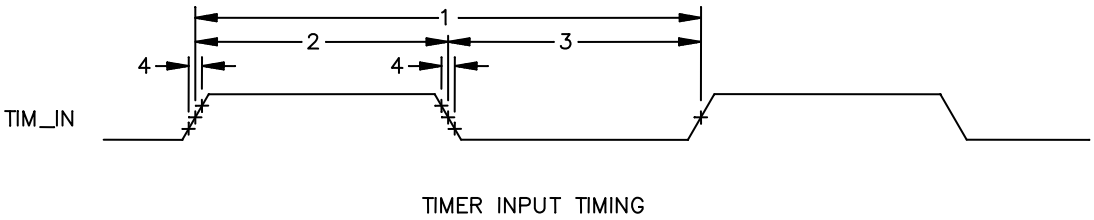


FIGURE 42. Timing waveforms.

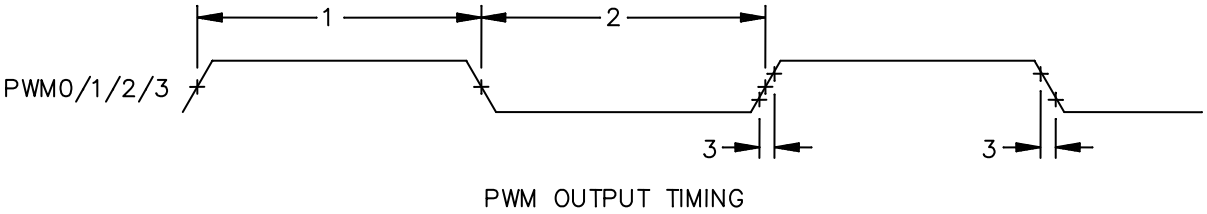
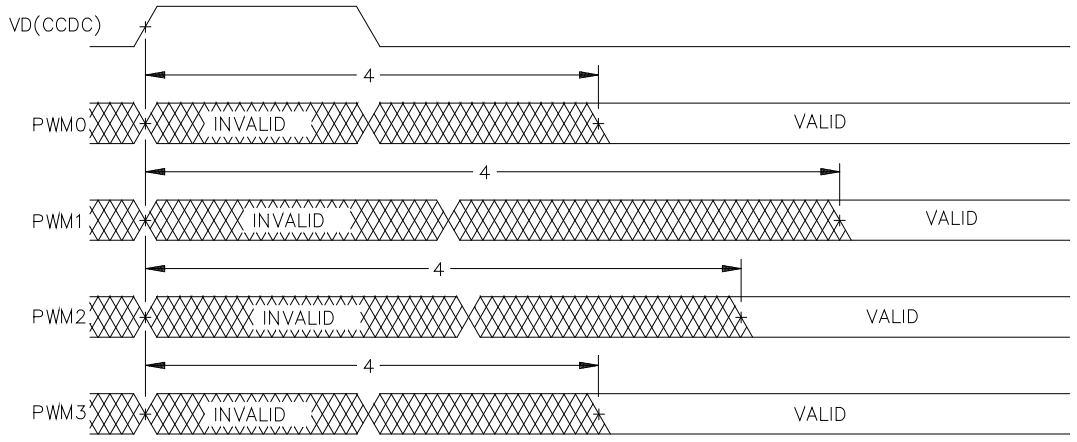
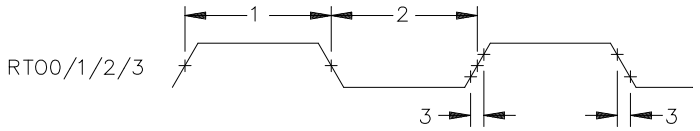


FIGURE 43. Timing waveforms.



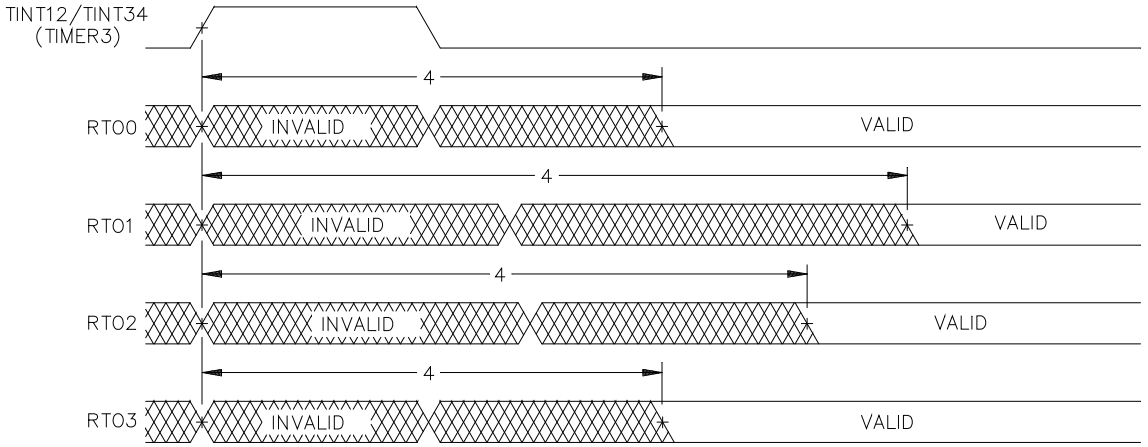
PWM OUTPUT DELAY TIMING

FIGURE 44. Timing waveforms.



RTO OUTPUT TIMING

FIGURE 45. Timing waveforms.



RTO OUTPUT DELAY TIMING

FIGURE 46. Timing waveforms.

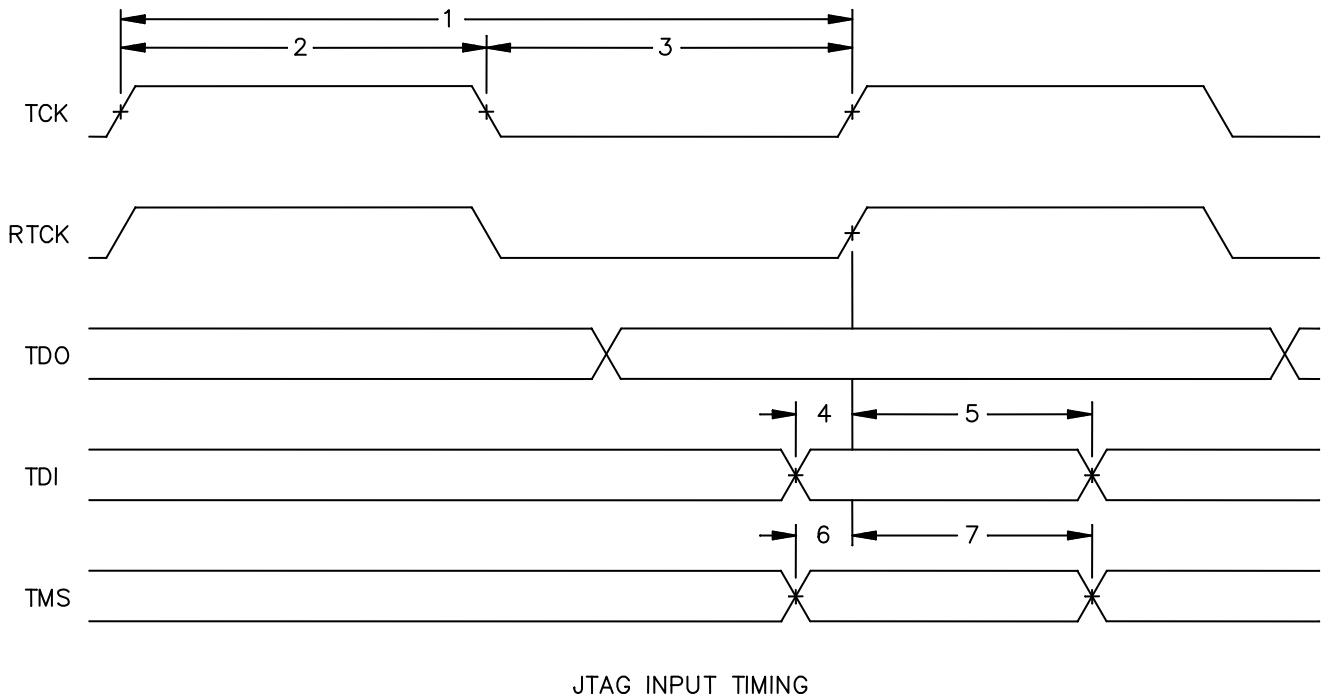


FIGURE 47. Timing waveforms.

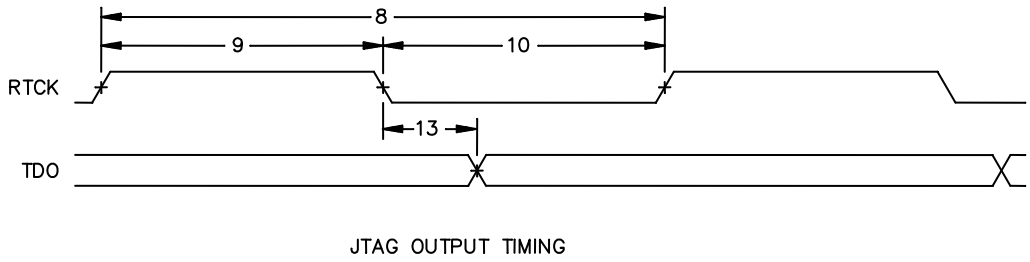


FIGURE 48. Timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/09643-01XE	01295	SM32DM355GCEM216EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493