

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update document paragraphs to current requirements. - ro	17-11-06	C. SAFFLE



Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																				
PAGE																				
REV																				
PAGE																				
REV STATUS OF PAGES	REV	A	A	A	A	A	A	A	A	A	A	A	A							
	PAGE	1	2	3	4	5	6	7	8	9	10									

PMIC N/A	PREPARED BY RICK OFFICER	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 <a href="http://www.dla.mil/landandmaritime">http://www.dla.mil/landandmaritime</a>	
Original date of drawing YY-MM-DD  11-06-29	CHECKED BY RAJESH PITHADIA	TITLE MICROCIRCUIT, LINEAR, CMOS, MICROPOWER, STEP UP SWITCHING VOLTAGE REGULATOR, MONOLITHIC SILICON	
	APPROVED BY CHARLES F. SAFFLE		
	SIZE A	CODE IDENT. NO. 16236	DWG NO. <b>V62/09637</b>
	REV A		PAGE 1 OF 10

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a CMOS micropower, step up switching voltage regulator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/09637</u>   Drawing number	-	<u>01</u>   Device type (See 1.2.1)	<u>X</u>   Case outline (See 1.2.2)	<u>B</u>   Lead finish (See 1.2.3)
--	---	--	--	---

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	MAX630	CMOS micropower, step up switching voltage regulator

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	8	MS-012-AA	Small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/09637</b>
		REV    A	PAGE    2

1.3 Absolute maximum ratings. 1/

Supply voltage (VS) .....	18 V
Input voltage (LBR, CX, IC, VFB pins) .....	-0.3 V to (+VS + 0.3 V)
Output voltage, LX and LBD .....	18 V
LX output current .....	525 mA (peak)
LBD output current .....	50 mA
Power dissipation (PD) .....	441 mW 2/
Junction temperature range (TJ) .....	150°C
Storage temperature range (TSTG) .....	-65°C to +160°C
Lead temperature (soldering, 10 seconds) .....	+300°C
Electrostatic discharge (ESD):	
Human body model (HBM) .....	2,000 V
Moisture sensitivity level (MSL) .....	Level 1

1.4 Recommended operating conditions. 3/

Supply voltage (VS) .....	+6.0 V
Operating free-air temperature range (TA) .....	-55°C to +125°C

1.5 Thermal data table.

Case outline letter	X	X	Units
PC board	Single layer	Multi-layer 4/	
Power dissipation (Pd), maximum at +70°C	471	606	mW
Power dissipation (Pd) derating above +70°C	5.9	7.6	mW/°C
Thermal resistance, junction to case (θJC)	40	38	°C/W
Thermal resistance, junction to ambient (θJA)	170	132	°C/W

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Derate 5.88 mW/°C above +50°C.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

4/ Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, contact the manufacturer.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/09637</b>
		REV A	PAGE 3

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

- JEDEC 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at <https://www.jedec.org>)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/09637</b>
		REV    A	PAGE    4

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions +VS = +6.0 V, IC = 5.0 $\mu$ A unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Supply voltage	+VS	Operating	+25°C	01	2.0	16.5	V
		Startup			1.9		
			-55°C to +125°C		2.2	16.5	
Internal reference voltage	VREF		+25°C	01	1.29	1.33	V
			-55°C to +125°C		1.25	1.37	
Switch current	ISW	V <sub>3</sub> = 400 mV	+25°C	01	75		mA
Supply current at +VS pin	IS	I <sub>3</sub> = 0 mA	+25°C	01		125	$\mu$ A
			-55°C to +125°C			200	
Efficiency			+25°C	01	85 typical		%
Line regulation		0.5 V <sub>OUT</sub> < V <sub>S</sub> < V <sub>OUT</sub> 2/	+25°C	01		0.2	%V <sub>OUT</sub>
			-55°C to +125°C			0.5	
Load regulation		V <sub>S</sub> = +5 V, P <sub>L</sub> = 0 to 150 mW 2/	+25°C	01		0.5	%V <sub>OUT</sub>
		V <sub>S</sub> = 0.5V <sub>O</sub> , P <sub>L</sub> = 0 to 150 mW 2/	-55°C to +125°C			1.0	
Operating frequency range	F <sub>O</sub>	3/	+25°C	01	0.1	75	kHz
Reference set internal pulldown resistance	RIC	V <sub>6</sub> = V <sub>S</sub>	+25°C	01	0.5	10	M $\Omega$
			-55°C to +125°C		0.3	10	
Reference set input voltage threshold	VIC		-55°C to +125°C	01	0.2	1.3	V
Switch current	ISW	V <sub>3</sub> = 1.0 V	+25°C	01	100		mA
Switch leakage current	ICO	V <sub>3</sub> = 16.5 V	+25°C	01		1.0	$\mu$ A
			-55°C to +125°C			30	
Supply current (shutdown)	ISO	I <sub>C</sub> < 0.01 $\mu$ A	+25°C	01		1.0	$\mu$ A
			-55°C to +125°C			10	

See footnotes at end of table.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/09637</b>
		<b>REV    A</b>	<b>PAGE    5</b>

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions +VS = +6.0 V, IC = 5.0 μA unless otherwise specified	Temperature, TA	Device type	Limits		Unit
					Min	Max	
Low battery bias current	ILBR		+25°C	01		10	nA
Capacitor charging current	ICX		+25°C	01	30 typical		μA
CX+ threshold voltage			+25°C	01	+VS – 0.1 typical		V
CX- threshold voltage			+25°C	01	0.1 typical		V
VFB input bias current	IFB		+25°C	01		10	nA
Low battery detector output current	ILBD	V <sub>8</sub> = 0.4 V, V <sub>1</sub> = 1.1 V	-55°C to +125°C	01	250		μA
Low battery detector output leakage	ILBDO	V <sub>8</sub> = 16.5 V, V <sub>1</sub> = 1.4 V	+25°C	01		5.0	μA

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Guaranteed by correlation with DC pulse measurements.

3/ The operating frequency range is guaranteed by design and verified with sample testing.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/09637</b>
		<b>REV     A</b>	<b>PAGE    6</b>

Case X

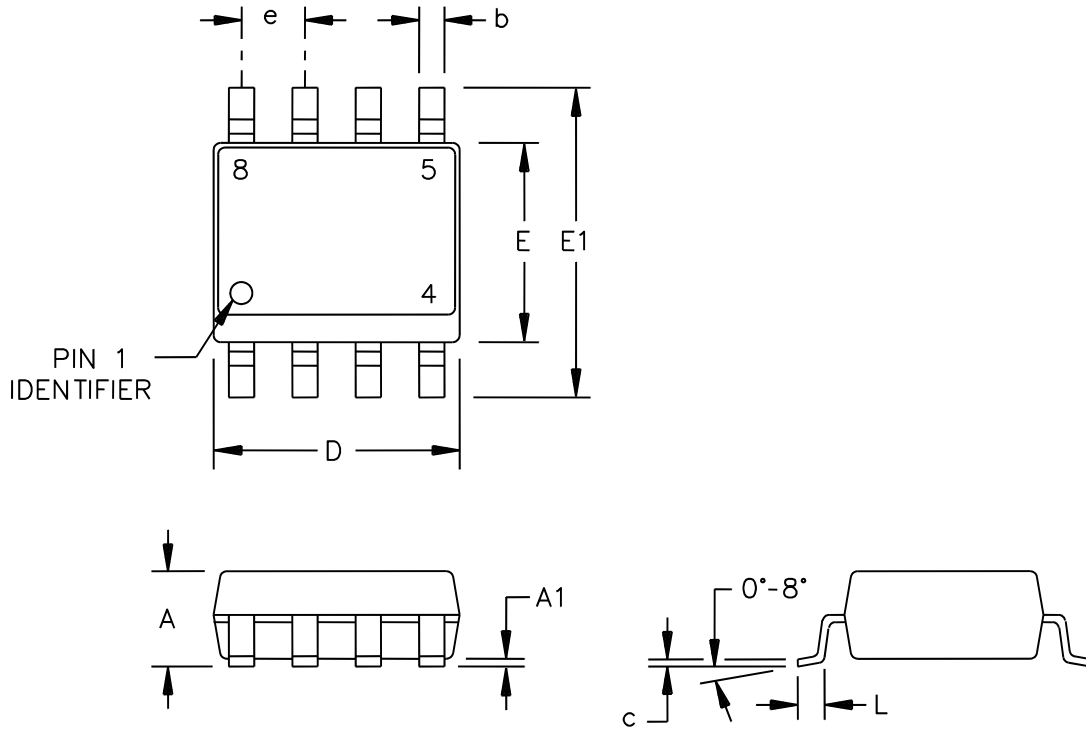


FIGURE 1. Case outline.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/09637</b>
		REV A	PAGE 7

Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
b	0.014	0.019	0.35	0.49
c	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
E1	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
n	8		8	

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Dimensions D and E do not include mold flash.
3. Mold flash or protrusions do not exceed 0.15 mm (0.006 inch).
4. Leads to be coplanar within 0.10 mm (.004 inch).
5. Falls within reference to JEDEC MS-012-AA.

FIGURE 1. Case outline - Continued.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/09637</b>
		REV A	PAGE 8



Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	LBR	Low battery detection comparator input. The LBD output, pin 8, sinks current whenever this pin is below the low battery detector threshold, typically 1.31 V
2	CX	An external capacitor connected between this terminal and ground sets the oscillator frequency. 47 pF = 40 kHz.
3	LX	This pin drives the external inductor. The internal N-channel metal oxide semiconductor field effect transistor (MOSFET) that drives LX has an output resistance of 4 $\Omega$ and a peak current rating of 525 mA.
4	GND	Ground.
5	+VS	The positive supply voltage, from 2.0 V to 16.5 V.
6	IC	The device will shut down when this pin is left floating or is driven below 0.2 V. For normal operation, connect IC directly to +VS or drive it high with either a CMOS gate or pullup resistor connected to +VS. The supply current is typically 10 nA in the shutdown mode.
7	VFB	The output voltage is set by an external resistive divider connected from the converter output to VFB and ground. The device will pulse the LX output whenever the voltage at this terminal is less than 1.31 V.
8	LBD	The low battery detector output is an open-drain N-channel MOSFET that sinks up to 600 $\mu$ A (typical) whenever the LBR input, pin 1, is below 1.31 V.

FIGURE 2. Terminal connections.

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/09637</b>
		REV A	PAGE 9

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number <u>2/</u>
V62/09637-01XB	1ES66	MAX630MSA/PR

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ Add "-T" suffix for tape and reel.

CAGE code

1ES66

Source of supply

Maxim Integrated  
160 Rio Robles  
San Jose, CA 95134

<b>DLA LAND AND MARITIME COLUMBUS, OHIO</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/09637</b>
		REV A	PAGE 10