REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**
Original date of drawing YY MM DD 11-07-14	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, DIGITAL, ,LOW VOLTAGE, QUAD, SPDT, CMOS ANALOG SWITCH, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/09636**
	REV	**PAGE** 1 **OF** 13

AMSC N/A

5962-V059-11

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low voltage, quad, SPDT, CMOS analog switch microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/09636	-	01	X	B
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	MAX394	Low voltage, quad, SPDT CMOS analog switch

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	JEDEC MS012	Small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Voltage referenced to GND:
- V+ ..... -0.3 V to +17 V
- V- ..... +0.3 V to -17 V
- V+ to V- ..... -0.3 V to +17 V

COM_, NO_, NC_, IN_ ..... (V- - 2 V) to (V+ + 2 V) or 30 mA, which ever occurs first 2/
Continuous current, any pin ..... 30 mA
Peak current, any pin (pulsed at 1 ms, 10% duty cycle max) ..... 100 mA
Continuous power dissipation (T_A = +70°C)
- Case X (derate 8.70 mW/°C above +70°C) ..... 696 mW

Operating temperature range ..... -55°C to +125°C
Storage temperature range ..... -65°C to 150°C
Lead temperature (soldering , 10 sec) ..... +300°C
Electro Static Discharge (ESD)
- Human Body Model (HBM) ..... 2500 V
- Class 2

Moisture Sensitive Level (MSL) ..... Level 1

1.4 Thermal data table.

Case outline letter	X	X	Units
PC Board	Single Layer	Multi-Layer 3/	
Power dissipation (P_D), maximum at +70°C	800	1194	mW
Power dissipation (P_D) derating above +70°C	10	14.9	mW/°C
Thermal resistance, junction to case (θ_{JC})	20	23	°C/W
Thermal resistance, junction to ambient (θ_{JA})	100	67	°C/W

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
JEDEC STD 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ Signals on NC, NO, COM, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current ratings.
3/ Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to manufacturer data.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional diagram. The functional diagram shall be as shown in figure 3.

3.5.4 Switching time test circuit. The switching time and test circuit shall be as shown in figure 4.

3.5.5 Channel capacitance. The channel capacitance shall be as shown in figure 5.

3.5.6 Break before make delay. The break before make delay shall be as shown in figure 6.

3.5.7 Charge injection. The charge injection shall be as shown in figure 7.

3.5.8 Off isolation. The off isolation shall be as shown in figure 8.

3.5.9 Cross talk test circuit. The cross test circuit shall be as shown in figure 9.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	T_A	Limits 3/		Unit
				Min	Max	
DUAL SUPPLIES						
Switch						
Analog signal range	V_{COM}, V_{NO}, V_{NC}	4/		0	V+	V
On resistance	R_{ON}	V+ = 4.5 V, V- = -4.5 V, V_{NC} or V_{NO} = ±3.5 V, I_{COM} = 10 mA V_{INH} = 2.4 V, V_{INL} = 0.8 V	25°C		30	Ω
			-55°C to 125°C		45	
On resistance matching between channels 5/	ΔR_{ON}	V_{NC} or V_{NO} = ±3 V, I_{COM} = 10 mA V+ = 5 V, V- = -5 V	25°C		2	Ω
			-55°C to 125°C		4	
On resistance flatness 5/	$R_{FLAT(ON)}$	V_{NC} or V_{NO} = 3 V, 0 V, -3 V I_{COM} = 10 Ma, V+ = 5 V, V- = -5 V	25°C		4	Ω
			-55°C to 125°C		6	
NC or NO off leakage current 6/	$I_{NC(OFF)}$ or $I_{NO(OFF)}$	V_{COM} = ±4.5 V, V_{NC} or V_{NO} = ±4.5 V V+ = 5.5 V, V- = -5.5 V	25°C	-0.1	+0.1	nA
			-55°C to 125°C	-20	+20	
COM leakage current 6/	$I_{COM(ON)}$	V_{COM} = ±4.5 V, V_{NC} or V_{NO} = ±4.5 V V+ = 5.5 V, V- = -5.5 V	25°C	-0.2	+0.2	nA
			-55°C to 125°C	-20	+20	
Digital logic input						
Input current with input voltage high	I_{INH}	V_{IN} = 2.4 V, all others = 0.8 V		-1.0	+1.0	µA
Input current with input voltage low	I_{INL}	V_{IN} = 0.8 V, all others = 2.4 V		-1.0	+1.0	µA
Logic high input voltage	V_{A_H}		-55°C to 125°C	2.4		V
Logic low input voltage	V_{A_L}		-55°C to 125°C		0.8	V
Dynamic						
Turn ON time	t_{ON}	V_{COM} = 3 V See figure 4	25°C		130	ns
			-55°C to 125°C		175	
Turn OFF time	t_{OFF}	V_{COM} = 3 V See figure 4	25°C		75	
			-55°C to 125°C		100	
Break before make time delay 4/	t_D	See figure 6	25°C	2		ns
Charge injection 4/	V_{CTE}	C_L = 1.0 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω, See figure 7	25°C		10	pC
Off isolation 7/	V_{ISO}	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz See figure 5	25°C	66 TYP		dB
Cross talk 8/	V_{CT}	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz See figure 9	25°C	88 TYP		dB
Off capacitance	C_{OFF}	f = 1 MHz, See figure 5	25°C	12 TYP		pF
COM Off capacitance	$C_{COM(OFF)}$	f = 1 MHz, See figure 5	25°C	12 TYP		
Channel On capacitance	$C_{COM(ON)}$	f = 1 MHz, See figure 5	25°C	39 TYP		
Supply						
Power supply range				±2.4	±8	V
Positive supply current	I+	All channels on or off, V+ = 5.5 V, V- = -5.5 V, V_{IN} = 0 V or V+		-1.0	+1.0	µA
Negative supply current	I-			-1.0	+1.0	

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 10/	T_A	Limits 3/		Unit
				Min	Max	
SINGLE +5 V SUPPLY						
Switch						
Analog signal range	V_{COM}, V_{NO}, V_{NC}	4/		0	V+	V
On resistance	R_{ON}	V+ = 5.0 V, V- = 0 V, V_{NC} or V_{NO} = 3.5 V, I_{COM} = 1.0 mA V_{INH} = 2.4 V, V_{INL} = 0.8 V	25°C		60	Ω
			-55°C to 125°C		75	
On resistance match between channels 5/	ΔR_{ON}	V_{NC} or V_{NO} = 3 V, I_{COM} = 1.0 mA V+ = 5 V	25°C		2	Ω
			-55°C to 125°C		4	
On resistance flatness 5/	$R_{FLAT(ON)}$	V_{NC} or V_{NO} = 3 V, 2 V, 1 V, I_{COM} = 1.0 mA, V+ = 5 V, V- = 0 V	25°C		6	Ω
			-55°C to 125°C		8	
NC or NO off leakage current 9/	$I_{NC(OFF)}$ or $I_{NO(OFF)}$	V_{COM} = 0 V, V_{NC} or V_{NO} = 4.5 V V+ = 5.5 V, V- = 0 V	25°C	-0.1	+0.1	nA
			-55°C to 125°C	-20	+20	
COM leakage current 9/	$I_{COM(ON)}$	V_{COM} = 4.5 V, V_{NC} or V_{NO} = 4.5 V V+ = 5.5 V, V- = 0 V	25°C	-0.2	+0.2	nA
			-55°C to 125°C	-20	+20	
Digital logic input						
Input current with input voltage high	I_{INH}	V_{IN} = 2.4 V, all others = 0.8 V		-1.0	+1.0	µA
Input current with input voltage low	I_{INL}	V_{IN} = 0.8 V, all others = 2.4 V		-1.0	+1.0	µA
Dynamic						
Turn ON time	t_{ON}	V_{COM} = 3 V See figure 4	25°C		250	ns
			-55°C to 125°C		300	
Turn OFF time	t_{OFF}	V_{COM} = 3 V See figure 4	25°C		125	
			-55°C to 125°C		175	
Break before make time delay 4/	t_D		25°C	5		ns
Charge injection 4/	V_{CTE}	C_L = 1.0 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω,	25°C		5	pC
Supply						
Power supply range	V+			2.4	16	V
Positive supply current	I+	All channels on or off, V_{IN} = 0 V or V+ V+ = 5.5 V, V- = 0 V		-1.0	+1.0	µA
Negative supply current	I-			-1.0	+1.0	

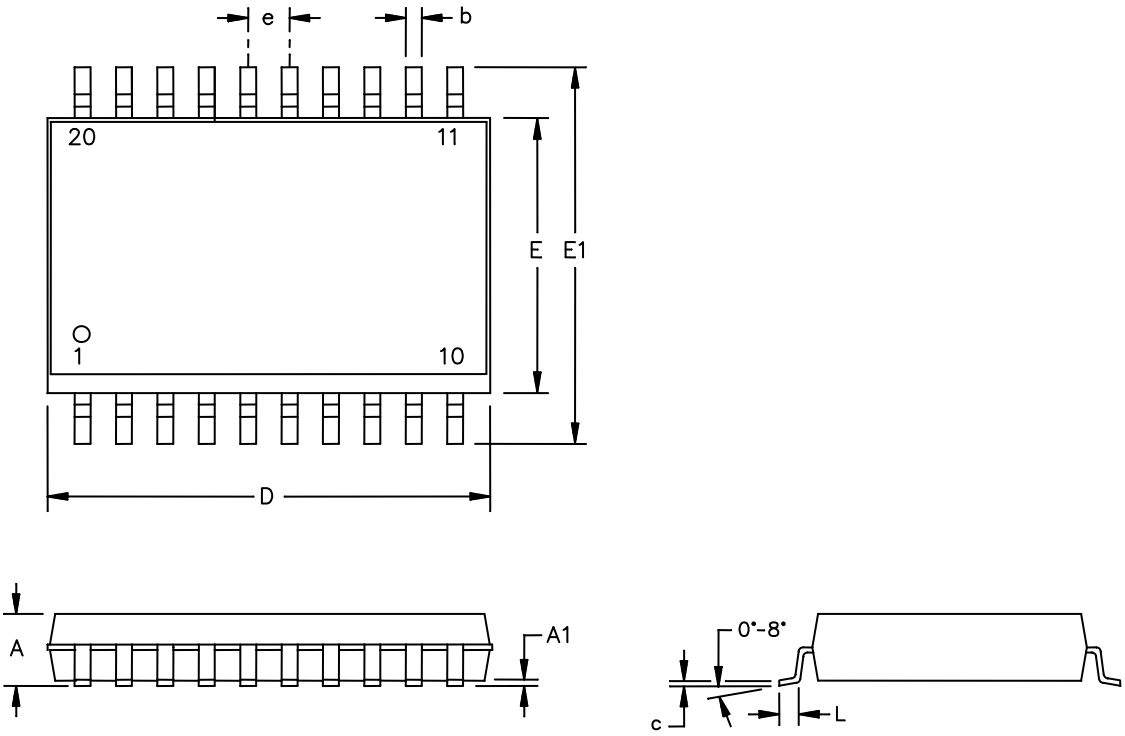
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 11/	T_A	Limits 3/		Unit
				Min	Max	
SINGLE +3.3 V SUPPLY						
Switch						
Analog signal range	V_{COM}, V_{NO}, V_{NC}	4/		0	V+	V
On resistance	R_{ON}	V+ = 3 V, V- = 0 V, V_{NC} or V_{NO} = 1.5 V, I_{COM} = 1.0 mA V_{INH} = 2.4 V, V_{INL} = 0.8 V	25°C		175	Ω
			-55°C to 125°C		250	
NC or NO off leakage current 9/	$I_{NC(OFF)}$ or $I_{NO(OFF)}$	V_{COM} = 0 V, V_{NC} or V_{NO} = 3 V V+ = 3.6 V, V- = 0 V	25°C	-0.1	+0.1	nA
			-55°C to 125°C	-5.0	+5.0	
COM leakage current 9/	$I_{COM(ON)}$	V_{COM} = 3 V, V_{NC} or V_{NO} = 3 V V+ = 3.6 V, V- = 0 V	25°C	-0.2	+0.2	nA
			-55°C to 125°C	-20	+20	
Digital logic input						
Input current with input voltage high	I_{INH}	V_{IN} = 2.4 V, all others = 0.8 V		-1.0	+1.0	µA
Input current with input voltage low	I_{INL}	V_{IN} = 0.8 V, all others = 2.4 V		-1.0	+1.0	µA
Dynamic						
Turn ON time 4/	t_{ON}	V_{COM} = 1.5 V, See figure 4	25°C		400	ns
Turn OFF time 4/	t_{OFF}	V_{COM} = 1.5 V, See figure 4	25°C		150	
Break before make time delay 4/	t_D	See figure 6	25°C	5		ns
Charge injection 4/	V_{CTE}	C_L = 1.0 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω, See figure 7	25°C		5	pC
Supply						
Power supply range	V+			2.7	16	V
Positive supply current	I+	All channels on or off, V_{IN} = 0 V or V+ V+ = 3.6 V, V- = 0 V		-1.0	+1.0	µA
Negative supply current	I-			-1.0	+1.0	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ V+ = 5 V ±10%, V- = -5 V ±10%, GND = 0 V, V_{INH} = 2.4 V, V_{INL} = 0.8 V, T_A = -55°C to 125°C (unless otherwise noted).
3/ The algebraic convention where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.
4/ Guaranteed by design.
5/ $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$. On resistance match between channels and flatness are guaranteed only with specified voltage. Flatness is defined as the difference between the maximum and minimum value of on resistance as measured at the extremes of the specified analog signal range.
6/ Leakage parameters are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.
7/ See figure 7. Off isolation = $20\log_{10} V_{COM}/V_{NC}$ or V_{NO}, V_{COM} = output, V_{NC} or V_{NO} = input to off switch.
8/ Between any two switches. See figure 5
9/ Leakage testing at single supply is guaranteed by testing with dual supplies.
10/ V+ = 5 V ±10%, V- = -0 V, GND = 0 V, V_{INH} = 2.4 V, V_{INL} = 0.8 V, T_A = -55°C to 125°C (unless otherwise noted).
11/ V+ = 3.0 V to 3.6 V, GND = 0 V, V_{INH} = 2.4 V, V_{INL} = 0.8 V, T_A = -55°C to 125°C (unless otherwise noted).

Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	.093	.104	2.35	2.65	e	.050 BSC		1.27 BSC	
A1	.004	.012	0.10	0.30	E	.291	.299	7.40	7.60
b	.014	.019	0.35	0.49	E1	.394	.419	10.00	10.65
c	.009	.013	0.23	0.32	L	.016	.050	0.40	1.27
D	.496	.512	12.60	13.00					

NOTES:
1. D and E do not include mold flash.
2. Mold flash or protrusions not to exceed 0.15 mm (.006”).
3. Leads to be coplanar within 0.10 mm (.004”).
4. Meets JEDEC MS012.

FIGURE 1. Case outline.

Case outline X			
Device type 01			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	IN1	11	IN3
2	NO1	12	NO3
3	COM1	13	COM3
4	NC1	14	NC3
5	V-	15	N.C.
6	GND	16	V+
7	NC2	17	NC4
8	COM2	18	COM4
9	NO2	19	NO4
10	IN2	20	IN4

N.C. = Not internally connected

FIGURE 2. Terminal connections.

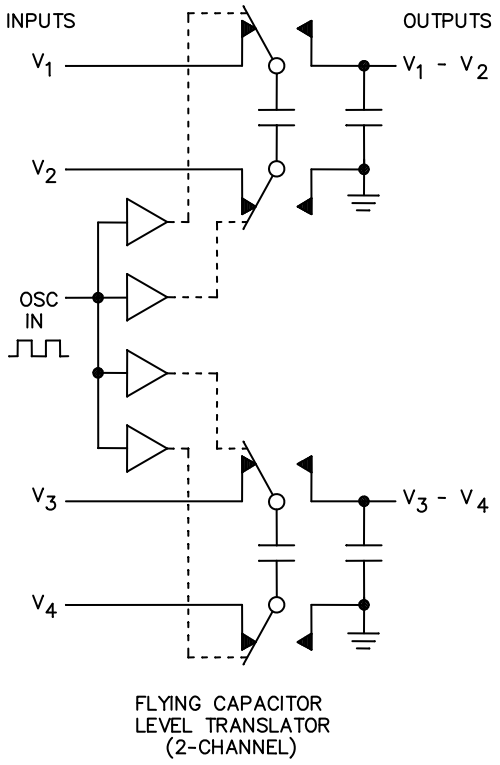


FIGURE 3. Functional diagram.

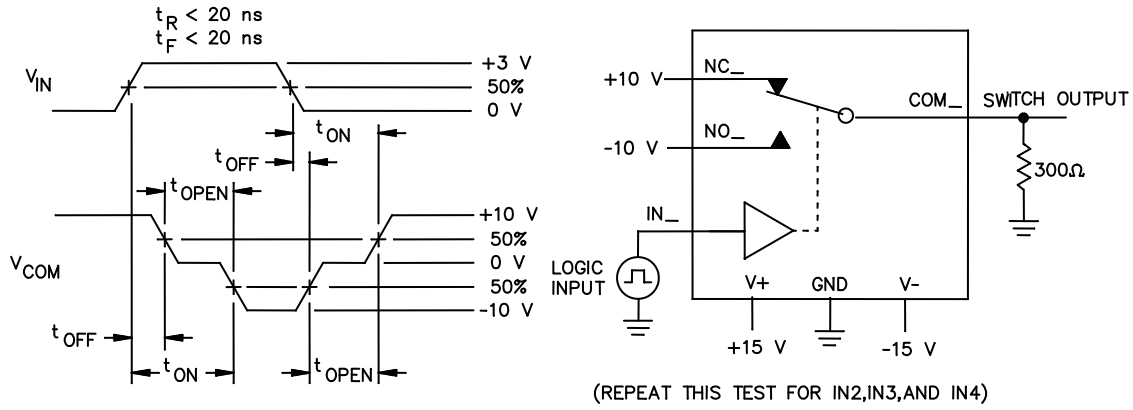


FIGURE 4. Switching time test circuit.

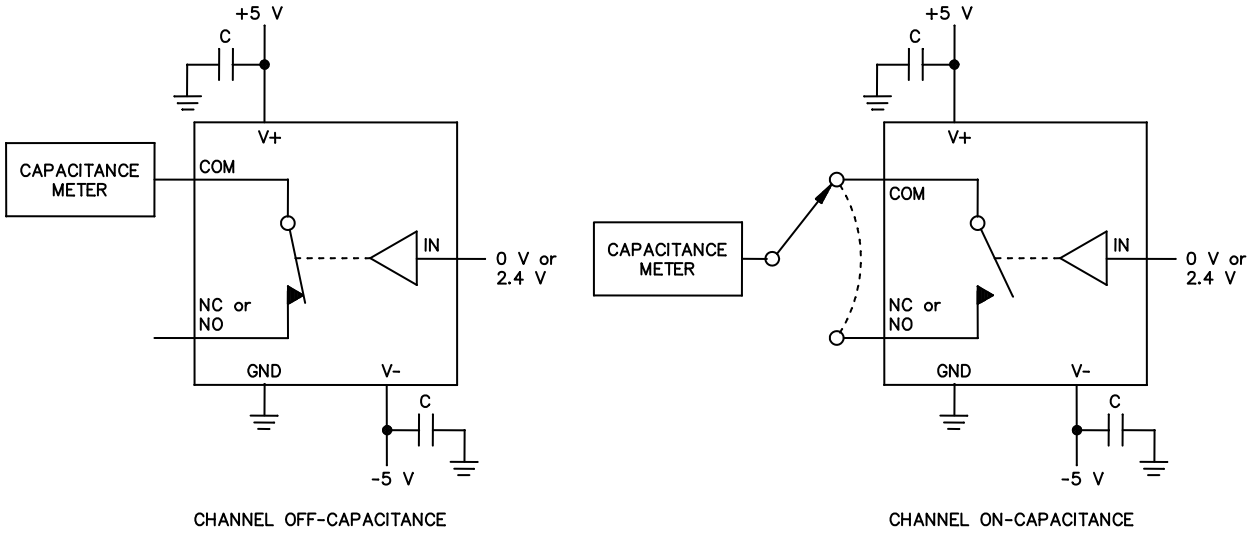


FIGURE 5. Channel capacitance.

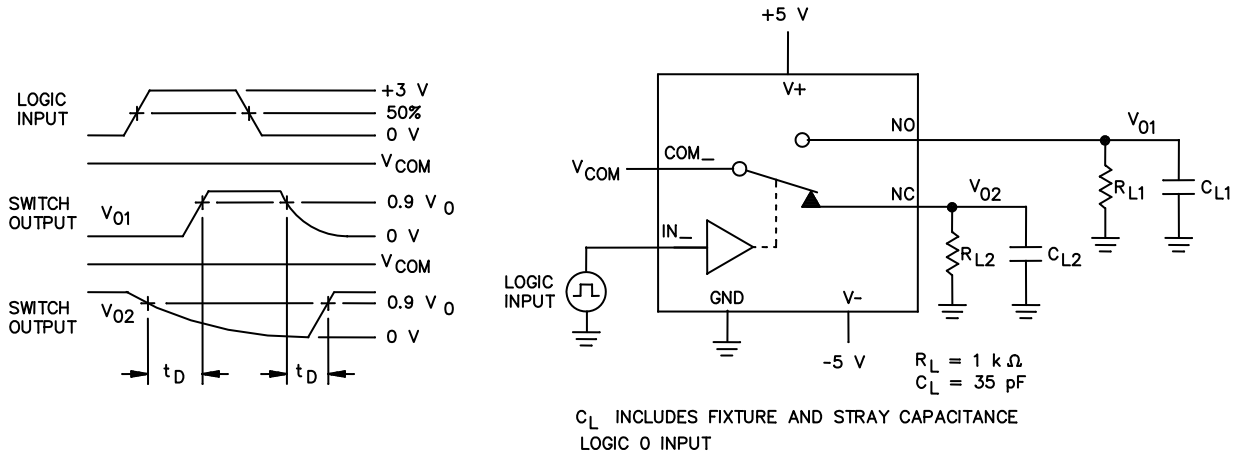


FIGURE 6. Break before make delay.

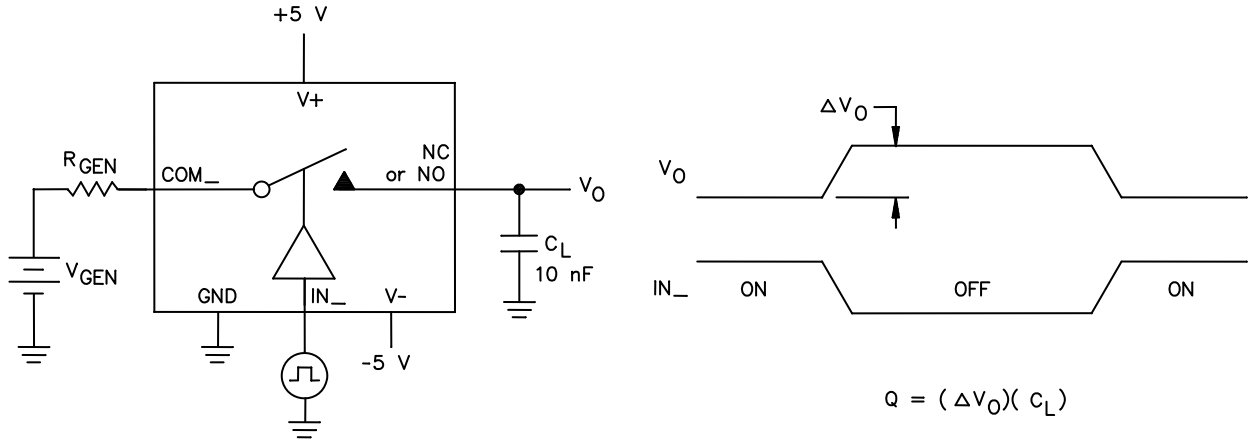


FIGURE 7. Charge injection.

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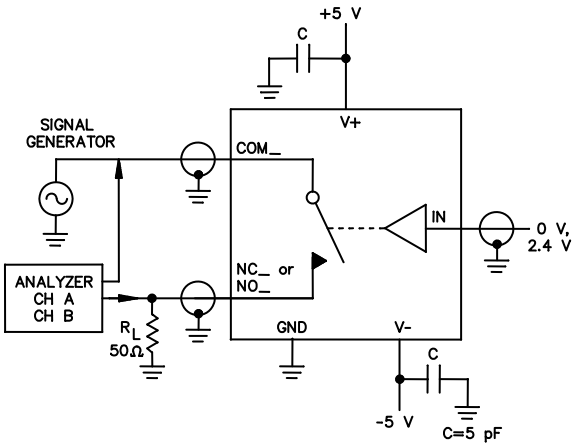
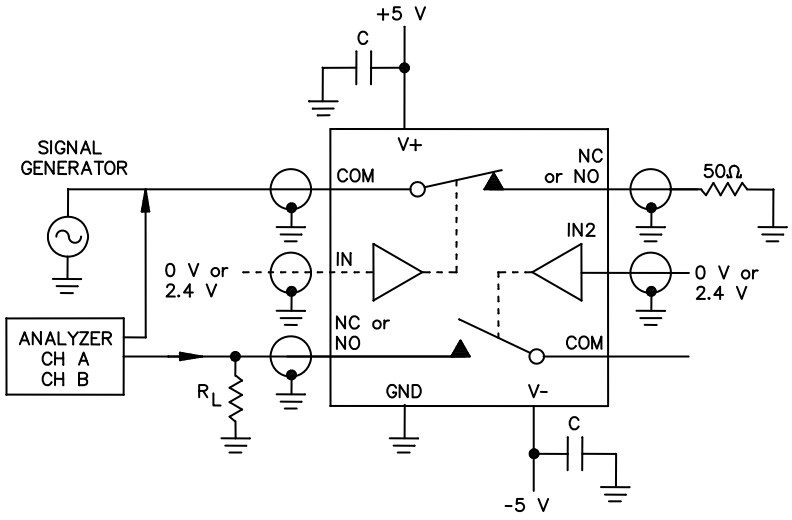


Frequency Tested	Signal generator	Analyzer
1 MHz	Automatic Synthesizer	Tracking spectrum analyzer

$$V_{ISO} = 20 \text{ Log } \frac{V_{COM}}{V_{NC} \text{ or } V_{NO}}$$

FIGURE 8. Off isolation.



Frequency Tested	Signal generator	Analyzer
1 MHz	Automatic Synthesizer	Tracking spectrum analyzer

$$V_{CT} = 20 \text{ Log } \frac{V_{COM}}{V_{NC} \text{ or } V_{NO}}$$

FIGURE 9. Crosstalk test circuit.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	
V62/09636-01XB	1ES66	MAX394MWP/PR	MAX394MWP/PR-T 2/

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ For tape and reel.

CAGE code	Source of supply
1ES66	Maxim Integrated Products 120 San Gabriel Dr Sunnyvale, CA 94086-5125