REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY MM DD 10-03-02	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, MICROPROCESSOR SUPERVISORY CIRCUITS, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/09632**
	REV	**PAGE** 1 **OF** 12

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a microprocessor supervisory circuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/09632	-	01	X	B
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	MAX691A	Microprocessor supervisory circuits

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	JEDEC MS012	Small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Terminal voltage (with respect to GND)
- V_{CC} ..... -0.3 V to +6.0 V
- V_{BATT} ..... -0.3 V to +6.0 V
- All other inputs ..... -0.3 V to (V_{OUT} + 0.3 V)

Input current:
- V_{CC} peak ..... 1.0 A
- V_{CC} continuous ..... 250 mA
- V_{BATT} peak ..... 250 mA
- V_{BATT} continuous ..... 25 mA
- GND, BATT ON ..... 100 mA
- All other outputs ..... 25 mA

Junction temperature (T_J) ..... 150°C
Operating temperature range ..... -55°C to +125°C
Storage temperature range ..... -65°C to 150°C
Lead temperature (soldering , 10 sec) ..... +300°C
Electro Static Discharge (ESD)
- Human Body Model (HBM) ..... 2000 V
- Class 1C

Moisture Sensitivity Level (MSL) ..... Level 1

1.4 Thermal data table. 2/

Case outline letter	X	X	Units
PC Board	Single Layer	Multi-Layer 2/	
Power dissipation (P_D), maximum at +70°C	696	1067	mW
Power dissipation (P_D) derating above +70°C	8.7	13.3	mW/°C
Thermal resistance, junction to case (θ_{JC})	32	24	°C/W
Thermal resistance, junction to ambient (θ_{JA})	115	75	°C/W

2. APPLICABLE DOCUMENTS

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
JESD51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org)

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to manufacturer’s website.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

3.5.4 Reset and chip enable timing. The reset and chip enable timing shall be as shown in figure 4.

3.5.5 $\overline{CE}$ propagation delay test circuit. The $\overline{CE}$ propagation delay test circuit shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions Device type: All 2/		Limits		Unit
				Min	Max	
Operating voltage range, VCC, VBATT 3/				0	5.5	V
V_{OUT} output		V_{CC} = 4.5 V	I_{OUT} = 25 mA		V_{CC} – 0.05	V
			I_{OUT} = 250 mA		V_{CC} – 0.40	
V_{CC} to V_{OUT} ON resistance		V_{CC} = 4.5 V			1.6	Ω
V_{OUT} in battery-backup mode		VBATT = 4.5 V, I_{OUT} = 20 mA		VBATT – 0.3		V
		VBATT = 2.8 V, I_{OUT} = 10 mA		VBATT – 0.25		
		VBATT = 2.0 V, I_{OUT} = 5 mA		VBATT – 0.15		
VBATT to V_{OUT} ON resistance		VBATT = 4.5 V			15	Ω
		VBATT = 2.8 V			25	
		VBATT = 2.0 V			30	
Supply current in normal operating mode (excludes I_{OUT})		V_{CC} > VBATT – 1 V			100	µA
Supply current in battery backup mode (excludes I_{OUT}) 4/		V_{CC} < VBATT – 1.2 V, VBATT = 2.8 V	T_A = 25°C		1	µA
			T_A = -55°C to +125°C		5	
VBATT standby current 5/		VBATT + 0.2 V ≤ V_{CC}	T_A = 25°C	-0.1	0.02	µA
			T_A = -55°C to +125°C	-1.0	0.02	
Battery switchover threshold		Power up		VBATT + 0.3 TYP		V
		Power down		VBATT – 0.3 TYP		V
Battery switchover hysteresis				60 TYP		mV
BATT ON output low voltage		I_{SINK} = 3.2 mA			0.4	V
		I_{SINK} = 25 mA			1.5	
BATT ON output short circuit current		Sink current		60 TYP		mA
		Source current		1	100	µA
Reset and watchdog timer						
Reset threshold voltage				4.50	4.75	V
Reset threshold hysteresis				15 TYP		mV
V_{CC} to RESET delay		Power down		80 TYP		µs
$\overline{\text{LOWLINE}}$ to $\overline{\text{RESET}}$ delay				800 TYP		ns
Reset active timeout period, internal oscillator		Power-up		140	280	ms
Reset active timeout period , external clock 6/		Power-up		2048 TYP		Clock cycles
Watchdog timeout period, internal oscillator		Long period		1.0	2.25	sec
		Short period		70	140	ms
Watchdog timeout period, external clock 6/		Long period		4096 TYP		Clock cycles
		Short period		1024 TYP		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions Device type: All 2/	Limits		Unit
			Min	Max	
Reset and watchdog timer – (continued)					
Minimum watchdog input pulse width		V_{IL} = 0.8 V, V_{IH} = 0.75 x V_{CC}	100		ns
$\overline{\text{RESET}}$ output voltage		I_{SINK} = 50 µA, V_{CC} = 1 V, VBATT = 0 V, V_{CC} falling		0.3	V
		I_{SINK} = 3.2 mA, V_{CC} = 4.25 V		0.4	
		I_{SOURCE} = 1.6 mA, V_{CC} = 5 V	3.5		
$\overline{\text{RESET}}$ output short circuit current		Output source current		20	mA
RESET output voltage low 7/		I_{SINK} = 3.2 mA	0.1		V
$\overline{\text{LOWLINE}}$ output voltage		I_{SINK} = 3.2 mA, V_{CC} = 4.25 V		0.4	V
		I_{SOURCE} = 1 µA, V_{CC} = 5 V	3.5		
$\overline{\text{LOWLINE}}$ output short circuit current		Output source current	1	100	µA
$\overline{\text{WDO}}$ output voltage		I_{SINK} = 3.2 mA,		0.4	V
		I_{SOURCE} = 500 µA, V_{CC} = 5 V	3.5		
$\overline{\text{WDO}}$ output short circuit current		Output source current		10	mA
WDI threshold voltage 8/		V_{IH}	0.75 x V_{CC}		V
		V_{IL}		0.8	
WDI input current		WDI = 0 V	-50		µA
		WDI = V_{OUT}		50	
Power fail comparator					
PFI input threshold		V_{CC} = 5 V	1.2	1.3	V
PFI leakage current				±25	nA
$\overline{\text{PFO}}$ output voltage		I_{SINK} = 3.2 mA		0.4	V
		I_{SOURCE} = 1 µA, V_{CC} = 5 V	3.5		
$\overline{\text{PFO}}$ output short circuit current		Output source current	1	100	µA
PFI to $\overline{\text{PFO}}$ delay		V_{IN} = -20 mV, V_{OD} = 15 mV	25 TYP		µs
		V_{IN} = 20 mV, V_{OD} = 15 mV	60 TYP		
Chip enable gating					
$\overline{\text{CE}}$ IN leakage current		Disable mode		±1	µA
$\overline{\text{CE}}$ IN to $\overline{\text{CE}}$ OUT resistance 9/		Enable mode		150	Ω
$\overline{\text{CE}}$ OUT short circuit current (Reset active)		Disable mode, $\overline{\text{CE}}$ OUT = 0 V	0.1	2.0	mA
$\overline{\text{CE}}$ IN to $\overline{\text{CE}}$ OUT propagation delay 10/		50 Ω source impedance driver, C_{LOAD} = 50 pF		10	ns
$\overline{\text{CE}}$ OUT output voltage high (Reset active)		V_{CC} = 5 V, I_{OUT} = -100 µA	3.5		V
		V_{CC} = 0 V, VBATT = 2.8 V, I_{OUT} = 1 µA	2.7		
RESET to $\overline{\text{CE}}$ OUT delay		Power down	12 TYP		µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions Device type: All 2/	Limits		Unit
			Min	Max	
Internal oscillator					
OSC IN leakage current		OSC SEL = 0 V		±5	µA
OSC IN input pullup current		OSC SEL = VOUT or floating, OSC IN = 0 V		100	µA
OSC SEL input pullup current		OSC SEL = 0 V		100	µA
OSC IN frequency range		OSC SEL = 0 V	50 TYP		kHz
OSC IN external oscillator threshold voltage		V_{IH}	V_{OUT} – 0.3		V
		V_{IL}		2.0	
OSC Infrequency with external capacitor		OSC SEL = 0 V, C_{OSC} = 47 pF	100 TYP		kHz

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ V_{CC} = +4.75 V to +5.5 V, VBATT = 2.8 V, T_A = -55°C to 125°C (unless otherwise noted).

3/ Either V_{CC} or VBATT can go to 0 V, if the other is greater than 2.0 V.

4/ The supply current drawn by this device from the battery excluding I_{OUT} typically goes to 10 µA when: (VBATT – 1 V) < V_{CC} < VBATT. In most applications, this is a brief period as V_{CC} falls through this region.

5/ "+" = battery discharging current, "-" = battery charging current.

6/ Although presented as typical values, the number of clock cycles for the reset and watchdog timeout periods are fixed and do not vary with process or temperature.

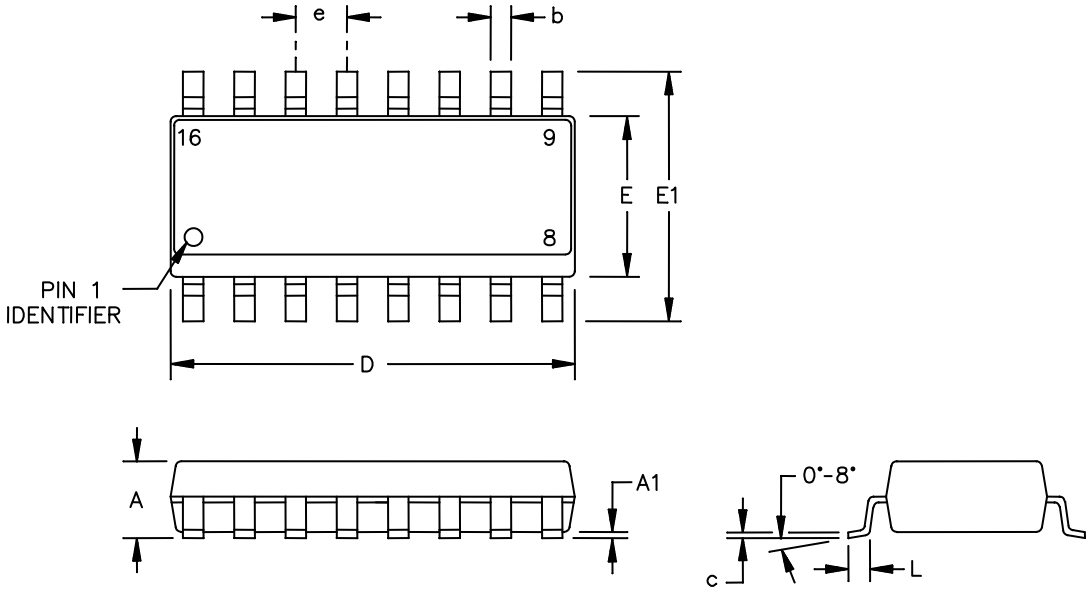
7/ RESET is an open drain output and sinks current only.

8/ WDI is internally connected to a voltage divider between VOUT and GND. If unconnected, WDI is driven to 1.6 V (TYP), disabling the watchdog function.

9/ The chip enable resistance is tested with V_{CC} = +4.75 V. $\overline{CE}$ IN = $\overline{CE}$ OUT = V_{CC}/2.

10/ The chip enable propagation delay is measured from 50% point at $\overline{CE}$ IN to the 50% point at $\overline{CE}$ OUT.

Case X



Dimensions									
Symbol	Inches		Millimeters		Symbol	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	.053	.069	1.35	1.75	e	.050 BSC		1.27 BSC	
A1	.004	.010	0.10	0.25	E	.150	.157	3.80	4.00
b	.014	.019	0.35	0.49	E1	.228	.244	5.80	6.20
c	.007	.010	0.19	0.25	L	.016	.050	0.40	1.27
D	.386	.394	9.80	10.00					

NOTES:
1. D and E do not include mold flash.
2. Mold flash or protrusions not to exceed 0.15 mm (.006”).
3. Leads to be coplanar within 0.10 mm (.004”).
4. Meets JEDEC MS012-AC.
5. Controlling dimensions are millimeters. Inch dimensions are provide for reference only.

FIGURE 1. Case outline.

Case outline X

Terminal number	Terminal symbol	FUNCTION
1	VBATT	Battery-Backup Input. Connect to external battery or capacitor and charging circuit. If backup battery is not used, connect to GND.
2	VOUT	Output Supply Voltage. When VCC is greater than VBATT and above the reset threshold, VOUT connects to V_{CC}. When V_{CC} falls below VBATT and is below the reset threshold, VOUT connects to VBATT. Connect a 0.1µFcapacitor from VOUT to GND. Connect VOUT to V_{CC} if no backup battery is used.
3	VCC	Input Supply Voltage, 5V Input.
4	GND	Ground. 0V reference for all signals.
5	BATT ON	Battery-On Output. When VOUT switches to VBATT, BATT ON goes high. When VOUT switches to VCC, BATT ON goes low. Connect the base of a PNP through a current-limiting resistor to BATT ON for VOUT current requirements greater than 250mA.
6	$\overline{\text{LOWLINE}}$	$\overline{\text{LOWLINE}}$ output goes low when VCC falls below the reset threshold. It returns high as soon as VCC rises above the reset threshold.
7	OSC IN	External Oscillator Input. When OSC SEL is unconnected or driven high, a 10µA pull-up connects from VOUT to OSC IN, the internal oscillator sets the reset and watchdog timeout periods, and OSC IN selects between fast and slow watchdog timeout periods. When OSC SEL is driven low, the reset and watchdog timeout periods may be set either by a capacitor from OSC IN to ground or by an external clock at OSC IN.
8	OSC SEL	Oscillator Select. When OSC SEL is unconnected or driven high, the internal oscillator sets the reset delay and watchdog timeout period. When OSC SEL is low, the external oscillator input (OSC IN) is enabled. OSC SEL has a 10µA internal pull-up.
9	PFI	Power-Fail Input. This is the noninverting input to the power-fail comparator. When PFI is less than 1.25V, $\overline{\text{PFO}}$ goes low. When PFI is not used, connect PFI to GND or VOUT.
10	$\overline{\text{PFO}}$	Power-Fail Output. This is the output of the power-fail comparator. $\overline{\text{PFO}}$ goes low when PFI is less than 1.25V. This is an uncommitted comparator, and has no effect on any other internal circuitry.
11	WDI	Watchdog Input. WDI is a three-level input. If WDI remains either high or low for longer than the watchdog timeout period. $\overline{\text{WDO}}$ goes low and reset is asserted for the reset timeout period. $\overline{\text{WDO}}$ remains low until the next transition at WDI. Leaving WDI unconnected disables the watchdog function. WDI connects to an internal voltage divider between VOUT and GND, which sets it to mid-supply when left unconnected.
12	$\overline{\text{CE}}$ OUT	Chip-Enable Output. $\overline{\text{CE}}$ OUT goes low only when $\overline{\text{CE}}$ IN is low and VCC is above the reset threshold. If $\overline{\text{CE}}$ IN is low when reset is asserted, $\overline{\text{CE}}$ OUT will stay low for 15 µs or until $\overline{\text{CE}}$ IN goes high, whichever occurs first.
13	$\overline{\text{CE}}$ IN	Chip-Enable Input. The input to chip-enable gating circuit. If $\overline{\text{CE}}$ IN is not used, connect $\overline{\text{CE}}$ IN to GND or VOUT.
14	$\overline{\text{WDO}}$	Watchdog Output. If WDI remains high or low longer than the watchdog timeout period, $\overline{\text{WDO}}$ goes low and reset is asserted for the reset timeout period. $\overline{\text{WDO}}$ returns high on the next transition at WDI. $\overline{\text{WDO}}$ remains high if WDI is unconnected.
15	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ Output goes low whenever VCC falls below the reset threshold. $\overline{\text{RESET}}$ will remain low typically for 200ms after VCC crosses the reset threshold on power-up.
16	RESET	RESET is an active-high output. It is open drain, and the inverse of $\overline{\text{RESET}}$.

FIGURE 2. Terminal connections.

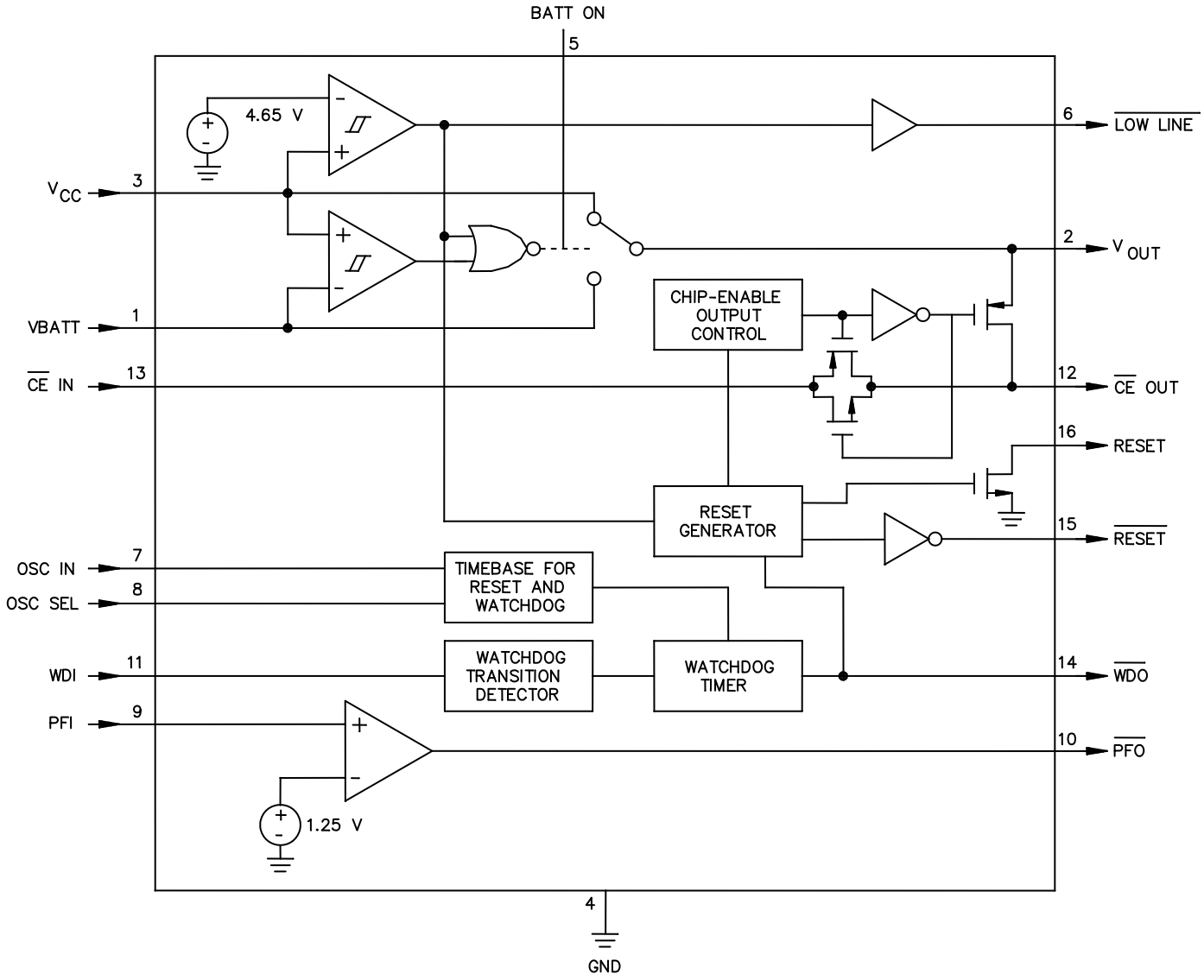


FIGURE 3. Block diagram.

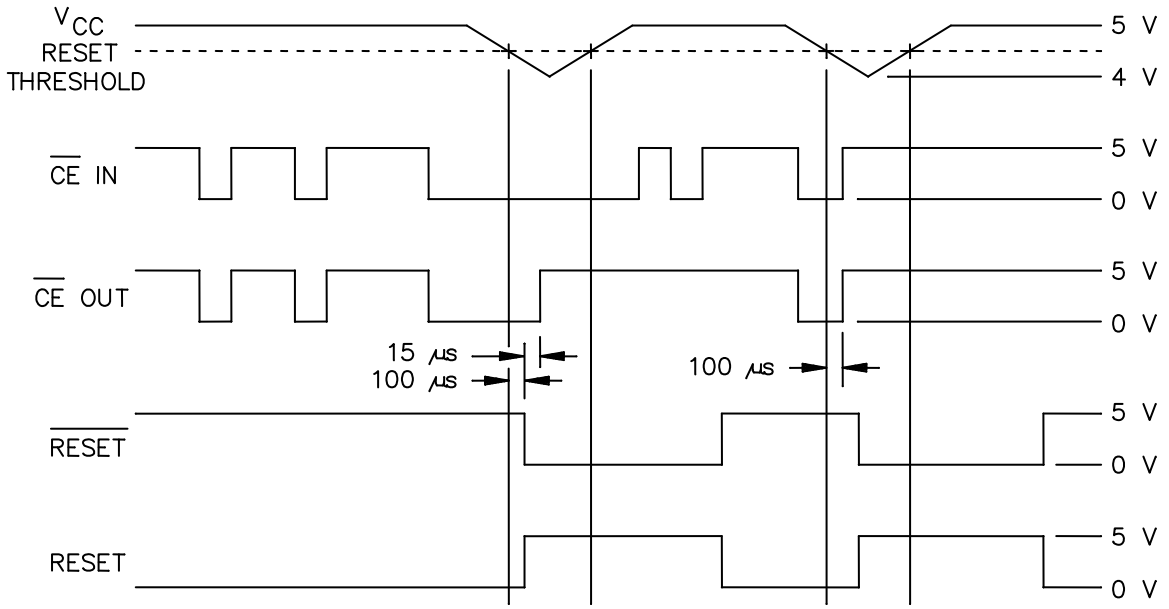


FIGURE 4. Reset and chip enable timing.

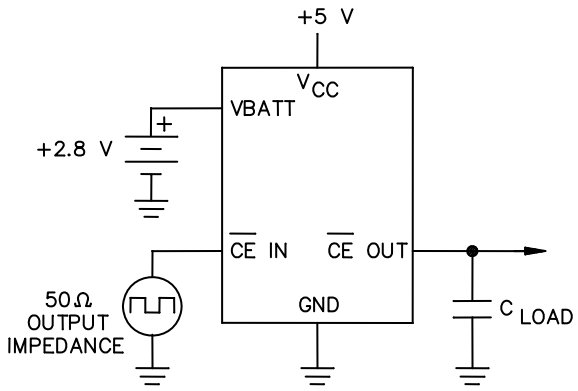


FIGURE 5. $\overline{\text{CE}}$ propagation delay test circuit.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/09632-01XB	1ES66	MAX691AMSE/PR 2/

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ For tape and reel add –T suffix to the part number.

CAGE code	Source of supply
1ES66	Maxim Integrated Products 120 San Gabriel Dr Sunnyvale, CA 94086-5125