REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV																						
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PMIC N/A	PREPARED BY Phu H. Nguyen	DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218-3990 http://www.dscc.dla.mil
Original date of drawing YY MM DD 10-02-10	CHECKED BY Phu H. Nguyen APPROVED BY Thomas M. Hess	TITLE MICROCIRCUIT, DIGITAL, FIXED POINT DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON
	SIZE: A CODE IDENT. NO.: 16236	DWG NO. V62/09629
	REV	PAGE 1 OF 48

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance Fixed-Point Digital Signal Processor microcircuit, with an operating temperature range of -40°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/09629	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s). 1/

Device type	Generic	Clock Rate	Circuit function
01	SM320C6424-EP	400 MHz	Fixed point digital signal Processor
02	SM320C6424-EP	500 MHz	Fixed point digital signal Processor
03	SM320C6424-EP	600 MHz	Fixed point digital signal Processor
04	SM320C6424-EP	700 MHz	Fixed point digital signal Processor

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	Package style
X	376	Plastic ball grid array

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1/ Users are cautioned to review the manufacturers data manual for additional user information relating to this device.

1.3 Absolute maximum ratings. 2/

Supply voltage ranges:
- Core, (CV_{DD}) ..... -0.5 V to +1.5 V 3/
- I/O, 3.3 V (DV_{DD33}) ..... -0.5 V to +4.2 V 3/
- I/O, 1.8 V (DV_{DDR2}, DDR_VDDDLL, PLL_{PWR18}, MXV_{DD}) ..... -0.5 V to +2.5 V 3/

Input voltage ranges: (V_I):
- V_I, I/O, 3.3 V pins (except PCI capable pins) ..... -0.5 V to 4.2 V
- V_I, I/O, 3.3 V pins PCI capable pins ..... -0.5 V to DV_{DD33} + 0.5 V
- V_I, I/O, 1.8 V ..... -0.5 V to +2.5 V

Output voltage ranges:
- V_O, I/O, 3.3 V pins (except PCI capable pins) ..... -0.5 V to 4.2 V
- V_O, I/O, 3.3 V pins PCI capable pins ..... -0.5 V to DV_{DD33} + 0.5 V
- V_O, I/O, 1.8 V ..... -0.5 V to +2.5 V

Operating junction temperature ranges, (T_J):
- Device type: 03 ..... -40°C to +125°C

Storage temperature range, (T_{STG}) ..... -65°C to +150°C

1.4 Recommended operating conditions. 4/ 5/

Supply voltage, core (CV_{DD}):
- device type 03 ..... 1.14 V to 1.26 V 6/)

Supply voltage, (DV_{DD}):
- I/O, 3.3 V (D_{VDD33}) ..... 2.97 V to 3.63 V
- I/O, 1.8 V (DV_{DDR2}, DDR_VDDDLL, PLL_{PWR18}, MXV_{DD} 7/) ..... 1.71 V to 1.89 V

Supply ground (V_{SS}, DDR_VSSDLL, MXV_{SS} 8/) ..... 0 V

DDR2 reference voltage, (DDR_VREF) 9/ ..... $0.49DV_{DDR2}$ V to $0.51DV_{DDR2}$ V

DDR2 impedance control, connected via 200 Ω resistor to V_{SS}, (DDR_ZP) ..... V_{SS} TYP

DDR2 impedance control, connected via 200 Ω resistor to DV_{DDR2}, (DDR_ZN) ..... DV_{DDR2} V TYP

High level input voltage, (V_{IH}):
- 3.3 V (except PCI capable and I2C pins) ..... 2 V minimum
- MXI/ CLKIN ..... $0.65MXV_{DD}$ V minimum
- PCI ..... $0.5DV_{DD33}$ to DV_{DD33} + 0.5 V
- I2C ..... $0.7DV_{DD33}$ V minimum

Low level input voltage, (V_{IL}):
- 3.3 V (except PCI capable and I2C pins) ..... 0.8 V maximum
- MXI/ CLKIN ..... $0.35MXV_{DD}$ V maximum
- PCI ..... -0.5 V to $0.3DV_{DD33}$ V
- I2C ..... 0.V to $0.3DV_{DD33}$ V maximum

2/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3/ All voltage values are with respect to V_{SS}.

4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

5/ The actual voltage must be determined at device power-up, and not be changed dynamically during run-time.

6/ Applies to “tape and reel” part number counterparts as well. For more information, see manufacturer data.

7/ Oscillator 1.8 V power supply (MXV_{DD}) can be connected to the same 1.8 V power supply as DV_{DDR2}.

8/ Oscillator ground (MXV_{SS}) must be kept separate from other grounds and connected directly to the crystal load capacitor ground.

9/ DDR_VREF is expected to equal $0.5V_{DDR2}$ of the transmitting device and to track variations in the V_{DDR2}.

1.4 Recommended operating conditions - Continued.

Operating junction temperature, (T_J) 10/ 11/:
Device type 03 ..... -40°C to +125°C
Operating ambient temperature (T_A): 11/
Device type 03 ..... -40°C to +85°C
DSP Operating frequency ($F_{SYSCLK1}$) 6/
CV_{DD} = 1.2 V: Device type 03 ..... 600 MHz
CV_{DD} = 1.05 V: Device type 03 ..... 450 MHz
Thermal data for case outline X:

No		°C/W 12/	Air Flow (m/s) 13/
1	Junction to case, $R_{\theta JC}$	7.7	N/A
2	Junction to board, $R_{\theta JB}$	10.5	N/A
3	Junction to free air, $R_{\theta JA}$	19.7	0.00
4		15.5	1.0
5		14.3	2.00
7	Junction to package top, Psi_{JT}	4.9	0.00
8		5.1	1.0
9		5.2	2.00
11	Junction to board, Psi_{JB}	10.4	0.00
12		9.8	1.0
13		9.6	2.00

10/ In the absence of a heat sink or direct thermal attachment on the top of device, use the following formula to determine the device junction temperature: $T_J = T_C + (\text{Power} \times Psi_{JT})$. Power and T_C can be measured by the user. Thermal data for GDU provide the junction to package top (Psi_{JT}) value based on airflow in the system. In the present of a heat sink or direct thermal attachment on the top of device, additional calculations and considerations must be taken into account. For more detail see manufacturer data.

11/ Applications must meet both the operating junction temperature and operating ambient temperature requirements. For more detailed information on thermal considerations, measurements, and calculations, see manufacturer data.

12/ The junction to case measurement was conducted in a JEDEC defined 1SOP system. Other measurements were conducted in a JEDEC defined 1S2P system and will change based on environment as well as application. For more information, see three EIA/JEDEC standards: JEDEC 51-2, JEDEC 51-3, JEDEC 51-7.

13/ m/s = meters per second

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2. APPLICABLE DOCUMENTS

JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JEDEC STD 51-2	–	Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
JEDEC STD 51-3	–	Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.
JEDEC STD 51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as specified in figure 3.

3.5.4 Test load circuit for AC timing measurement. The test load circuit for AC timing measurements shall be as specified in figure 4.

3.5.5 Timing waveforms. The timing waveforms shall be as shown in figures 5-57.

TABLE I. Electrical performance characteristics. 1/

Test		Symbol	Test condition 2/ Device type: All	Limits Min	Limits Max	Unit
High level output voltage	3.3 V I/O except PCI capable and I2C pins	V_{OH}	DV_{DD33} = MIN, I_{OH} = MAX	2.4		V
	3.3 V I/O PCI capable pins 3/		I_{OH} = -0.5 mA, DV_{DD33} = 3.3 V	$0.9DV_{DD33}$		
Low level output voltage	3.3 V I/O except PCI capable and I2C pins	V_{OL}	DV_{DD33} = MIN, I_{OL} = MAX		0.4	V
	3.3 V I/O PCI capable pins 3/		I_{OH} = 1.5 mA, DV_{DD33} = 3.3 V		$0.22DV_{DD33}$	
	3.3 V I/O I2C pins		I_O = 3 mA	0	0.4	
Input current [DC]	3.3 V pins (except PCI capable and I2C pins)	I_I 4/	$V_I = V_{SS}$ to DV_{DD33}, pins with internal pullup resistor 5/	50	250	µA
			$V_I = V_{SS}$ to DV_{DD33}, pins with internal pulldown resistor	-250	-50	
	I2C pins		$V_I = V_{SS}$ to DV_{DD33}		±10	
	PCI capable pins 6/		$0 < V_I < DV_{DD33}$ = 3.3 V without internal resistance		±50	
			$0 < V_I < DV_{DD33}$ = 3.3 V without internal pull up resistance 5/	50	250	
			$0 < V_I < DV_{DD33}$ = 3.3 V without internal pull down resistance 5/	-250	-50	
High level output current [DC]		I_{OH}	CLK_OUT0/PWM2/GPIO[84] and VLYNQ_CLOCK/PCICLK/GP[57]		-8	mA
			DDR2		-13.4	
			PCI capable pins		-0.5 3/	
			All other peripherals		-4	
Low level output current [DC]		I_{OL}	CLK_OUT0/PWM2/GPIO[84] and VLYNQ_CLOCK/PCICLK/GP[57]		8	
			DDR2		13.4	
			PCI capable pins		1.5 3/	
			All other peripherals		4	
I/O Off state output current		I_{OZ} 7/	$V_O = DV_{DD33}$ or VSS, internal pull disabled		±50	µA
			$V_O = DV_{DD33}$ or VSS, internal pull enabled	± 100 TYP		µA
Core (CV_{DD}) supply current 8/		I_{CDD}	CV_{DD} = 1.2 V, DSP clock = 700 MHz	597 TYP		mA
			CV_{DD} = 1.2 V, DSP clock = 600 MHz	524 TYP		
			CV_{DD} = 1.2 V, DSP clock = 500 MHz	460 TYP		
			CV_{DD} = 1.2 V, DSP clock = 400 MHz	392 TYP		
			CV_{DD} = 1.2 V, DSP clock = 560 MHz	442 TYP		
			CV_{DD} = 1.2 V, DSP clock = 450 MHz	372 TYP		
			CV_{DD} = 1.2 V, DSP clock = 400 MHz	341 TYP		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test condition 2/ Device type: All	Limits		Unit
			Min	Max	
3.3 V I/O (DV_{DD33}) supply current	I_{DDD}	DV_{DD} = 3.3 V, CV_{DD} = 1.2 V, DSP clock = 700 MHz	13 TYP		mA
		DV_{DD} = 3.3 V, CV_{DD} = 1.2 V, DSP clock = 600 MHz	13 TYP		
		DV_{DD} = 3.3 V, CV_{DD} = 1.2 V, DSP clock = 500 MHz	13 TYP		
		DV_{DD} = 3.3 V, CV_{DD} = 1.2 V, DSP clock = 400 MHz	13 TYP		
		DV_{DD} = 3.3 V, CV_{DD} = 1.05 V, DSP clock = 560 MHz	13 TYP		
		DV_{DD} = 3.3 V, CV_{DD} = 1.05 V, DSP clock = 450 MHz	13 TYP		
		DV_{DD} = 3.3 V, CV_{DD} = 1.05 V, DSP clock = 400 MHz	13 TYP		
1.8 V I/O (DV_{DDR2}, DDR_VDDDLL, $PLLV_{PRW18}$, MXV_{DD}) supply current	I_{DDD}	DV_{DD} = 1.8 V, CV_{DD} = 1.2 V, DSP clock = 700 MHz	94 TYP		
		DV_{DD} = 1.8 V, CV_{DD} = 1.2 V, DSP clock = 600 MHz	93 TYP		
		DV_{DD} = 1.8 V, CV_{DD} = 1.2 V, DSP clock = 500 MHz	92 TYP		
		DV_{DD} = 1.8 V, CV_{DD} = 1.2 V, DSP clock = 400 MHz	91 TYP		
		DV_{DD} = 1.8 V, CV_{DD} = 1.05 V, DSP clock = 560 MHz	74 TYP		
		DV_{DD} = 1.8 V, CV_{DD} = 1.05 V, DSP clock = 450 MHz	73 TYP		
		DV_{DD} = 1.8 V, CV_{DD} = 1.05 V, DSP clock = 400 MHz	72 TYP		
Input capacitance	C_i			5	pF
Output capacitance	C_o			5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No.	Test		Symbol	Test condition 2/ Device type: All	Limits Min	Limits Max	Unit
	RESET ELECTRICAL DATA/TIMING						
Timing requirements for Reset (See figure 5 and 6)							
1	Pulse duration, $\overline{\text{POR}}$ low or $\overline{\text{RESET}}$ low		$t_{w(RESET)}$		12C 9/		ns
4	Setup time, boot and configuration pins valid before $\overline{\text{POR}}$ high or $\overline{\text{RESET}}$ high		$t_{su(CONFIG)}$		12C 9/		
5	Hold time, boot and configuration pins valid after $\overline{\text{POR}}$ high or $\overline{\text{RESET}}$ high		$t_{h(CONFIG)}$		0		
Switching characteristics during reset 11/							
2	Delay time, $\overline{\text{POR}}$ high or $\overline{\text{RESET}}$ high to $\overline{\text{RESETOUT}}$ high		$t_{d(RSTH-RSTOUTH)}$			1900C	ns
3	Pulse duration, SYSCLKs paused (low) before $\overline{\text{RESETOUT}}$ high		$t_{w(PAUSE)}$		10C	10C	
6	Delay time, $\overline{\text{POR}}$ low or $\overline{\text{RESET}}$ low to pins invalid		$t_{d(RSTL-IV)}$			20	
7	Delay time, $\overline{\text{POR}}$ high or $\overline{\text{RESET}}$ high to pins valid		$t_{d(RSTH-V)}$			20	
8	Delay time, $\overline{\text{RESET}}$ high to pins valid		$t_{d(RSTOUTH-V)}$			0	
9	Delay time, $\overline{\text{RESET}}$ high to pins invalid		$t_{d(RSTOUTH-IV)}$			12C	
	EXTERNAL CLOCK INPUT FROM MXI/CLKIN PIN						
Input requirement for Crystal 12/ See figure 7							
	Start up time (from power up until oscillating at stable frequency of 30 MHz)					4	ms
	Oscillation frequency				15	30	MHz
	ESR					60	Ω
	CLOCK PLLs						
PLLC1 clock frequency ranges							
	MXI/CLKIN 13/				15	30	MHz
	PLLOUT	Device type 03		CV_{DD} = 1.2 V	300	600	
	PLLOUT	Device type 03		CV_{DD} = 1.05 V	300	520	
	SYSCLK1 14/ (CLKDIV1 domain)	Device type 03		CV_{DD} = 1.2 V		600	
	SYSCLK1 14/ (CLKDIV1 domain)	Device type 03		CV_{DD} = 1.05 V		450	
PLLC2 clock frequency ranges							
	MXI/CLKIN 13/				15	30	MHz
	PLLOUT			At 1.2 V CV_{DD}	300	900	
				At 1.05 V CV_{DD}	300	666	
	PLL2_SYSCLK1 (to DDR2 PHY)					333	
PLL stabilization/Lock/Reset time							
	PLL stabilization time				150		µs
	PLL lock time					2000C 15/	ns
	PLL reset time				128C 15/		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

	Test	Symbol	Test condition 2/ Device type: All	Limits Min	Limits Max	Unit
	CLOCK PLLs - Continued					
	Timing requirements for MXI/CLKIN 15/ 16/ 17/ 18/ (See figure 8)					
1	Cycle time, MXI/CLKIN	$t_{c(MXI)}$		33.3	66.7	ns
2	Pulse duration, MXI/CLKIN high	$t_{w(MXIH)}$		0.45C	0.55C	
3	Pulse duration, MXI/CLKIN low	$t_{w(MXIL)}$		0.45C	0.55C	
4	Transition time, MXI/CLKIN	$t_{t(MXI)}$			0.05C	
5	Period jitter, MXI/CLKIN	$t_{J(MXI)}$			0.02C	
	Switching characteristics for CLKOUTT0 19/ 20/ (See figure 9)					
1	Cycle time, CLKOUT0	t_C		33.3	66.7	ns
2	Pulse duration, CLKOUT0 high	$t_{w(CLKOUT0H)}$		0.45P	0.55P	
3	Pulse duration, CLKOUT0 low	$t_{w(CLKOUT0L)}$		0.45P	0.55P	
4	Period jitter, CLKOUT0	$t_{t(CLKOUT0)}$			0.05P	
	EXTERNAL MEMORY INTERFACE (EMIF)					
	EMIFA Electrical Data/Timing					
	Timing requirements for Asynchronous memory cycles for EMIFA module 21/ (See figure 10 and 11)					
	Reads and Writes					
2	Pulse duration, EM_WAIT assertion and deassertion	$t_{w(EM_WAIT)}$		2E TYP		ns
	Reads					
12	Setup time, EM_D[15:o] valid before $\overline{EM_OE}$ high	$t_{su(EMDV_EMOEH)}$		5		ns
13	Hold time, EM_D[15:o] valid after $\overline{EM_OE}$ high	$t_{h(EMOEH_EMDIV)}$		0		
14	Setup time, EM_WAIT asserted before $\overline{EM_OE}$ high 22/	$t_{su(EMWAIT-EMOEH)}$		4E + 5		
	Writes					
25	Setup time, EM_WAIT asserted before $\overline{EM_WE}$ high 22/			4E + 5		ns
	Switching characteristics for Asynchronous memory cycles for EMIFA module 21/ 23/ (See figure 10 and 11)					
	Reads and Writes					
1	Turn around time	$t_{d(TURNAROUND)}$		(TA + 1)*E TYP		ns
	Reads					
3	EMIF read cycle time	$t_{c(EMRCYCLE)}$		(RS + RST + RH + TA + 4) * E TYP 24/		
4	Output setup time, $\overline{EM_CS[5:2]}$ low to $\overline{EM_OE}$ low (SS = 0)	$t_{su(EMCSL-EMOEL)}$		(RS + 1)*E - 4	(RS + 1)*E + 4	ns
	Output setup time, $\overline{EM_CS[5:2]}$ low to $\overline{EM_OE}$ low (SS = 1)			-4	4	
5	Output hold time, $\overline{EM_OE}$ high to $\overline{EM_CS[5:2]}$ high (SS = 0)	$t_{h(EMOEH-EMCSH)}$		(RH + 1)*E - 4	(RH + 1)*E + 4	
	Output hold time, $\overline{EM_OE}$ high to $\overline{EM_CS[5:2]}$ high (SS = 1)			-4	4	
6	Output setup time, $\overline{EM_BA[1:0]}$ valid to $\overline{EM_OE}$ low	$t_{su(EMBAV-EMOEL)}$		(RS + 1)*E - 4	(RS + 1)*E + 4	
7	Output hold time, $\overline{EM_OE}$ high to $\overline{EM_BA[1:0]}$ invalid	$t_{h(EMOEH-EMBAIV)}$		(RH + 1)*E - 4	(RH + 1)*E + 4	
8	Output setup time, $\overline{EM_A[21:0]}$ valid to $\overline{EM_OE}$ low	$t_{su(EMBAV-EMOEL)}$		(RS + 1)*E - 4	(RS + 1)*E + 4	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No.	Test	Symbol	Test condition 2/ Device type: All	Limits Min	Limits Max	Unit
	EXTERNAL MEMORY INTERFACE (EMIF) - Continued					
	EMIFA Electrical Data/Timing					
	Switching characteristics for Asynchronous memory cycles for EMIFA module 21/ 23/ (See figure 10 and 11) - Continued					
9	Output hold time, $\overline{EM_OE}$ high to $\overline{EM_A[21:0]}$ invalid	$t_{h(EMOEH-EMBAIV)}$			(RH + 1)*E + 4	ns
10	$\overline{EM_OE}$ active low width	$t_{w(EMOEL)}$		(RST + 1)*E TYP 24/		
11	Delay time from EM_WAIT deasserted to $\overline{EM_OE}$ high	$t_{d(EMWAITH-EMOEH)}$			4E + 4	
	Writes					
15	EMIF write cycle time	$t_{c(EMWCYCLE)}$		(WS + WST + WH + TA + 4) * E TYP 24/		ns
16	Output setup time, $\overline{EM_CS[5:2]}$ low to $\overline{EM_WE}$ low (SS = 0)	$t_{su(EMCSL-EMWEL)}$		(WS + 1)*E - 4	(WS + 1)*E + 4	
	Output setup time, $\overline{EM_CS[5:2]}$ low to $\overline{EM_WE}$ low (SS = 1)			-4	4	
17	Output hold time, $\overline{EM_WE}$ high to $\overline{EM_CS[5:2]}$ high (SS = 0)	$t_{h(EMWEH-EMCSH)}$		(WH + 1)*E - 4	(WH + 1)*E + 4	
	Output hold time, $\overline{EM_WE}$ high to $\overline{EM_CS[5:2]}$ high (SS = 1)			-4	4	
18	Output setup time, EM_R/$\overline{W}$ valid to $\overline{EM_WE}$ low	$t_{su(EMBAV-EMWEL)}$		(WS + 1)*E - 4	(WS + 1)*E + 4	
19	Output hold time, $\overline{EM_WE}$ high to EM_R/$\overline{W}$ invalid	$t_{h(EMWEH-EMBAIV)}$		(WH + 1)*E - 4	(WH + 1)*E + 4	
20	Output setup time, $\overline{EM_BA[1:0]}$ valid to $\overline{EM_WE}$ low	$t_{su(EMBAV-EMWEL)}$		(WS + 1)*E - 4	(WS + 1)*E + 4	
21	Output hold time, $\overline{EM_WE}$ high to $\overline{EM_BA[1:0]}$ invalid	$t_{h(EMWEH-EMBAIV)}$		(WH + 1)*E - 4	(WH + 1)*E + 4	
22	Output setup time, $\overline{EM_A[21:0]}$ valid to $\overline{EM_WE}$ low	$t_{su(EMAV-EMWEL)}$		(WS + 1)*E - 4	(WS + 1)*E + 4	
23	Output hold time, $\overline{EM_WE}$ high to $\overline{EM_A[21:0]}$ invalid	$t_{h(EMWEH-EMAIV)}$		(WH + 1)*E - 4	(WH + 1)*E + 4	
24	$\overline{EM_WE}$ active low width	$t_{w(EMWEL)}$		(WST + 1)*E 24/		
25	Delay time from EM_WAIT deasseted to $\overline{EM_WE}$ high	$t_{d(EMWAITH-EMWEH)}$			4E + 4	
26	Output setup time, EM_D[15:0] valid to $\overline{EM_WE}$ low	$t_{su(EMDV-EMWEL)}$			(WS + 1)*E + 4	
27	Output hold time, $\overline{EM_WE}$ high to EM_D[15:0] invalid	$t_{h(EMWEH-EMDIV)}$			(WH + 1)*E + 4	
	Switching characteristics for DDR2 memory 25/ 26/ (See figure 14)					
1	Cycle time, DDR_CLK	$t_{c(DDR_CLK)}$		6	8	ns
	UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART)					
	Timing requirements for UARTx receive 27/ (See figure 15)					
4	Pulse duration, UART receive data bit (URXDx)[15/30/100 pf]	$t_{w(URXDB)}$		0.96U	1.05U	
5	Pulse duration, UART receive start bit [15/30/100 pF]	$t_{w(URXSB)}$		0.96U	1.05U	
	Switching characteristics for UARTx transmit 27/ (See figure 15)					
1	maximum programmable baud rate	$f_{(baud)}$			128	ns
2	Pulse duration, UART transmit data bit (UTXDx)[15/30/100 pF]	$t_{w(UTXDB)}$		U - 2	U + 2	
3	Pulse duration, UART transmit start bit [15/30/100 pF]	$t_{w(UTXSB)}$		U - 2	U + 2	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No.	Test	Symbol	Test condition 2/ Device type: All	Limits				Unit
				Standard mode		Fast mode		
				Min	Max	Min	Max	
	INTER-INTEGRATED CIRCUIT (I2C)							
Timing requirements for I2C timings 28/ (See figure 16)								
1	Cycle time, SCL	$t_{c(SCL)}$		10		2.5		µs
2	Setup time, SCL high before SDA low (for a repeated START condition)	$t_{su(SCLH-SDAL)}$		4.7		0.6		
3	Hold time, SCL low after SDA low (for a START and a repeated START condition)	$t_{h(SCLL-SDAL)}$		4		0.6		
4	Pulse duration, SCL low	$t_{w(SCLL)}$		4.7		1.3		
5	Pulse duration, SCL high	$t_{w(SCLH)}$		4		0.6		
6	Setup time, SDA valid before SCL high	$t_{su(SDAV-SCLH)}$		250		100 29/		ns
7	Hold time, SDA valid after SCL low	$t_{h(SDA-SCLL)}$		0 30/		0 30/	0.9 31/	µs
8	Pulse duration, SDA high between STOP and START conditions	$t_{w(SDAH)}$		4.7		1.3		
9	Rise time, SDA	$t_{r(SDA)}$			1000	20 + 0.1C_b 32/	300	ns
10	Rise time, SCL	$t_{r(SCL)}$			1000	20 + 0.1C_b 32/	300	
11	Fall time, SDA	$t_{f(SDA)}$			300	20 + 0.1C_b 32/	300	
12	Fall time, SCL	$t_{f(SCL)}$			300	20 + 0.1C_b 32/	300	
13	Setup time, SCL high before SDA high (for STOP condition)	$t_{su(SCLH-SDAH)}$		4		0.6		µs
14	Pulse duration, spike (must be suppressed)	$t_{w(SP)}$				0	50	ns
15	Capacitive load for each bus line	C_b 32/			400		400	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No.	Test	Symbol	Test condition 2/ Device type: All	Limits				Unit
				Standard mode		Fast mode		
				Min	Max	Min	Max	
	INTER-INTEGRATED CIRCUIT (I2C) - Continued							
Switching characteristics for I2C timings 28/ (See figure 17)								
16	Cycle time, SCL	$t_{c(SCL)}$		10		2.5		µs
17	Setup time, SCL high before SDA low (for a repeated START condition)	$t_{su(SCLH-SDAL)}$		4.7		0.6		
18	Delay time, SDA low to SCL low (for a START and a repeated START condition)	$t_{h(SCLL-SDAL)}$		4		0.6		
19	Pulse duration, SCL low	$t_{w(SCLL)}$		4.7		1.3		
20	Pulse duration, SCL high	$t_{w(SCLH)}$		4		0.6		
21	Delay time, SDA valid to SCL high	$t_{su(SDAV-SCLH)}$		250		100		ns
22	Valid time, SDA valid after SCL low	$t_{h(SDA-SCLL)}$		0		0	0.9	µs
23	Pulse duration, SDA high between STOP and START conditions	$t_{w(SDAH)}$		4.7		1.3		
24	Rise time, SDA	$t_{r(SDA)}$			1000	$20 + 0.1C_b$ 32/	300	ns
25	Rise time, SCL	$t_{r(SCL)}$			1000	$20 + 0.1C_b$ 32/	300	
26	Fall time, SDA	$t_{f(SDA)}$			300	$20 + 0.1C_b$ 32/	300	
27	Fall time, SCL	$t_{f(SCL)}$			300	$20 + 0.1C_b$ 32/	300	
28	Delay time, SCL high to SDA high (for STOP condition)	$t_{su(SCLH-SDAH)}$		4		0.6		µs
29	Capacitive load for each I2C pin	C_b 32/			10		10	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

No.	Test		Symbol	Test condition 2/ Device type: All	Limits		Unit
					Min	Max	
	HOST PORT INTERFACE (HPI) PERIPHERAL						
Timing requirements for HPI interface cycles 33/ 34/ (See figure 18 and 19)							
1	Setup time, select signals 35/ valid before $\overline{\text{HSTROBE}}$ low		$t_{su(SELV-HSTBL)}$		5		ns
2	Hold time, select signals 35/ valid after $\overline{\text{HSTROBE}}$ low		$t_{h(HSTBL-SELV)}$		2		
3	Pulse duration, $\overline{\text{HSTROBE}}$ active low		$t_{w(HSTBL)}$		15		
4	Pulse duration, $\overline{\text{HSTROBE}}$ inactive high between consecutive accesses		$t_{w(HSTBH)}$		2M		
11	Setup time, host data valid before $\overline{\text{HSTROBE}}$ high		$t_{su(HDV-HSTBH)}$		5		
12	Hold time, host data valid after $\overline{\text{HSTROBE}}$ high		$t_{h(HSTBH-HDV)}$		0		
13	Hold time, $\overline{\text{HSTROBE}}$ high after $\overline{\text{HRDY}}$ low. $\overline{\text{HSTROBE}}$ should not be inactivated until $\overline{\text{HRDY}}$ is active (low); otherwise, HPI writes will not complete properly.		$t_{h(HRDYL-HSTBL)}$		0		
Switching characteristics for HPI cycles 33/ 34/ 36/ (See figure 17 and 18)							
	Delay time, $\overline{\text{HSTROBE}}$ low to $\overline{\text{HRDY}}$ valid	For HPI Write, $\overline{\text{HRDY}}$ can go high (not ready) for these HPI Write conditions; otherwise, $\overline{\text{HRDY}}$ stay low (ready): *Case 1*: Back to back HPIA writes (can be either first or half word) *Case 2*: HPIA write following a PREFETCH command (can be either first or second half-word) *Case 3*: HPID write when FIFO is full or flushing (can be either first or half word) *Case 4*: HPIA write and Write FIFO not empty. For HPI Read, $\overline{\text{HRDY}}$ can go high (not ready) for these HPI Read conditions: *Case 1*: HPID read (with auto-increment) and data not in read FIFO (can only happen to first half word of HPID access) *Case 2*: First half word access of HPID Read without auto-increment and dat is already in Read FIFO (applies to either half-word of HPID access) *Case 3*: HPIC or HPIA read (applies to either half word access)					
	Enable time, HD driven from $\overline{\text{HSTROBE}}$ low						
	Delay time, $\overline{\text{HRDY}}$ low to HD valid						
	Output hold time, HD valid after $\overline{\text{HSTROBE}}$ high						
	Disable time, HD high impedance from $\overline{\text{HSTROBE}}$ high						
	Delay time, $\overline{\text{HSTROBE}}$ low to HD valid	37/					
	Delay time, $\overline{\text{HSTROBE}}$ low to $\overline{\text{HRDY}}$ valid	38/					

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test condition 2/ Device types: All		Limits Min	Limits Max	Unit
	MULTICHANNEL BUFFERED SERIAL PORT (McBSP) TIMING						
Timing requirements for McBSP 39/							
2	Cycle time, CLKR/X	$t_{c(CKRX)}$	See figure 20	CLKR/X ext	2P 40/ 41/		ns
3	Pulse duration, CLKR/X high or CLKR/X low	$t_{w(CKRX)}$		CLKR/X ext	P – 1 42/		
5	Setup time, external FSR high before CLKR low	$t_{su(FRH-CKRL)}$		CLKR int	14		
				CLKR ext	4		
6	Hold time, external FSR high after CLKR low	$t_{h(CKRL-FRH)}$		CLKR int	6		
				CLKR ext	4		
7	Setup time, DR valid before CLKR low	$t_{su(DRV-CKRL)}$		CLKR int	14		
				CLKR ext	4		
8	Hold time, DR valid after CLKR low	$t_{h(CKRL-DRV)}$		CLKR int	3.5		
				CLKR ext	3		
10	Setup time, external FSX high before CLKX low	$t_{su(FXH-CKXL)}$		CLKR int	14		
				CLKR ext	4		
11	Hold time, external FSX high after CLKX low	$t_{h(CKXL-FXH)}$		CLKR int	6		
				CLKR ext	3		
Switching characteristics for McBSP 44/ 47/							
1	Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input 48/	$t_{d(CKSH-CKRXH)}$	See figure 20		3	10	ns
2	Cycle time, CLKR/X	$t_{c(CKRX)}$		CLKR/X int	2P 40/ 44/ 45/		
3	Pulse duration, CLKR/X high or CLKR/X low	$t_{w(CKRX)}$		CLKR/X int	C-2 46/	C+2 46/	
4	Delay time, CLKR high to internal FSR valid	$t_{d(CKRH-FRV)}$		CLKR int	-4	5.5	
9	Delay tine, CLKR high to internal FSX valid	$t_{d(CKXH-FXV)}$		CLKX int	-4	5.5	
				CLKX ext	2.5	14.5	
12	Disable time, DX high impedance following last data bit from CLKX high	$t_{d(CKXH-DXHZ)}$		CLKX int	55.5	7.5	
				CLKX ext	-2.1	16	
13	Delay time, CLKX high to DX valid	$t_{d(CKXH-DXV)}$		CLKX int	-4+D1 47/	5.5+D2 47/	
				CLKX ext	2.5+D1 47/	14.5+D2 47/	
14	Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode	$t_{d(FXH-DXV)}$		FSX int	-4 48/	5 48/	
				FSX ext	1 48/	14.5 53/	
Timing requirements for FSR when GSYNC = 1							
1	Setup time, FSR high before CLKS high	$t_{su(FRH-CKSH)}$	See figure 21		4		ns
2	Hold time, FSR high after CLKS high	$t_{h(CKSH-FRH)}$			4		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test condition 2/ Device types: All	Limits				Unit
				Master		Slave		
				Min	Max	Min	Max	
MULTICHANNEL BUFFERED SERIAL PORT (McBSP) TIMING - CONTINUED								
Timing requirements for McBSP as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0 40/ 49/								
4	Setup time, DR valid before CLKX low	$t_{su(DRV-CKXL)}$	See figure 22	14		2-3P		ns
5	Hold time, DR valid after CLKX low	$t_{h(CKXL-DRV)}$		4		5+6P		
Switching characteristics for McBSP as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0 40/ 49/ 50/								
1	Hold time, FSX low after CLKX low 51/	$t_{h(CKXL-FXL)}$	See figure 22	T-4	T+5.5			ns
2	Delay time, FSX low to CLKX high 52/	$t_{d(FXL-CKXH)}$		L-4	L+4			
3	Delay time, CLKX high to DX valid	$t_{d(CKXH-DXV)}$		-4	5.5	3P+2.8	5P+17	
6	Disable time, DX high impedance following last data bit for CLKX low	$t_{dis(CKXL-DXHZ)}$		L-6	L+7.5			
7	Disable time, DX high impedance following last data bit from FSX high	$t_{dis(FXH-DXHZ)}$				P+3	3P+17	
8	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$				2P+1.8	4P+17	
Timing requirements for McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0 40/ 49/								
4	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	See figure 23	14		2-3P		ns
5	Hold time, DR valid after CLKX high	$t_{h(CKXH-DRV)}$		4		5+6P		
Switching characteristics for McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0 40/ 49/								
1	Hold time, FSX low after CLKX low 51/	$t_{h(CKXL-FXL)}$	See figure 23	L-4	L+5.5			ns
2	Delay time, FSX low to CLKX high 52/	$t_{d(FXL-CKXH)}$		T-4	T+4			
3	Delay time, CLKX low to DX valid	$t_{d(CKXL-DXV)}$		-4	5.5	3P+2.8	5P+17	
6	Disable time, DX high impedance following last data bit for CLKX low	$t_{dis(CKXL-DXHZ)}$		-6	7.5	3P+2	5P+17	
7	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$		H-4	H+5.5	2P+2	4P+17	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test condition 2/ Device types: All	Limits				Unit
				Master		Slave		
				Min	Max	Min	Max	
MULTICHANNEL BUFFERED SERIAL PORT (McBSP) TIMING - CONTINUED								
Timing requirements for McBSP as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1 40/ 49/								
4	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	See figure 24	14		2-3P		ns
5	Hold time, DR valid after CLKX high	$t_{h(CKXH-DRV)}$		4		5+6P		
Switching characteristics for McBSP as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1 40/ 49/								
1	Hold time, FSX low after CLKX high 51/	$t_{h(CKXH-FXL)}$	See figure 24	T-4	T+5.5			ns
2	Delay time, FSX low to CLKX low 52/	$t_{d(FXL-CKXL)}$		H-4	H+4			
3	Delay time, CLKX low to DX valid	$t_{d(CKXL-DXV)}$		-4	5.5	3P+2.8	5P+17	
6	Disable time, DX high impedance following last data bit for CLKX high	$t_{dis(CKXH-DXHZ)}$		H-6	H+7.5			
7	Disable time, DX high impedance following last data bit from FSX high	$t_{dis(FXH-DXHZ)}$				P+3	3P+17	
8	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$				2P+2	4P+17	
Timing requirements for McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1 40/ 49/								
4	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	See figure 25	14		2-3P		ns
5	Hold time, DR valid after CLKX high	$t_{h(CKXH-DRV)}$		4		5+6P		
Switching characteristics for McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1 8/ 54/								
1	Hold time, FSX low after CLKX high 51/	$t_{h(CKXH-FXL)}$	See figure 25	H-4	H+5.5			ns
2	Delay time, FSX low to CLKX low 52/	$t_{d(FXL-CKXL)}$		T-4	T+4			
3	Delay time, CLKX high to DX valid	$t_{d(CKXH-DXV)}$		-4	5.5	3P+2.8	30P+17	
6	Disable time, DX high impedance following last data bit for CLKX high	$t_{dis(CKXH-DXHZ)}$		-6	7.5	3P+2	30P+17	
7	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$		L-4	L+5.5	2P+2	4P+17	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test condition 2/ Device types: All		Limits Min	Limits Max	Unit
	MULTICHANNEL BUFFERED SERIAL PORT (McBSP) TIMING						
Multichannel Audio Serial Port (McASP) Timing							
Timing requirements for McASP 53/ (See figure 26 and 27)							
1	Cycle time, AHCLKR/X	$t_{c(AHCKRX)}$			25		ns
2	Pulse duration, AHCLKR/X high or low	$t_{w(AHCKRX)}$			10		
3	Cycle time, ACLKR/X 54/	$t_{c(CKRX)}$		ACLKR/X ext	25		
4	Pulse duration, ACLKR/X high or low	$t_{w(CKRX)}$		ACLKR/X ext	10		
5	Setup time, external AFSR/X input valid before ACLKR/X latches data	$t_{su(FRX-CKRX)}$		ACLKR/X int	11		
				ACLKR/X ext	3		
6	Hold time, AFSR/X input valid after ACLKR/X latches data	$t_{h(CKRX-FRX)}$		ACLKR/X int	0		
				ACLKR/X ext input	4		
				ACLKR/X ext output	6		
7	Setup time, AXR input valid before ACLKR/X latches data	$t_{su(AXR-CKRX-CKRL)}$		ACLKR/X int	11		
				ACLKR/X ext	3		
8	Hold time, AXR input valid after ACLKR/X latches data	$t_{h(CKRX-AXR)}$		ACLKR/X int	3		
				ACLKR/X ext input	4		
				ACLKR/X ext output	6		
Switching characteristics for McaSP 53/ 55/ 56/ (See figure 26 and 27)							
9	Cycle time, AHCLKR/X	$t_{c(AHCKRX)}$			25		ns
10	Pulse duration, AHCLKR/X high or low	$t_{w(AHCKRX)}$			AH-2.5		
11	Cycle time, ACLKR/X 54/	$t_{c(CKRX)}$		ACLKR/X int	25		
12	Pulse duration, ACLKR/X high or low	$t_{w(CKRX)}$		ACLKR/X int	A-2.5		
13	Delay time, ACLKR/X transmit edge to AFSX/R output valid	$t_{d(CKRX-FRX)}$		ACLKR/X int	-2.25	5.5	
				ACLKR/X ext input	0	12.5	
				ACLKR/X ext output	0	14	
14	Delay time, ACLKX transmit edge to AXR output valid	$t_{d(CKX-AXRV)}$		ACLKR/X int	-2.25	5.5	
				ACLKR/X ext input	0	12.5	
				ACLKR/X ext output	0	14	
15	Disable time, AXR high impedance following last data bit from ACLKR/X transmit edge	$t_{dis(CKRX-AXRHZ)}$		ACLKR/X int	-4.5	8	
				ACLKR/X ext	-4.5	12.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No.	Test	Symbol	Test condition 2/ Device types: All	Limits				Unit
				Min	Max	Min	Max	
EMAC MII ELECTRICAL DATA/TIMING								
Timing requirements for MRCLK – MII operation				10 Mbps		100 Mbps		
1	Cycle time, MRCLK 57/	$t_{c(MRCLK)}$	See figure 28	400		40		ns
2	Pulse duration, MRCLK high	$t_{w(MRCLKH)}$		140		14		
3	Pulse duration, MRCLK low	$t_{w(MRCLKL)}$		140		14		
Timing requirements for MTCLK-MII operation				10 Mbps		100 Mbps		
1	Cycle time, MTCLK	$t_{c(MTCLK)}$	See figure 29	400		40		ns
2	Pulse duration, MTCLK high	$t_{w(MTCLKH)}$		140		14		
3	Pulse duration, MTCLK low	$t_{w(MTCLKL)}$		140		14		
Timing requirements for EMAC MII receive 10/100 Mbits 58/								
1	Setup time, receive selected signals valid before MRCLK high	$t_{su(MRXD-MRCLKH)}$	See figure 30			8		ns
2	Hold time, receive selected signals valid after MRCLK high	$t_{h(MRCLKH-MRXD)}$				8		
Switching characteristics for EMAC MII and GMII transmit 10/100 Mbit/s 58/								
1	Delay time, MTCLK high to transmit selected signals valid	$t_{d(MTCLKH-MTXD)}$	See figure 31			5	25	ns
Timing requirements for RMREFCLK – RMII operation								
1	Cycle time, RMREFCLK 57/	$t_{c(RMREFCLK)}$	See figure 32			20		ns
2	Pulse duration, RMREFCLK high	$t_{w(RMREFCLKH)}$				7	13	
3	Pulse duration, RMREFCLK low	$t_{w(RMREFCLKL)}$				7	13	
4	Transition time, RMREFCLK	$t_{t(RMREFCLK)}$					2	
Timing requirements for EMAC RMII input receive for 10/100 Mbps 60/								
1	Setup time, receive selected signals valid before MREFCLK high	$t_{su(RMRXD-REFCLKH)}$	Sii figure 33			4		ns
2	Hold time, receive selected signals valid after MREFCLK high	$t_{h(REFCLKH-RMRXD)}$				2		
Switching characteristics for EMAC RMII transmit 10/100 Mbit/s 61/								
1	Delay time, RMREFCLK high to transmit selected signals valid	$t_{d(REFCLKH-MTXD)}$	See figure 34			2.2	15.5	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No.	Test	Symbol	Test condition 2/ Device types: All	Limits Min	Limits Max	Unit
	MANAGEMENT DATA INPUT/OUTPUT (MDIO) ELECTRICAL DATA/TIMING					
Timing requirements for MDIO input (R)(G)MII						
1	Cycle time, MDCLK	$t_{c(MDCLK)}$	See figure 35 and 36	400		ns
2	Pulse duration, MDCLK high/low	$t_{w(MDCLK)}$		180		
3	Transition time, MDCLK	$t_{t(MDCLK)}$			5	
4	Setup time, MDIO data input valid before MDCLK high	$t_{su(MDIO-MDCLKH)}$		10		
5	Hold time, MDIO data input valid afterMDCLK high	$t_{h(MDCLKH-MDIO)}$		10		
Switching characteristics for MDIO output						
7	Delay time, MDCLK low to MDIO data output valid	$t_{d(MDCLKL-MDIO)}$	See figure 36		100	ns
	TIMERS ELECTRICAL DATA/TIMING					
Timing requirements for timers inputs 62/ 63/ 64/						
1	Pulse duration, TINPLx high	$t_{w(TINPH)}$	TINP0L, if TIMERCTL.TINP0SEL = 0 [default]	2P		ns
			TINP0L, if TIMERCTL.TINP0SEL = 1	0.33P		
			TNP1L	2P		
2	Pulse duration, TINPLx low	$t_{w(TINPL)}$	TINP0L, if TIMERCTL.TINP0SEL = 0 [default]	2P		
			TINP0L, if TIMERCTL.TINP0SEL = 1	0.33P		
			TNP1L	2P		
Switching characteristics for timer output 62/						
3	Pulse duration, TOUTLx high	$t_{w(TOUTH)}$	See figure 37	P		ns
4	Pulse duration, TOUTLx low	$t_{w(TOUTL)}$		P		
	PWM0/1/2 ELECTRICAL DATA/TIMING					
Switching characteristics for PWM0/1/2 Outputs						
1	Pulse duration, PWMx high	$t_{w(PWMH)}$	See figure 38	37		ns
2	Pulse duration, PWMx low	$t_{w(PWML)}$		37		
3	Transition time, PWMx	$t_{t(PWM)}$			5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

No.	Test	Symbol	Test condition 2/ Device type: All	Limits Min	Limits Max	Unit
	VLYNQ ELECTRICAL DATA/TIMING					
Timing requirements for VLYNQ_CLK input						
1	Cycle time, VLYNQ_CLK	$t_{c(VCLK)}$	See figure 39	10		ns
2	Pulse duration, VLYNQ_CLK high	$t_{w(VLKH)}$		3		
3	Pulse duration, VLYNQ_CLK low	$t_{w(VLKL)}$		3		
Switching characteristics for VLYNQ_CLK output						
1	Cycle time, VLYNQ_CLK	$t_{c(VCLK)}$	See figure 40	10		ns
2	Pulse duration, VLYNQ_CLK high	$t_{w(VLKH)}$		4		
3	Pulse duration, VLYNQ_CLK low	$t_{w(VLKL)}$		4		
Switching characteristics for transmit data for the VLYNQ module						
1	Delay time, VLYNQ_CLK high to VLYNQ_TXD[3:0] invalid	$t_{d(VCLKH-TXD)}$	See figure 40	2.25		ns
2	Delay time, VLYNQ_CLK high to VLYNQ_TXD[3:0] valid	$t_{d(VCLKH-TXDV)}$			12	
Timing requirements for receive data for the VLYNQ module 65/			See figure 40			
3	Setup time, VLYNQ_RXD[3:0] valid before VLYNQ_CLK high	$t_{su(RXDV-VCLKH)}$	RTM disabled, RTM sample = 3	1.75		ns
			RTM enabled	65/		
4	Hold time, VLYNQ_RXD[3:0] valid after VLYNQ_CLK high	$t_{h(VCLKH-RXDV)}$	RTM disabled, RTM sample = 3	3		
			RTM enabled	65/		
	GPIO PERIPHERAL INPUT/OUTPUT ELECTRICAL DATA/TIMING					
Timing requirements for GPIO inputs 66/						
1	Pulse duration, GP[x] input high	$t_{w(GPIH)}$	See figure 41	2C 67/		ns
2	Pulse duration, GP[x] input low	$t_{w(GPIL)}$		2C 67/		
Switching characteristics for GPIO outputs						
3	Pulse duration, GP[x] input high	$t_{w(GPIH)}$	See figure 41	2C 67/ 68/		ns
4	Pulse duration, GP[x] input low	$t_{w(GPIL)}$		2C 67/ 68/		
	JTAG ELECTRICAL DATA/TIMING					
Timing requirements for JTAG test port						
1	Cycle time, TCK	tc(TCK)	See figure 42	33		ns
3	Setup time, TDI/TMS/$\overline{TRST}$ valid before TCK high	$t_{su(TDIV-TCKH)}$		2.5		
4	Hold time, TDI/TMS/$\overline{TRST}$ valid after TCK high	$t_{h(TCKH-TDIV)}$		16.5		
Switching characteristics for JTAG test port						
2	Dealy time, TCK low to TDO valid	$t_{d(TCKL-TDOV)}$	See figure 42	0	14	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ Over recommended ranges of supply voltage and operating temperature in the recommended operating conditions table. (Unless otherwise noted.)
3/ These rated numbers are from PCI specification. The DC specification and AC specification are defined in manufacturer data.
4/ I_I applies to input only pins and bi-directional pins. For input only pins, I_I indicates the input leakage current. For bi-directional pins, I_I includes input leakage current and off-state (hi-Z) output leakage current.
5/ Applies only to pins with an internal pulllup (IPU) or pull down (IPD) resistor
6/ PCI input leakage currents include Hi-Z output leakage for all bidirectional buffers with 3-state outputs.
7/ I_{OZ} applies to output only pins, indicating off state (hi-Z) output leakage current.
8/ Measured under the following conditions: 60% DSP CPU utilization doing typical activity (peripheral configurations, other housekeeping activities); DDR2 Memory Controller at 50% utilization (135 MHz), 50% writes, 32 bits, 50% bit switching; 2-MHz McBSP0 at 100% utilization and 50% switching; Timer0 at 100% utilization. The actual current draw varies across manufacturing processes and is highly application dependent. The C642x DSP device are offered in two basic options: lower power option and high performance option. Low power device offer low power consumption across temperature and voltage when compared with high performance devices. However, high performance devices offer higher operating speeds. For more details on core and I/O activity, as well as information relevant to board power supply design, see manufacturer data.
9/ C = 1/MXI clock frequency in ns. The device clock source must be stable and at a valid frequency prior to meeting the $t_{w(RESET)}$ requirement.
10/ For the list of boot and configuration pins, see manufacturer data.
11/ C = 1/CLJKIN1 clock frequency in ns.
12/ For audio appliance, stability of the input clock is very important. The user should select crystal with low enough ppm to ensure good audio quality for the specific application.
13/ MXI/CLKIN input clock is used for both PLL controllers (PLLC1 and PLLC2).
14/ Applies to “tape and reel” part number counterparts as well. For more information see manufacturer data.
15/ C = CLKIN cycle time in ns. For example, when MXI/CLKIN frequency is 25 MHz, use C = 40 ns.
16/ The MXI/CLKIN frequency and PLL multiply factor should be chosen such that the resulting clock frequency is within the specific range for CPU operating frequency. For example, for a -6 speed device with a 25 MHz CLKIN frequency, the PLL multiply factor should be ≤ 24.
17/ The reference points for the rise and fall transactions are measured at V_{IL} MAX and V_{IH} MIN.
18/ For more details on the PLL multiplier factors, see manufacturer data.
19/ The reference points for the rise and fall transactions are measured at V_{OL} MAX and V_{OH} MIN.
20/ P = 1/CLKOUT0 clock frequency in ns. For example, when CLKOUT0 frequency is 30 MHz, use P = 33.3 ns.
21/ E = SYSCLK3 period in ns for EMIFA. For example for running the DSP CPU at 600 MHz, use E = 10 ns.
22/ Setup before end of STROBE phase (If no extended wait state are inserted) by which EM_WAIT must be asserted to add extended wait states. See figure 11 and 12 describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.
23/ RS = Read setup, RST = Read Strobe, RH = Read Hold, WS = Write Setup, WST = Write Strobe, WH = Write Hold, TA = Turn Around, EW = Extend Wait mode, SS = Select Strobe mode. These parameters are programmed via the Asynchronous n Configuration and Asynchronous Wait Cycle Configuration Registers.
24/ When EW = 1, the EMIF will extend the strobe period up to 4,096 additional cycles when the EM_WAIT pin is asserted by the external device.
25/ DDR_CLK cycle time = 2 x PLL2_SYSCLK1 cycle time.
26/ The PLL2 controller must be programmed such that the resulting DDR_CLK clock frequency is within the specified range.
27/ U = UART baud time = 1/programmed baud rate.

TABLE I. Electrical performance characteristics - Continued.

28/ The I^2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.

29/ A fast mode I^2C bus device can be used in a standard mode I^2C bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r max + $t_{su(SDA-SCLH)}$ = 1000 + 250 = 1250 ns (according to the standard mode I^2C bus specification) before the SCL line is released.

30/ A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL

31/ The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the low period [$t_{w(SCLL)}$] of the SCL signal.

32/ C_b = total capacitance of one bus line in pF. If mixed with HS mode devices, faster fall time are allowed.

33/ $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$:[NOT($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{HCS}}$.

34/ M = SYSCLK3 period = (CPU clock frequency)/6 in ns. For example, when running parts at 600 MHz, use M = 10 ns.

35/ Select signals include: HCNTL[1:0], HR/$\overline{\text{W}}$ and HHWIL.

36/ By design, whenever $\overline{\text{HCS}}$ is driven inactive (high), HPI will $\overline{\text{HRDY}}$ active low.

37/ For HPI Read. Applies to conditions where data is already residing in HPID/FIFO:
Case 1: HPIC or HPIA read.
Case 2: First half word of HPID read with auto-increment and data is already in Read FIFO.
Case 3: Second half word of HPID read with or without auto-increment.

38/ For HPI Write, $\overline{\text{HRDY}}$ can go high (not ready) for these HPI Write conditions; otherwise, $\overline{\text{HRDY}}$ stays low (ready):
Case 1: HPID write when Write FIFO is full (can happen to either half word)
Case 2: HPIA write (can happen to either half word)
Case 3: HPID write without auto-increment (only happens to second half-word)

39/ CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

40/ P = SYSCLK3 period in ns. For example, when running parts at 600 MHz, use M = 10 ns.

41/ Use whichever value is greater. Minimum CLKR/X cycle times must be met, even when CLKR/X is generated by an internal clock source. Minimum CLRK/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.

42/ This parameter applies to the maximum McBSP frequency. Operate serial clock (CLKR/X) in the reasonable range of 40/60 duty cycle.

43/ Minimum delay times also represent minimum output hold times.

44/ Minimum CLKR/X cycle times must be met, even when CLKR/X is generated by an internal clock source. Minimum CLRK/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.

45/ Use whichever value is greater.

46/ C = H or L
S = Sample rate generator input clock = P if CLKSM = 1 (P = SYSCLK3 period)
= Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd
CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the maximum limit (see 40/ above).

47/ Extra delay from CLKX high to DX valid applies only to the first data bit of a device, if and only if DXENA = 1 in SPCR.
If DXENA = 0, then D1 = D2 = 0
If DXENA = 1, then D1 = 6P, D2 = 12P

48/ Extra delay from FSX high to DX valid applies only to the first data bit of a device, if and only if DXENA = 1 in SPCR.
If DXENA = 0, then D1 = D2 = 0
If DXENA = 1, then D1 = 6P, D2 = 12P

49/ For all SPI Slave mode, the rate of internal clock CLKG must be at least 8 times faster than that of the SPI data rate. User should program sample rate generator to achieve maximum CLKG by setting CLKSM = CLKGDV = 1.

50/ S = Sample rate generator input clock = 2P if CLKSM = 1 (P = SYSCLK3 period)
= Sample rate generator input clock = 2P_clks if CLKSM = 0 (P_clks = CLKS period)
T = CLKX period = (1 + CLKGDV)
H = CLKX period = (1 + CLKGDV)*S if CLKGDV is even
H = (CLKGDV + 1)/2 * S if CLKGDV is odd
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
L = (CLKGDV + 1)/2 * S if CLKGDV is odd

51/ FSRP = FSXP = 1. As a SPI Master, FSX is inverted to provide active low slave enable output. As a Slave, the active low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for Master McBSP
CLKXM = CLKRM =FSXM = FSRM = 0 for Slave McBSP

52/ FSX should be low before the rising edge of clock to enable Slave devices and then begin a SPI transfer at the rising edge of the Master clock (CLKX).

53/ ACLKX internal: ACLKXCTL.CLKXM = 1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 0
ACLKX external output: ACLKXCTL.CLKXM = 0, PDIR.ACLKX = 1
ACLKR internal: ACLKRCTL.CLKRM = 1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 0
ACLKR external output: ACLKRCTL.CLKRM = 0, PDIR.ACLKR = 1

54/ Ther is a clock ratio requirement between the system infrastructure clock, SYSCLK3, and the McASP0 bit clocks, ACLKR/ACLKX. Fpr proper device operation, the ACLKR/ACLKX must be no faster than = of SYSCLK3 frequency.

55/ A = (ACLKR/X period)/2 in ns. For example, when ACLKR/X period is 25 ns, use A = 12.5 ns.

56/ AH = (AHCLKR/X period)/2 in ns. For example, when AHCLKR/X period is 25 ns, use AH = 12.5 ns.

57/ There is a clock rqtio requirement between the system infrastructure clock, SYSCLK3, and the EMAC receive/transmit input clocks, MRCLK and MTCLK. For proper device operation, the SYSCLK3 frequency must be faster than 12.5 MHz.

58/ Receive selected signals include: MRXD3-MRXD0, MRXDV, and MRXER.

59/ Transmit select signals include: MTXD3-MTXD0, and MTXEN

60/ Receive selected signals include: RMRXD1-RMRXD0, RMCRSDV, and RMRXER

61/ Transmit selected signals include: RMTXD1-RMTXD0, and RMTXEN

62/ P = MXI/CLKIN cycle time in ns. For example, when MXI/CLKIN frequency is 25 MHz, use P = 40 ns.

63/ The TIMERCTL.TINP0SEL field in the System Module determines if the TINP0L input directly goes to Timer 0 (TIMERCTL.TINP0SEL = 0), or if the TINP0L input is first divided down by 6 before going to Timer 0 (TIMERCTL.TINP0SEL = 1).

64/ TINP1L input goes directly to Timer 1.

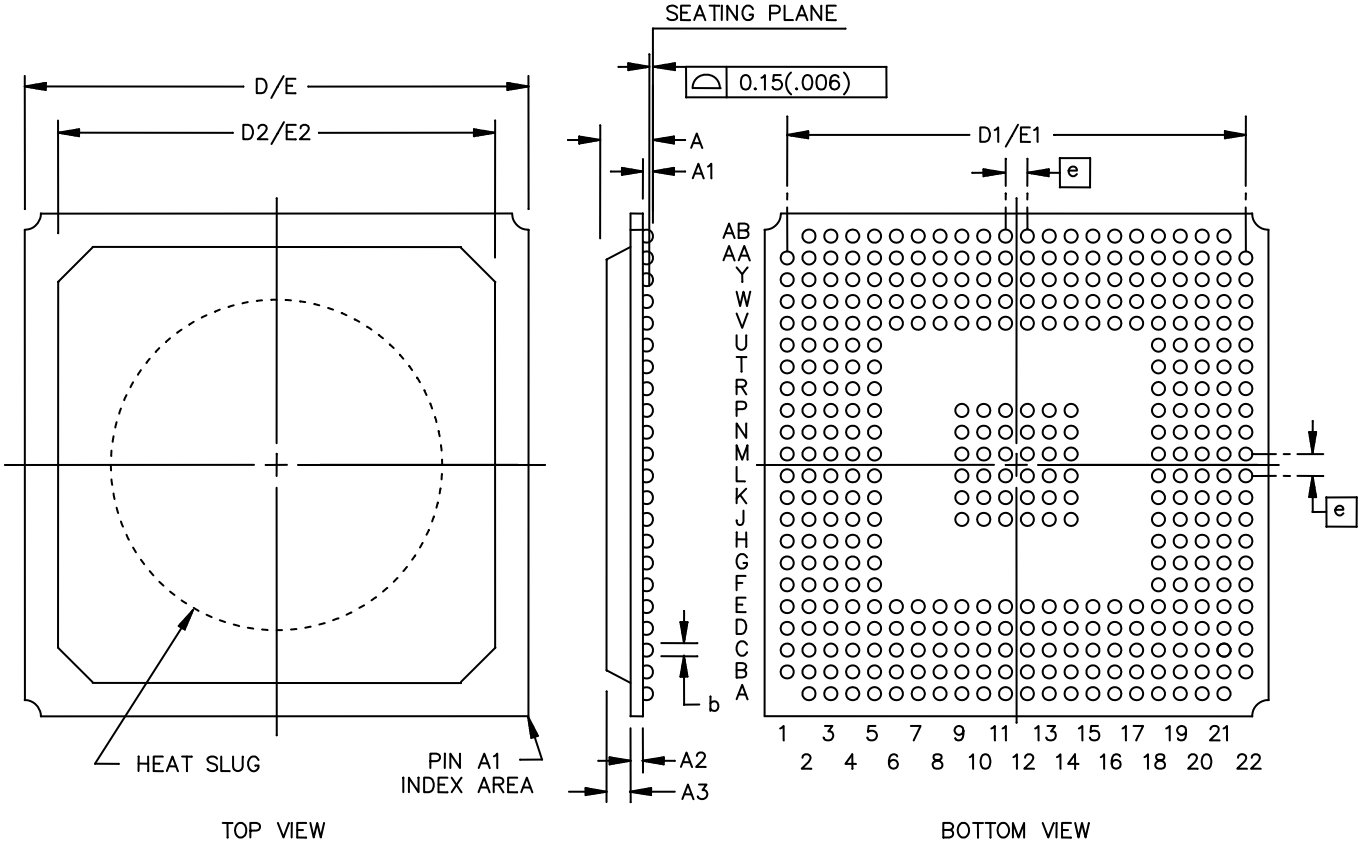
65/ The VLYNQ receive timing manager (RTM) is a serial receive logic designed to eliminate setup and hold violation that could occur in traditional input signals. RTM logic automatically selects the setup and hold timing from one of eight data flops. When RTM logic is disabled, the setup and hold timing from the default data flop (3) is used.

66/ The pulse width given is sufficient to generate a CPU interrupt or an EDMA event. However, if a user wants to have DSP recognize the GP[x] input changes through software polling of the GPIO register, the GP[x] input duration must be extended to allow enough time to access the GPIO register through the internal bus.

67/ C = SYSCLK3 period in ns. For example, when running parts at 600 MHz, use C = 10 ns.

68/ This parameter value should not be used as a maximum performance specification. Actual performance of back to back accesses of the GPIO is dependent upon internal bus activity.

Case X



Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		2.48	D/E	22.80	23.20
A1	0.40	0.60	D1/E1	21.00 TYP	
A2	0.52	0.65	D2/E2	19.30	19.70
A3	1.12	1.22	e	1.00 BSC	
b	0.50	0.70			

Notes:
1. This drawing is subject to change without notice.
2. Thermally enhanced plastic package with heat slug (HSL).
3. Falls within JEDEC MO-151.

FIGURE 1. Case outline.

Case X

FIGURE 2. Terminal connections.

Case X – Continued.

	12	13	14	15	16	17	18	19	20	21	22	
AB	DDR_A[7]	DDR_A[4]	DDR_A[1]	DDR_A[0]	DDR_D[18]	DDR_D[21]	DDR_D[22]	DDR_D[25]	DDR_D[28]	DV_{DDR2}	DV_{DDR2}	AB
AA	DDR_A[9]	DDR_A[6]	DDR_A[3]	DDR_DQS[2]	DDR_D[16]	DDR_D[19]	DDR_DQS[3]	DDR_D[23]	DDR_D[26]	DDR_D[30]	V_{SS}	AA
Y	DDR_A[8]	DDR_A[5]	DDR_A[2]	DDR_DQM[2]	DDR_D[17]	DDR_D[20]	DDR_DQM[3]	DDR_D[24]	DDR_D[27]	DDR_D[29]	DDR_D[31]	Y
W	DDR_ZN	DDR_ZP	DDR_VDDDLL	DDR_VSSDLL	RSV5	DV_{DDR2}	DDR_VREF	DV_{DDR2}	V_{SS}	V_{SS}	V_{SS}	W
V	DV_{DDR2}	V_{SS}	DV_{DDR2}	V_{SS}	DV_{DDR2}	V_{SS}	DV_{DDR2}	V_{SS}	RSV12	RSV7	RSV6	V
	12	13	14	15	16	17						
U							V_{SS}	V_{SS}	RSV11	RSV15	RSV8	U
T							V_{SS}	RSV14	RSV13	RSV9	RSV10	T
R							V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	R
P	CV_{DD}	CV_{DD}	V_{SS}			P	DV_{DD33}	RSV4	DV_{DD33}	V_{SS}	DV_{DD33}	P
N	V_{SS}	V_{SS}	CV_{DD}			N	V_{SS}	DV_{DD33}	PLL_{PWR18}	MXV_{DD}	MXI/ CLKIN	N
M	V_{SS}	V_{SS}	CV_{DD}			M	DV_{DD33}	V_{SS}	DV_{DD33}	MXV_{SS}	MXO	M
	12	13	14				18	19	20	21	22	

FIGURE 2. Terminal connections - Continued.

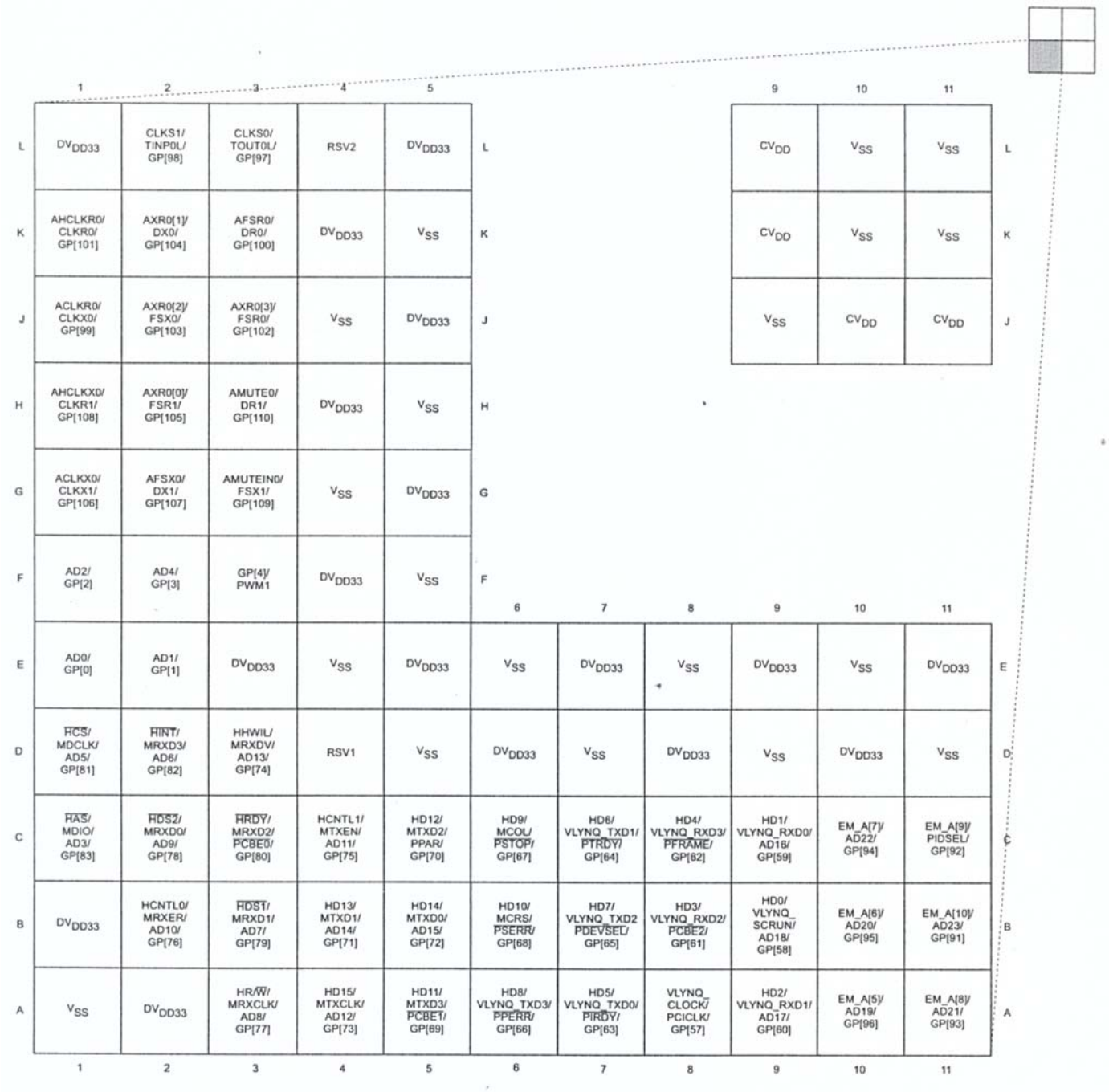


FIGURE 2. Terminal connections - Continued.

Case X – Continued.

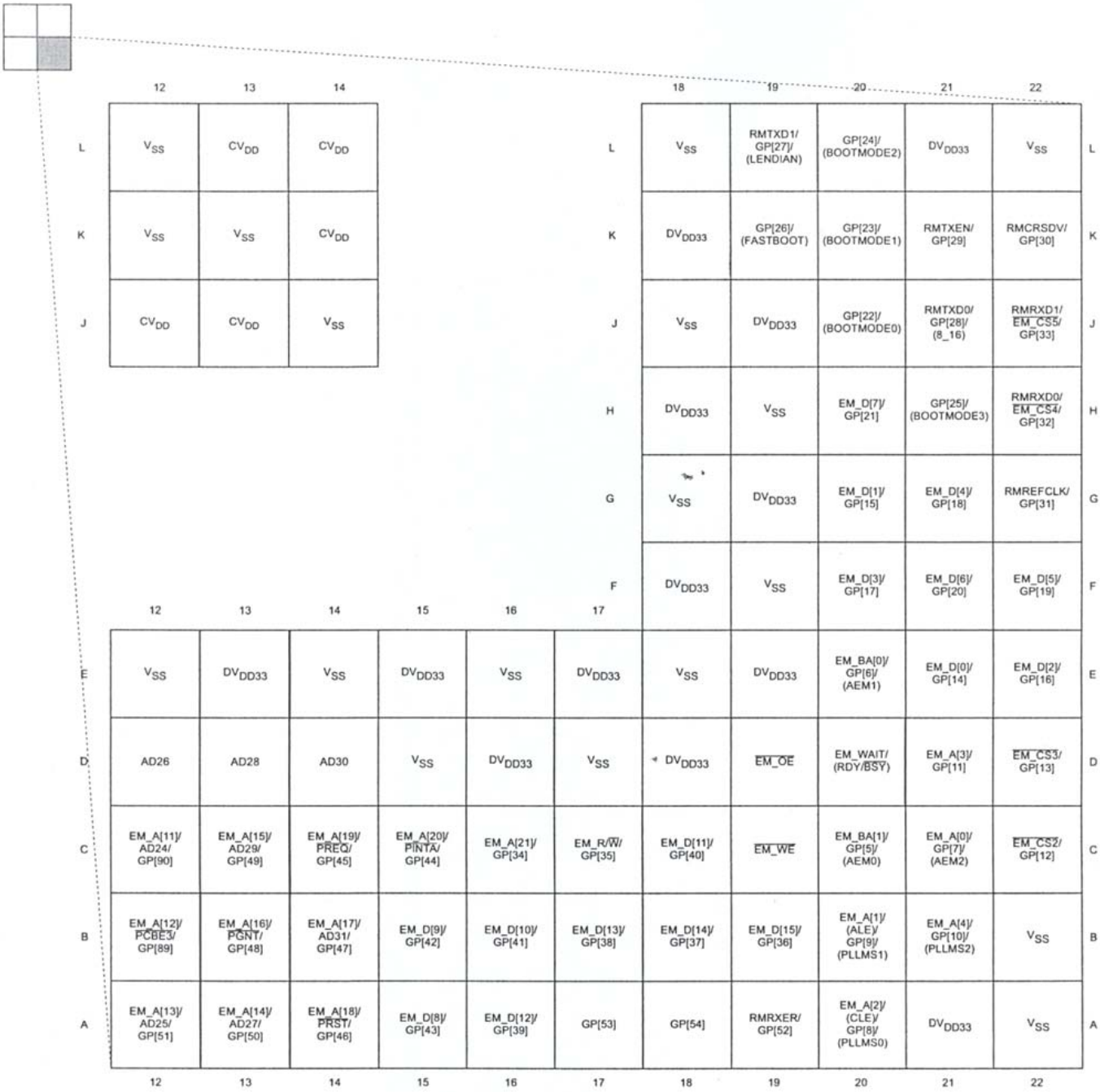


FIGURE 2. Terminal connections - Continued.

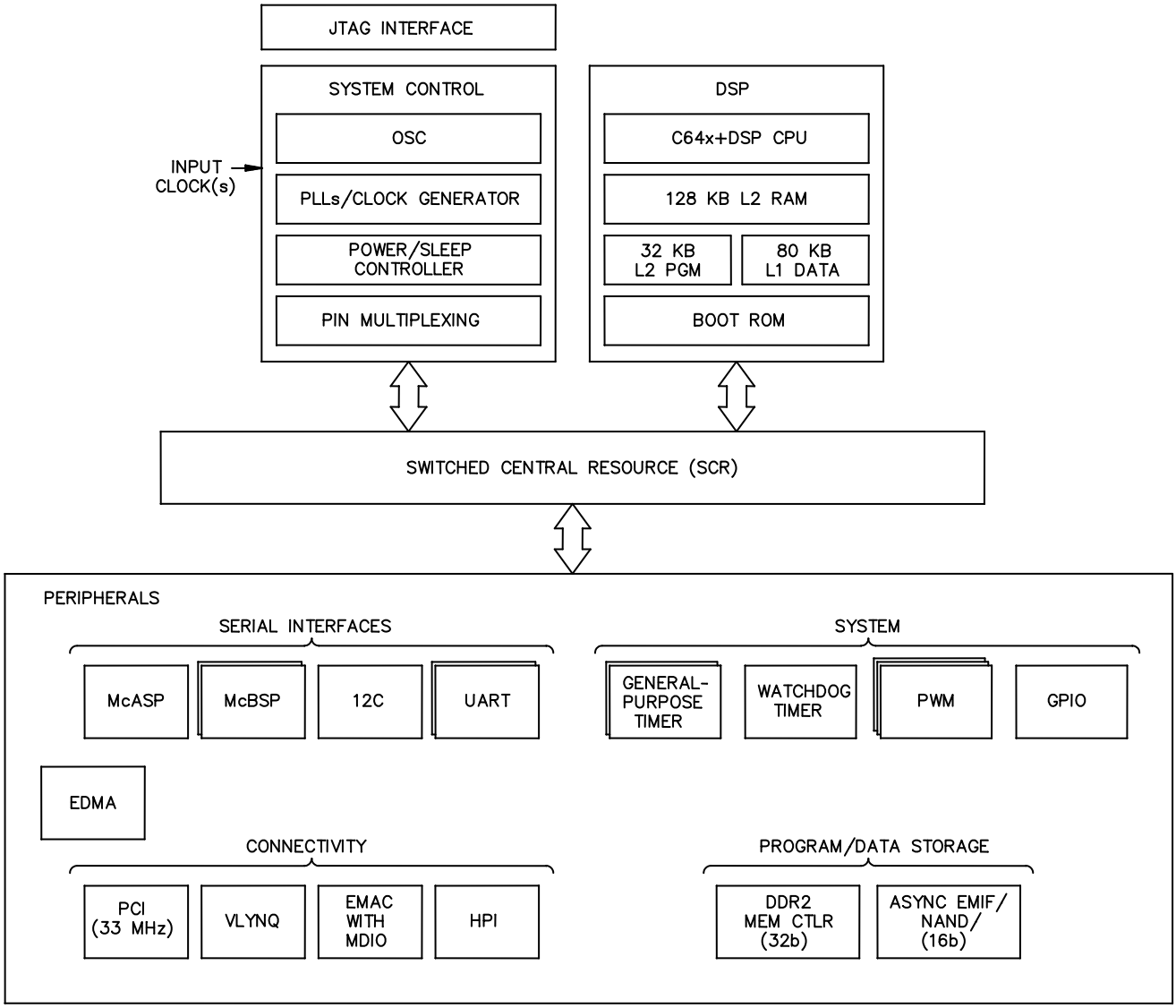
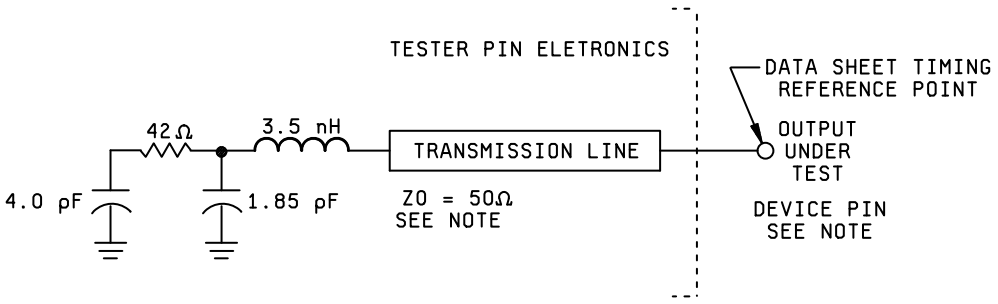


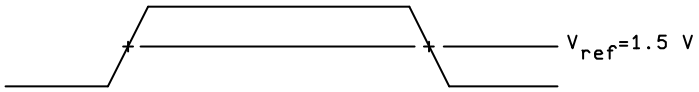
FIGURE 3. Block diagram - Continued.



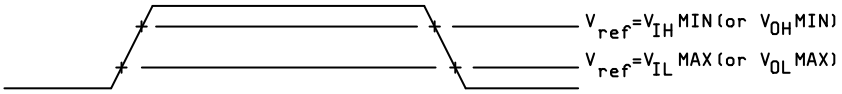
TEST LOAD CIRCUIT FOR AC TIMING MEASUREMENTS

Notes:

1. The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timings.
   Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond ($ V/ns) at the device pin.

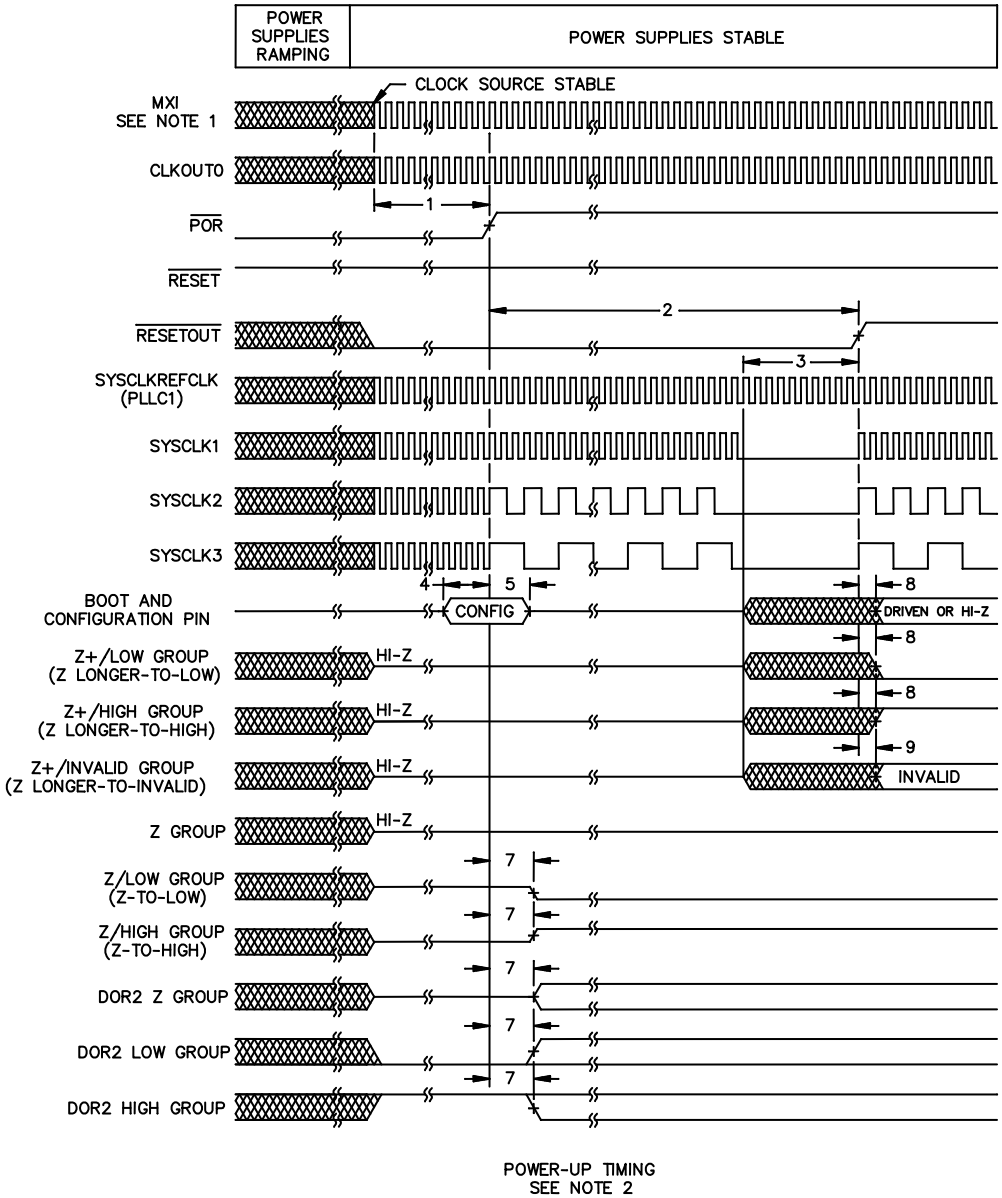


INPUT AND OUTPUT VOLTAGE REFERENCE LEVELS FOR AC TIMING MEASUREMENTS



RISE AND FALL TRANSITION TIME VOLTAGE REFERENCE LEVELS

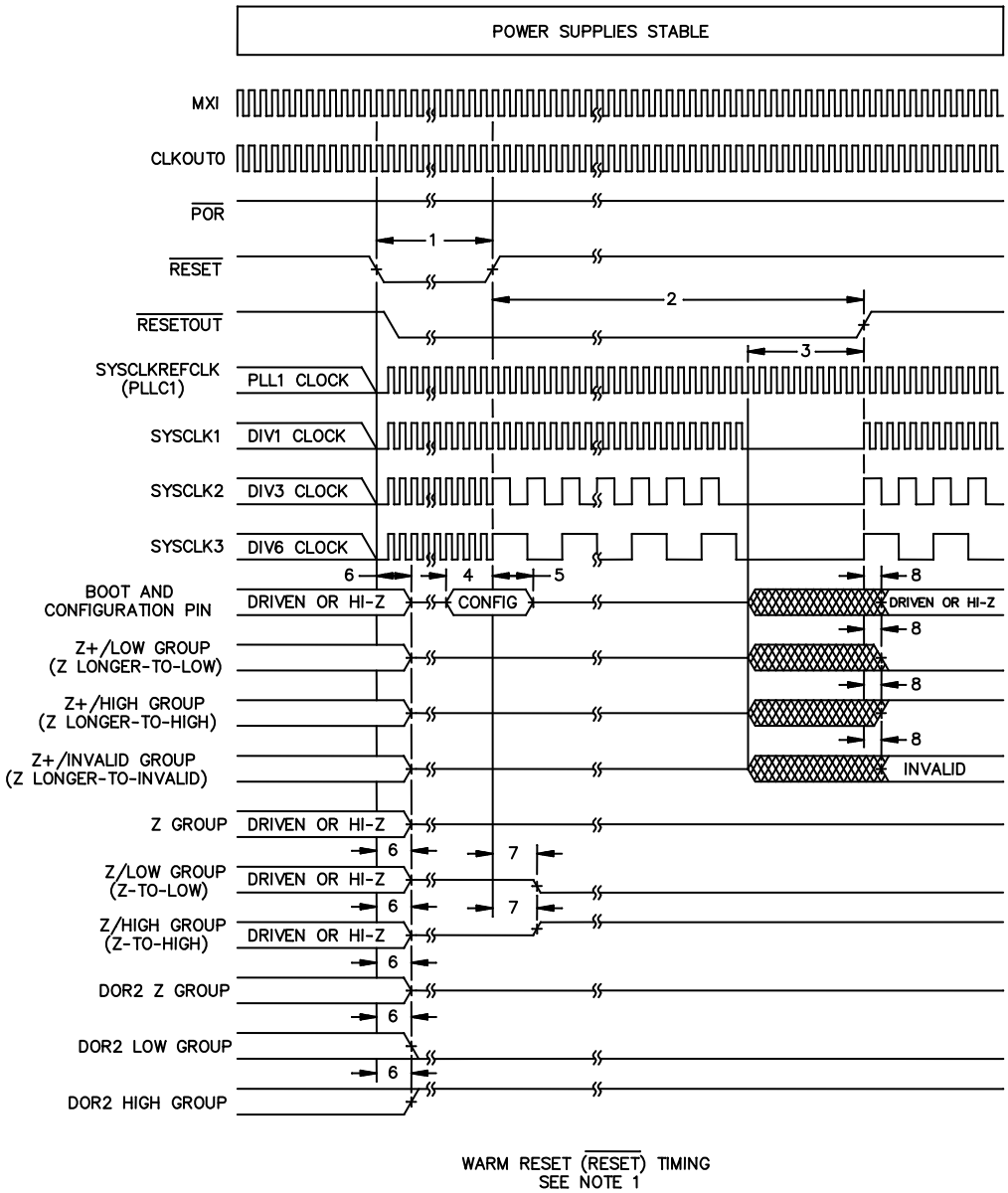
FIGURE 4. Test load circuit for AC timing measurements.



NOTES::

1. Power supplies and MXI must be stable before the start of $t_{w(RESET)}$.
2. Pin reset behavior depends on which peripheral defaults to controlling the multiplexed pin. For more details on what pin group (e.g. Z group, Z/Low group, Z/High group etc.) each pin belongs to, see manufacturer data, Pin Behavior at Reset for more information.

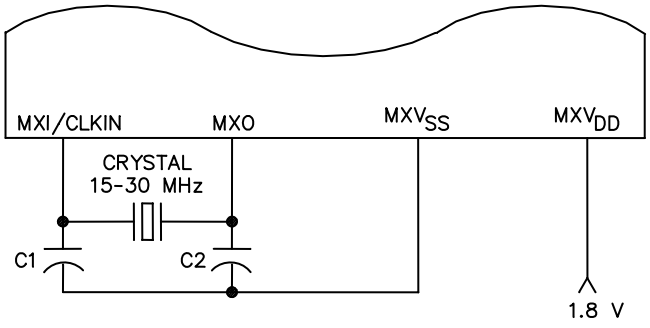
FIGURE 5. Timing waveforms.



NOTES::

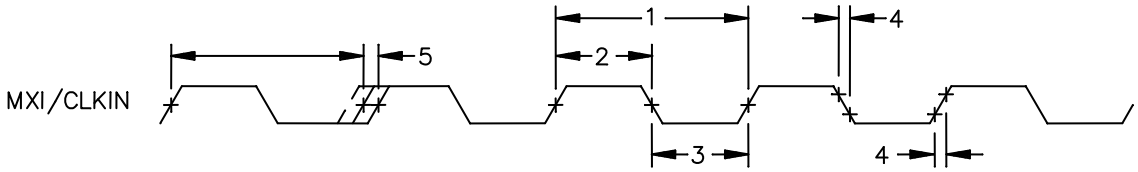
1. Power supplies and MXI must be stable before the start of $t_{w(RESET)}$.
2. Pin reset behavior depends on which peripheral defaults to controlling the multiplexed pin. For more details on what pin group (e.g. Z group, Z/Low group, Z/High group etc.) each pin belongs to, see manufacturer data, Pin Behavior at Reset for more information.

FIGURE 6. Timing waveforms.



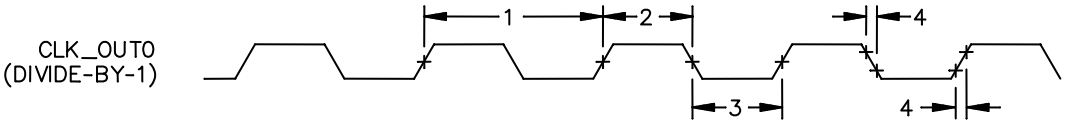
15-30-MHZ SYSTEM OSCILLATOR

FIGURE 7. Timing waveforms.



MXI/CLKIN1 TIMING

FIGURE 8. Timing waveforms.



CLKOUT0 TIMING

FIGURE 9. Timing waveforms.

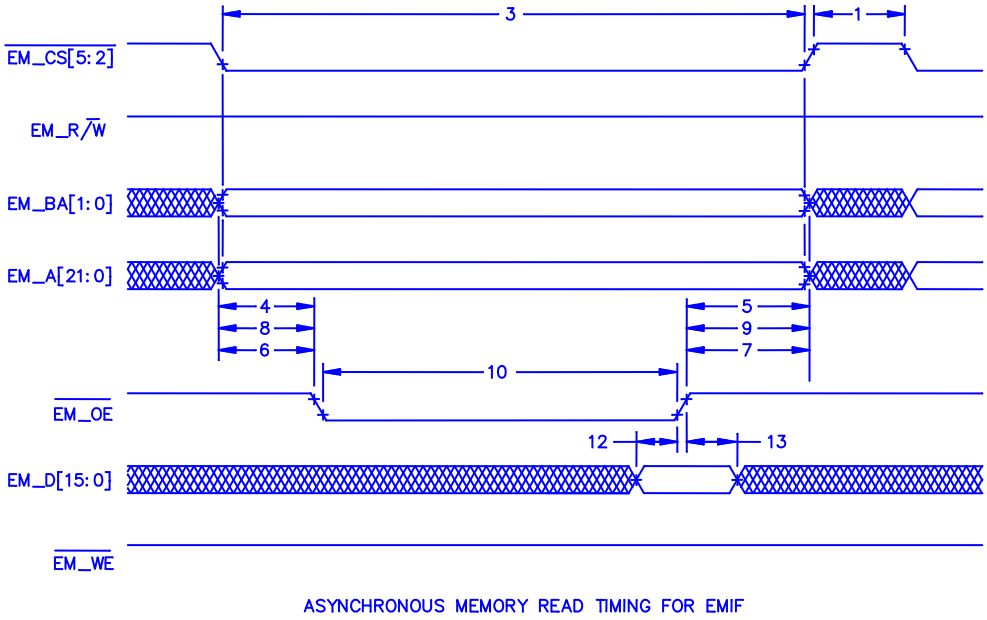


FIGURE 10. Timing waveforms.

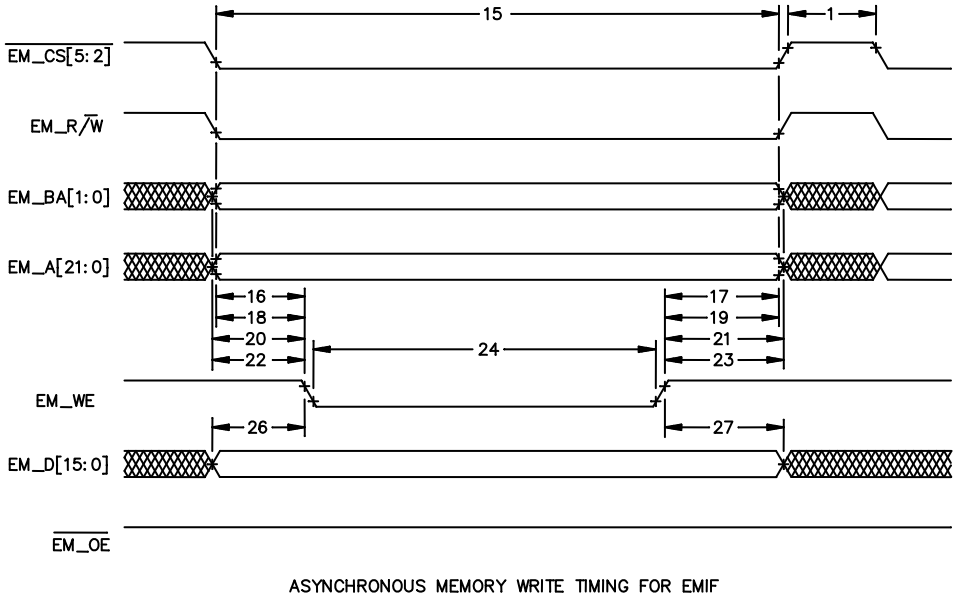
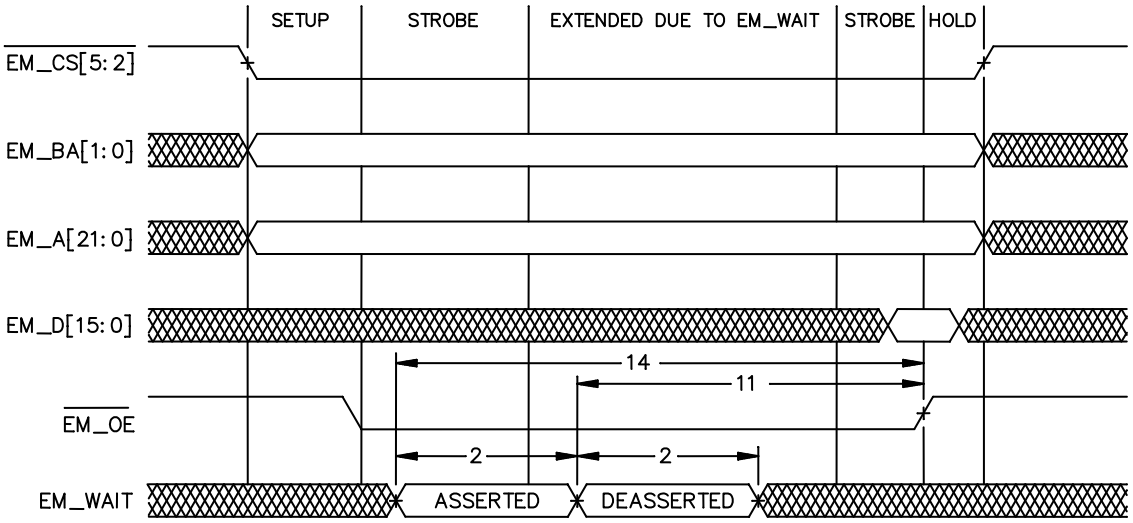
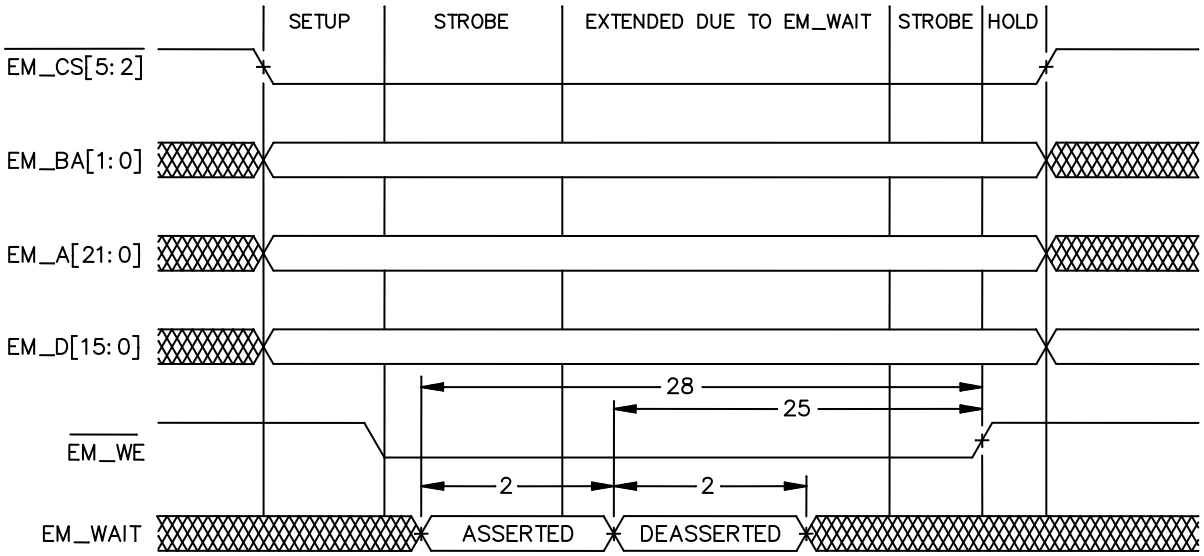


FIGURE 11. Timing waveforms.



EM_WAIT READ TIMING REQUIREMENTS

FIGURE 12. Timing waveforms.



EM_WAIT WRITE TIMING REQUIREMENTS

FIGURE 13. Timing waveforms.

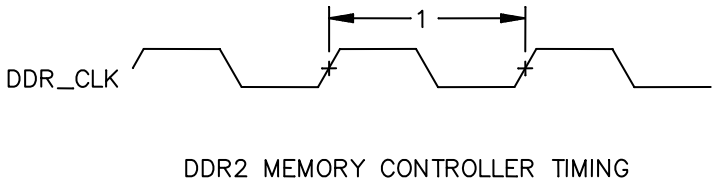


FIGURE 14. Timing waveforms.

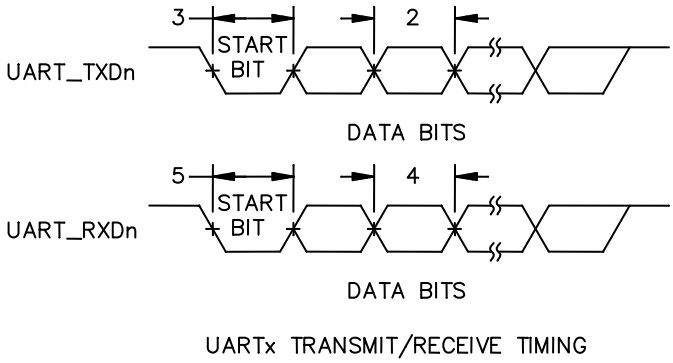


FIGURE 15. Timing waveforms.

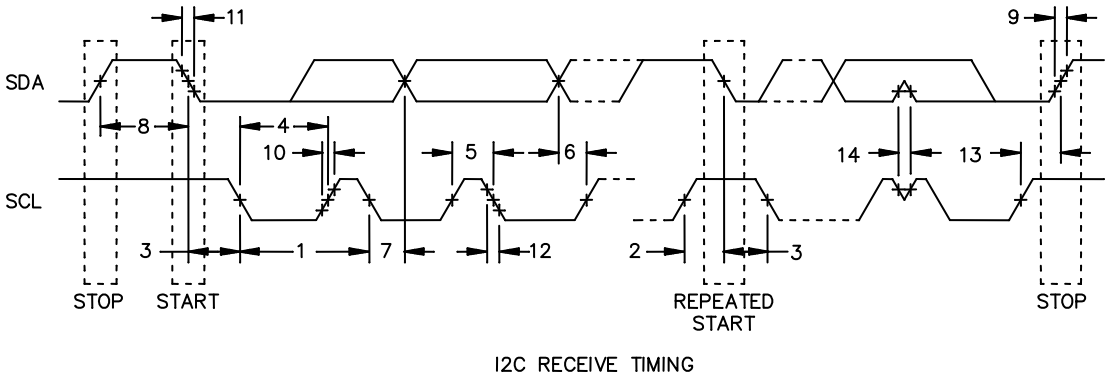


FIGURE 16. Timing waveforms.

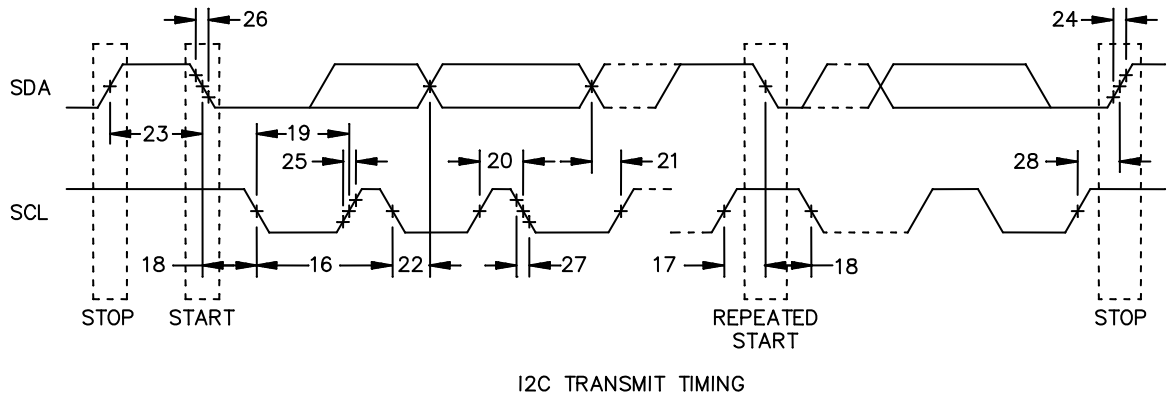
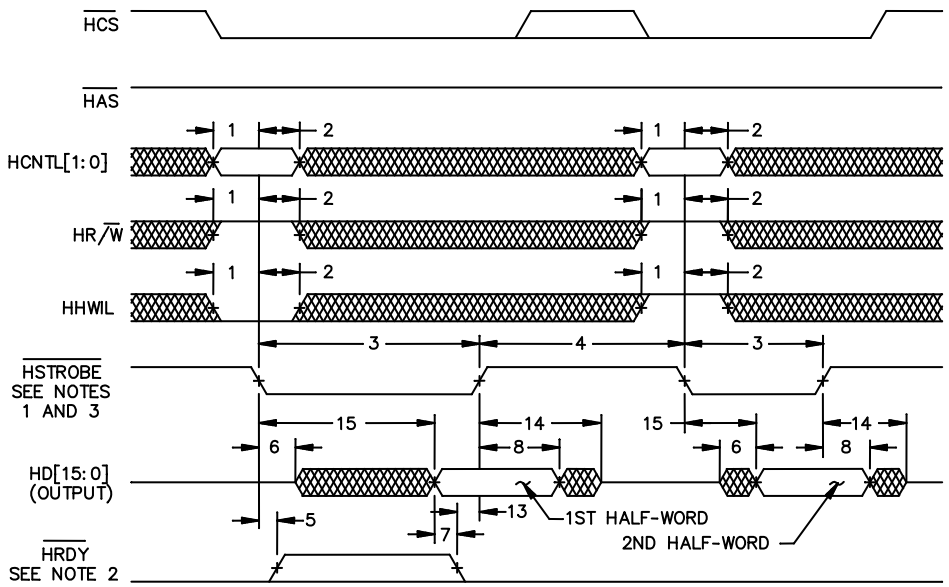


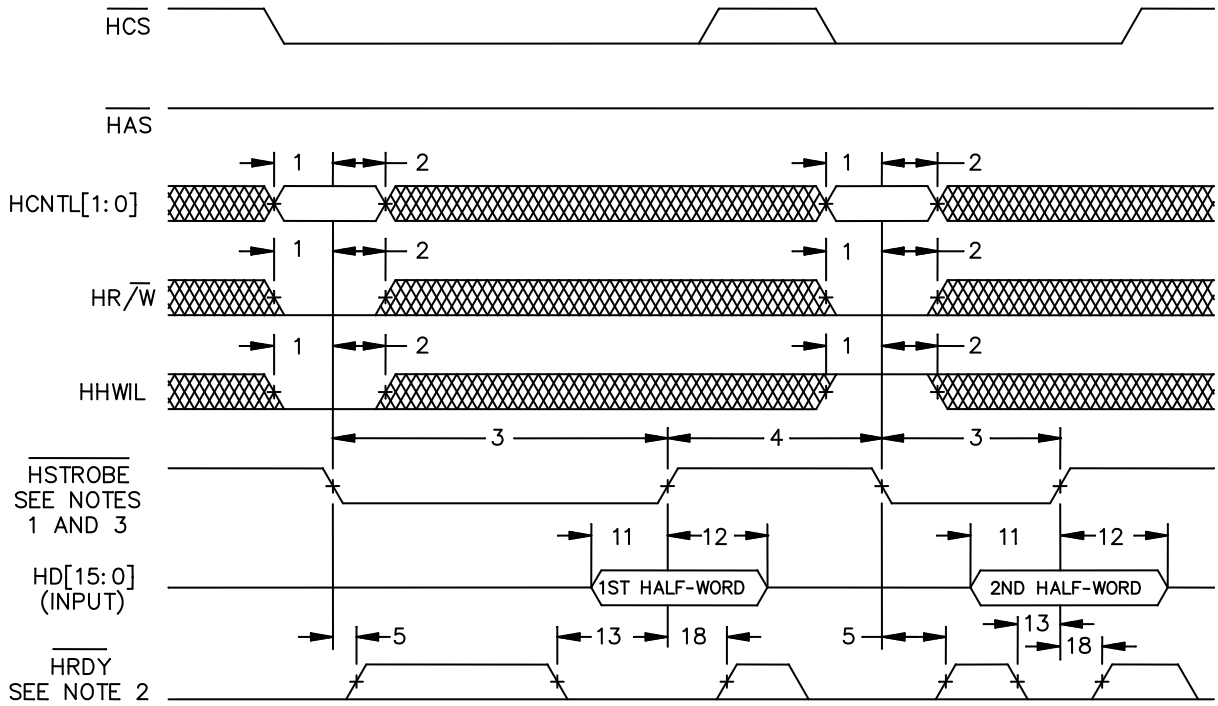
FIGURE 17. Timing waveforms.



NOTES:

1. $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: [NOT ($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{HCS}}$.
2. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on $\overline{\text{HRDY}}$ may or may not occur. For more detailed see manufacturer data.
3. $\overline{\text{HCS}}$ reflect typical $\overline{\text{HCS}}$ behavior when $\overline{\text{HSTROBE}}$ assertion is caused by $\overline{\text{HDS1}}$ or $\overline{\text{HDS2}}$. $\overline{\text{HCS}}$ timing requirements are reflected by parameters for $\overline{\text{HSTROBE}}$

FIGURE 18. Timing waveforms.

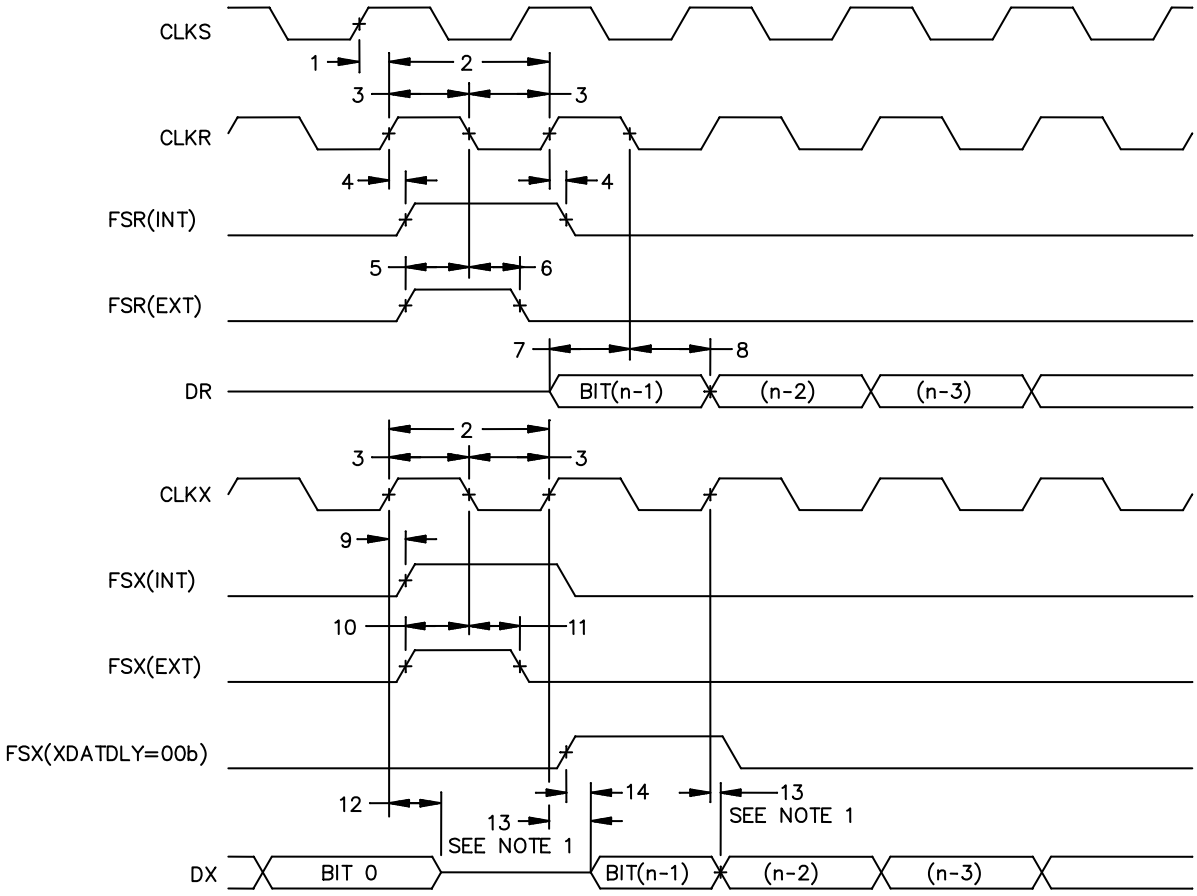


HPI16 WRITE TIMING (HAS NOT USED,TIED HIGH)

NOTES:

1. HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT (HDS1 XOR HDS2)] OR HCS.
2. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on HRDY may or may not occur. For more detailed see manufacturer data.
3. HCS reflect typical HCS behavior when HSTROBE assertion is caused by HDS1 or HDS2. HCS timing requirements are reflected by parameters for HSTROBE

FIGURE 19. Timing waveforms.



MCBSP TIMING
SEE NOTE 2

NOTES:
1. Parameter No 13 applies to the first data bit only when XDATDLY ≠ 0.

FIGURE 20. Timing waveforms.

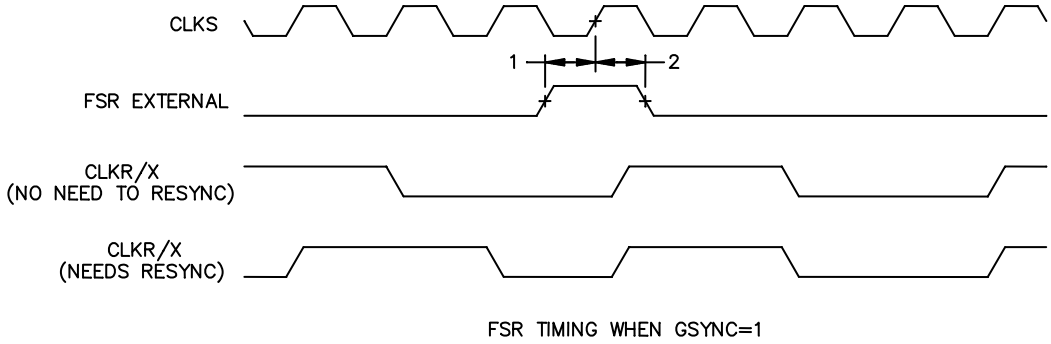


FIGURE 21. Timing waveforms.

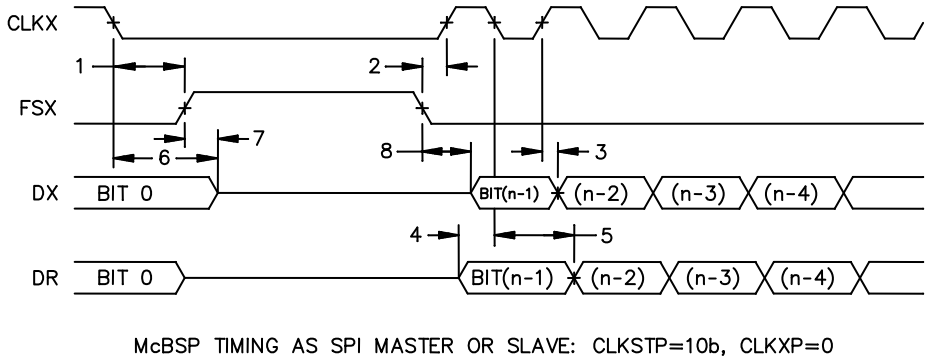


FIGURE 22. Timing waveforms.

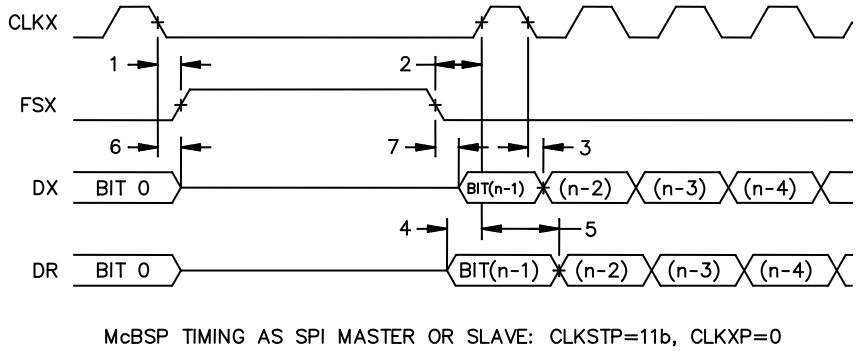


FIGURE 23. Timing waveforms.

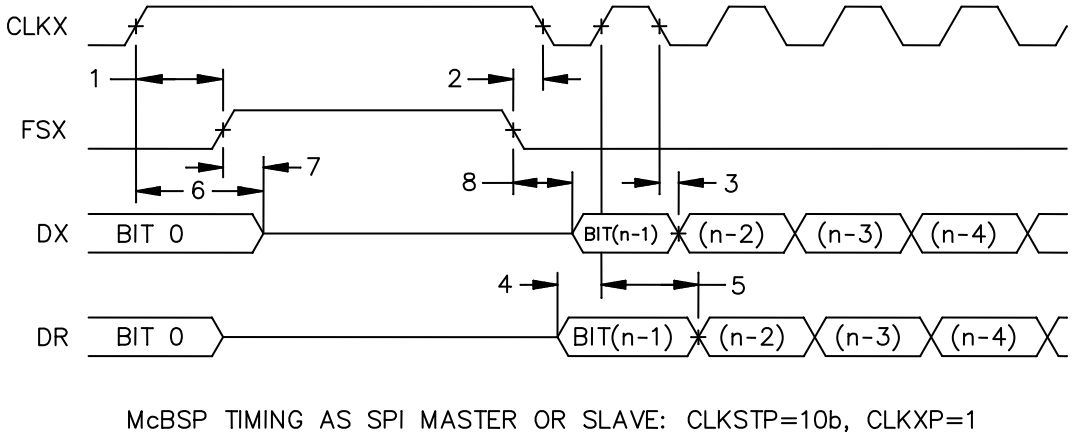


FIGURE 24. Timing waveforms.

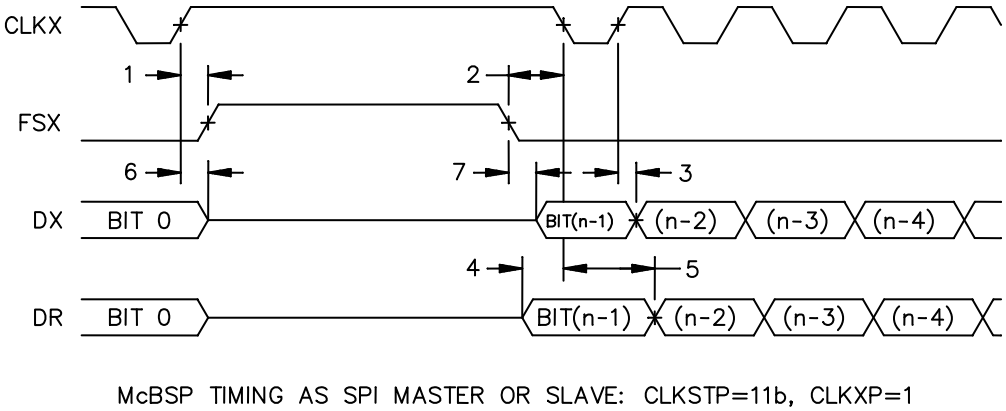
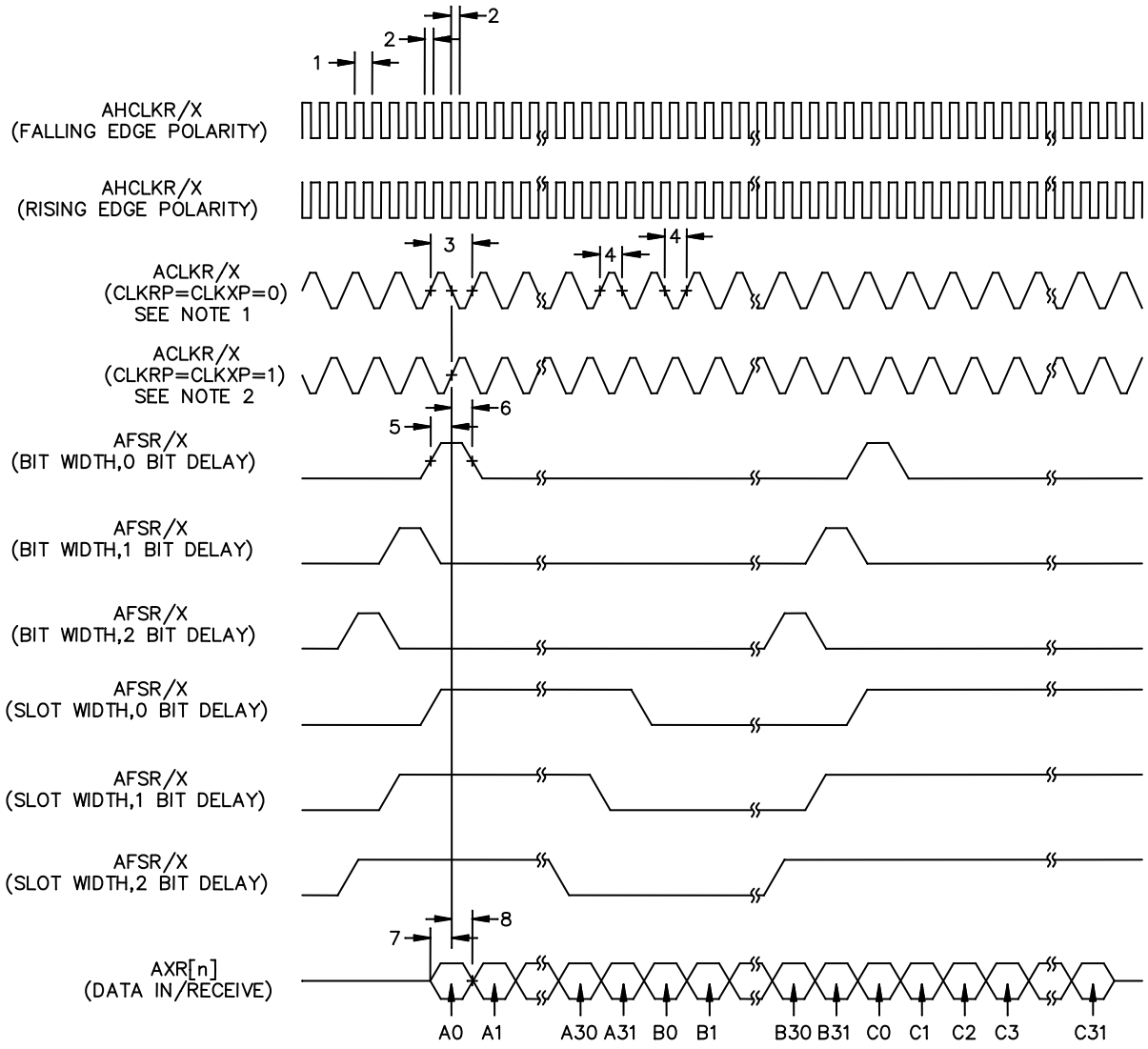


FIGURE 25. Timing waveforms.

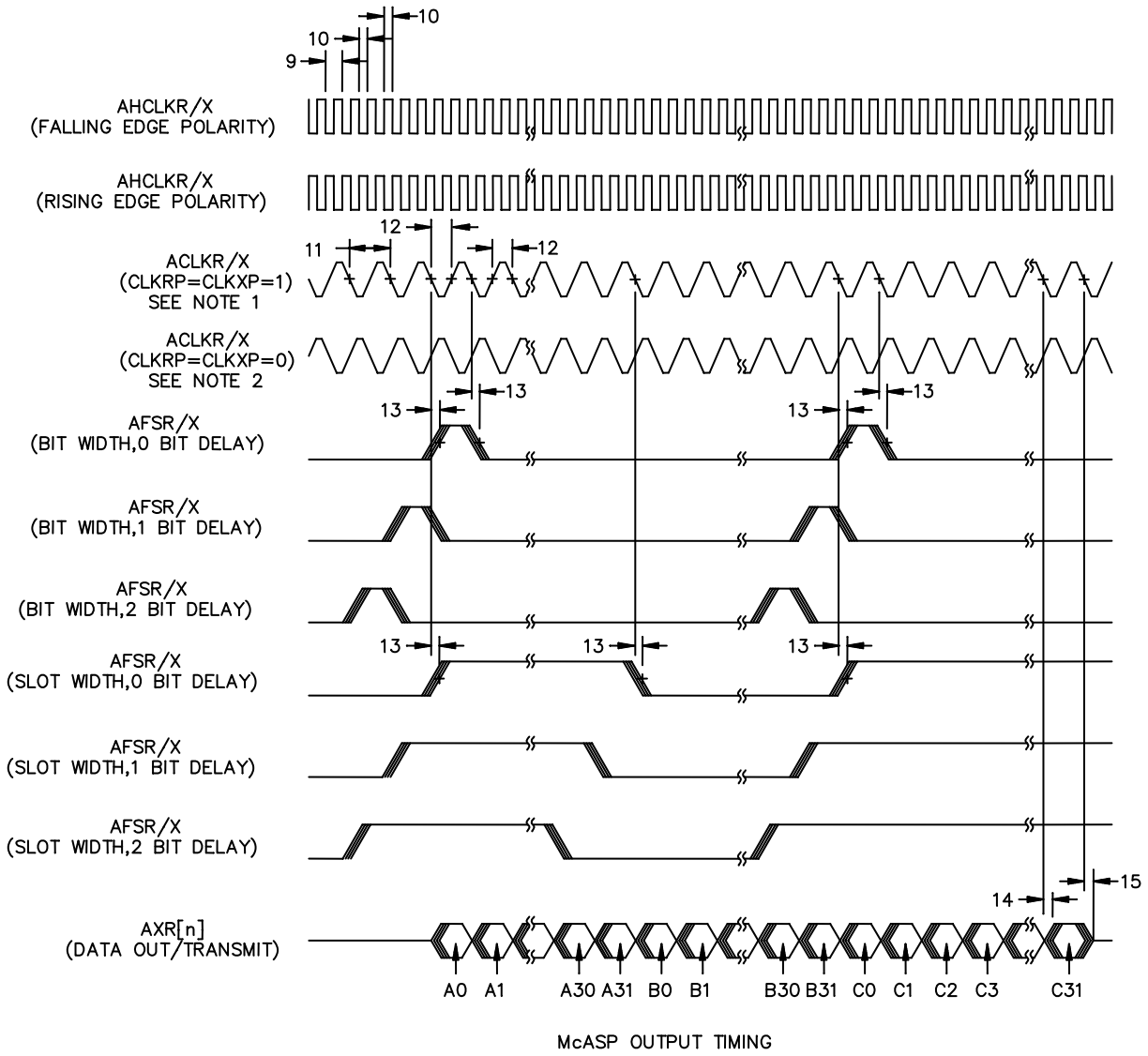


McASP INPUT TIMING

NOTES:

1. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).
2. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).

FIGURE 26. Timing waveforms.

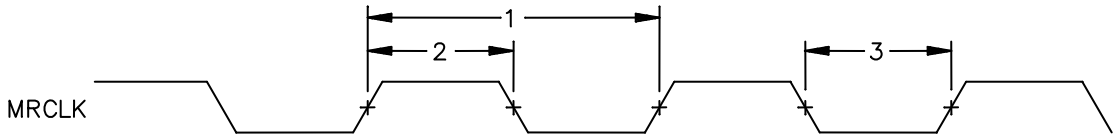


McASP OUTPUT TIMING

NOTES:

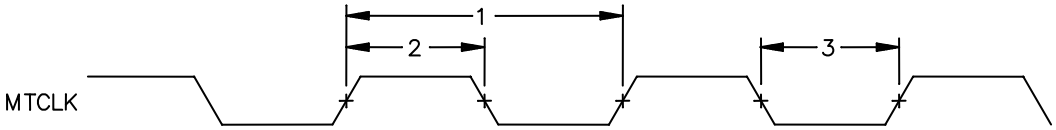
1. For CLKRP = CLKXP = 1, the McASP transmitter is configured for falling edge (to shift data out) and the McASP receiver is configured for rising edge (to shift data in).
2. For CLKRP = CLKXP = 0, the McASP transmitter is configured for rising edge (to shift data out) and the McASP receiver is configured for falling edge (to shift data in).

FIGURE 27. Timing waveforms.



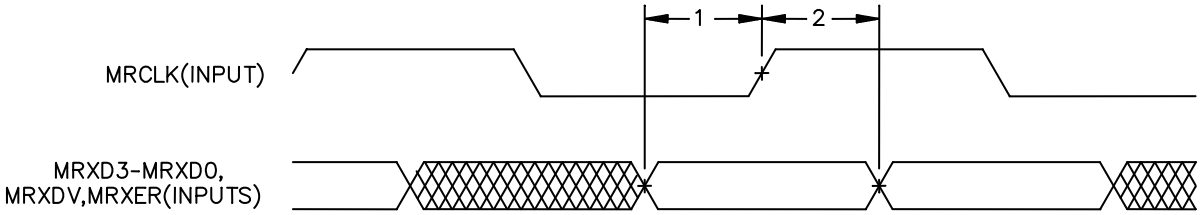
MRCLK TIMING (EMAC-RECEIVE)[MII OPERATION]

FIGURE 28. Timing waveforms.



MTCLK TIMING (EMAC-TRANSMIT)[MII OPERATION]

FIGURE 29. Timing waveforms.



EMAC RECEIVE INTERFACE TIMING [MII OPERATION]

FIGURE 30. Timing waveforms.

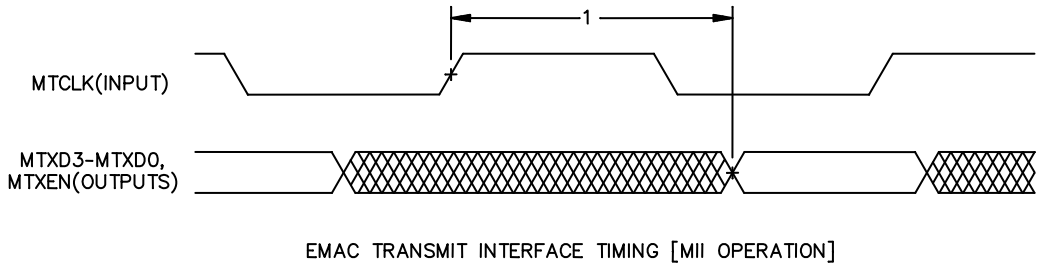


FIGURE 31. Timing waveforms.

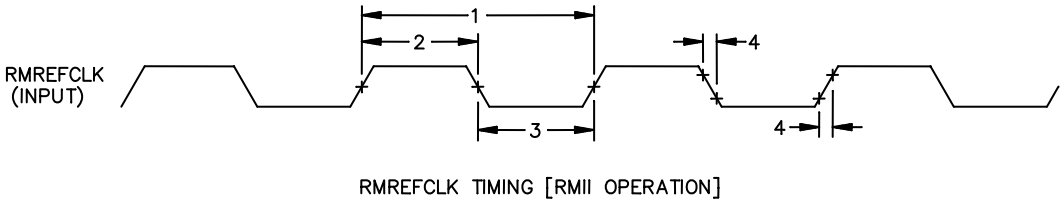


FIGURE 32. Timing waveforms.

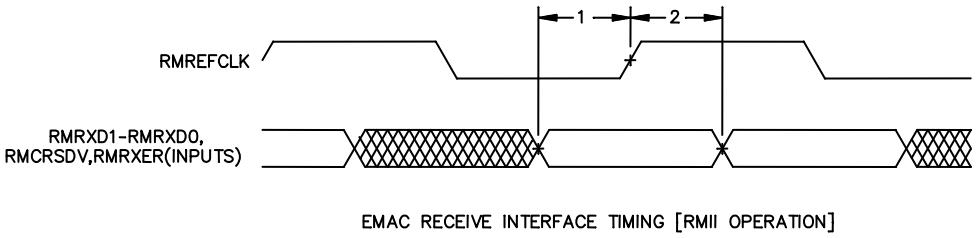


FIGURE 33. Timing waveforms.

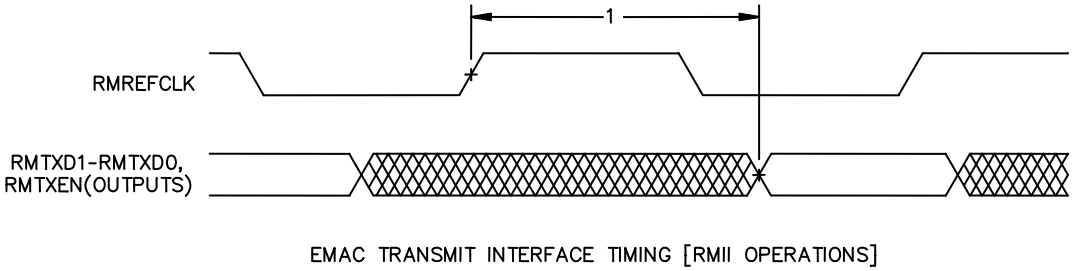


FIGURE 34. Timing waveforms.

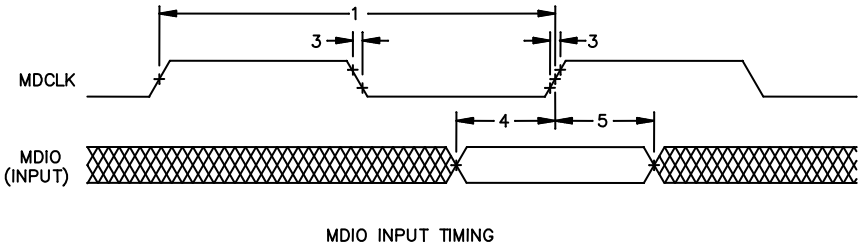


FIGURE 35. Timing waveforms.

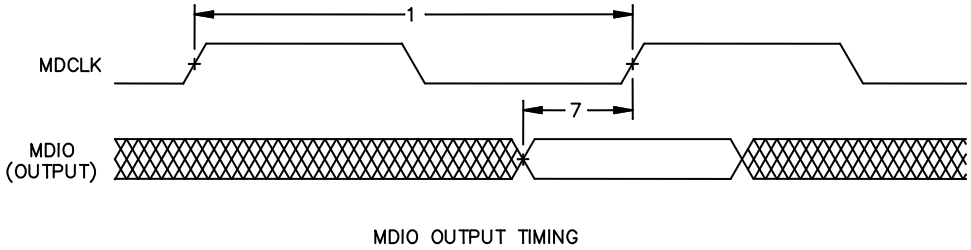


FIGURE 36. Timing waveforms.

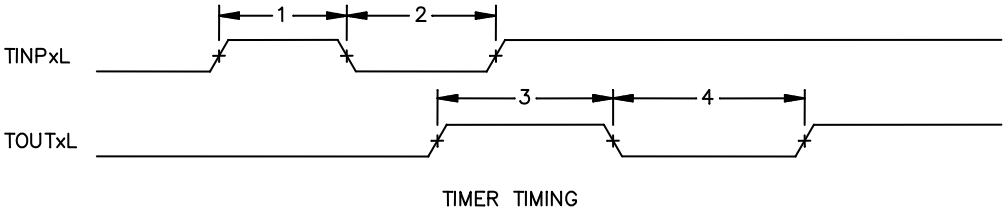


FIGURE 37. Timing waveforms.

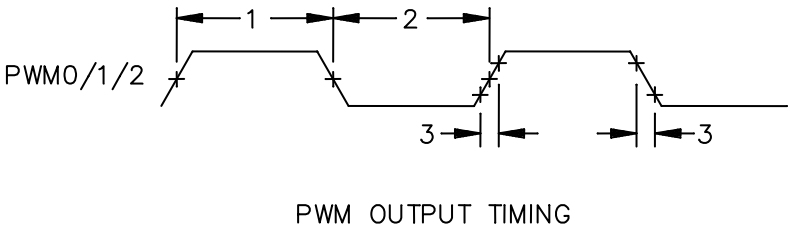
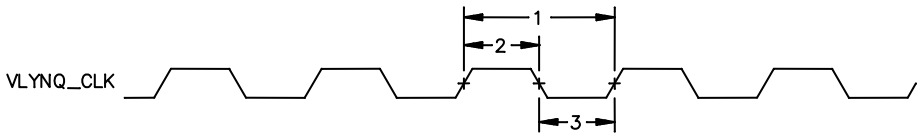
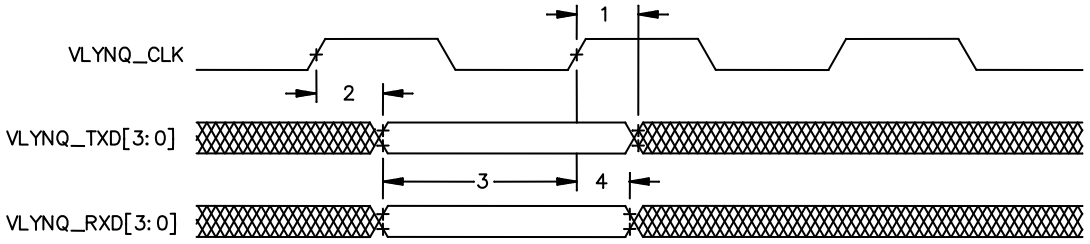


FIGURE 38. Timing waveforms.



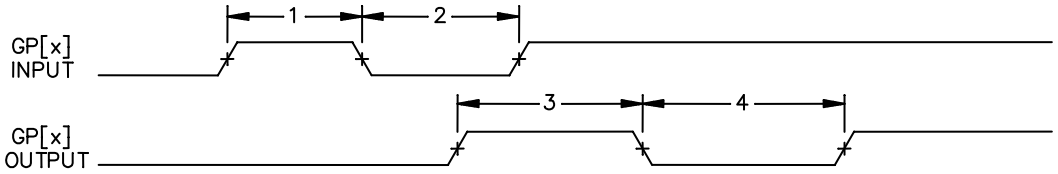
VYLYNQ_CLK TIMING FOR VLYNQ

FIGURE 39. Timing waveforms.



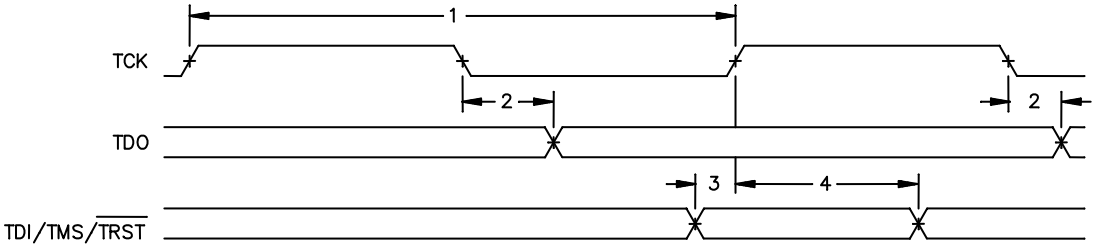
VLYNQ TRANSMIT/RECEIVE TIMING

FIGURE 40. Timing waveforms.



GPIO PORT TIMING

FIGURE 41. Timing waveforms.



JTAG TEST-PORT TIMING

FIGURE 42. Timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/09629-01XA	2/	SM320C6424GDUQ4EP
V62/09629-02XA	2/	SM320C6424GDUQ5EP
V62/09629-03XE	01295	SM320C6424GDUQ6EP
V62/09629-04XA	2/	SM320C6424GDUQ7EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Not yet available from a source of supplied.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493