REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add device types 02 and 03. Add three footnotes under paragraph 1.2.1. Add footnote under paragraph 6.3. - ro	10-01-21	C. SAFFLE
B	Update document paragraphs to current requirements. - ro	16-03-02	C. SAFFLE

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
PAGE																						
REV	B	B	B	B	B	B																
PAGE	18	19	20	21	22	23																

REV STATUS OF PAGES	**REV**	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 09-09-01	**CHECKED BY** RAJESH PITHADIA	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, LOW POWER, 8-CHANNEL, SERIAL 10 BIT ANALOG TO DIGITAL CONVERTER, MONOLITHIC SILICON
	APPROVED BY CHARLES F. SAFFLE	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/09628**
	REV **B**	**PAGE** 1 **OF** 23

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a low power 8-channel, serial, 10 bit analog to digital converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/09628	-	01	X	B
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01 1/	MAX149BMAP/PR	Low power 8-channel, serial, 10 bit analog to digital converter
02 2/	MAX149BMAP/PR2	Low power 8-channel, serial, 10 bit analog to digital converter
03 3/	MAX149BMAP/PR3	Low power 8-channel, serial, 10 bit analog to digital converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	MO-150	Shrink small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1/ Device type 01, 100% burn-in and 100% testing at room, hot, and cold temperatures.

2/ Device type 02, 100% testing at room, hot, and cold temperatures.

3/ Device type 03, 100% testing at room temperature only, guaranteed by design to the limits specified in table I for hot and cold temperatures.

1.3 Absolute maximum ratings. 4/

V_{DD} to AGND, DGND ..... -0.3 V to +6 V
AGND to DGND ..... -0.3 V to +0.3 V
CH0 – CH7, COM to AGND, DGND ..... -0.3 V to (V_{DD} + 0.3 V)
VREF, REFADJ to AGND ..... -0.3 V to (V_{DD} + 0.3 V)
Digital inputs to DGND ..... -0.3 V to +6 V
Digital outputs to DGND ..... -0.3 V to (V_{DD} + 0.3 V)
Digital output sink current ..... 25 mA
Storage temperature range (T_{STG}) ..... -60°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Junction temperature range (T_J) ..... +150°C
Electrostatic discharge (ESD):
  Human body model (HBM) ..... 800 V
Moisture sensitivity level (MSL) ..... Level 1

1.4 Recommended operating conditions. 5/

Operating free-air temperature range (T_A) ..... -55°C to +125°C

1.5 Thermal data table.

Case outline letter	X	X	Unit
PC board	Single layer	Multi-layer 6/	
Power dissipation (P_D), maximum at +70°C	640	952	mW
Power dissipation (P_D) derating above +70°C	8.0	11.9	mW/°C
Thermal resistance, junction to case (θ_{JC})	33	32	°C/W
Thermal resistance, junction to ambient (θ_{JA})	125	84	°C/W

4/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
6/ Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, contact the manufacturer.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC JESD51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth tables. The truth tables shall be as shown in figure 3.

3.5.4 Block diagram. The block diagram shall be as shown in figure 4.

3.5.5 Load circuits. The load circuits shall be as shown in figures 5 and 6.

3.5.6 Timing waveforms. The timing waveforms shall be as shown in figure 7.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC accuracy 3/							
Resolution			-55°C to +125°C	01,02, 03	10		Bits
Relative accuracy 4/	INL		-55°C to +125°C	01,02, 03		±1.0	LSB
Differential nonlinearity	DNL	No missing codes over temperature	-55°C to +125°C	01,02, 03		±1	LSB
Offset error	OE		-55°C to +125°C	01,02, 03		±2	LSB
Gain error 5/	AE		-55°C to +125°C	01,02, 03		±2	LSB
Gain temperature coefficient	ΔAE/ΔT		-55°C to +125°C	01,02, 03	±0.25 typical		ppm / °C
Channel to channel offset matching			-55°C to +125°C	01,02, 03	±0.05 typical		LSB
Dynamic specifications		6/					
Signal to noise + distortion noise	SINAD		-55°C to +125°C	01,02, 03	66 typical		dB
Total harmonic distortion	THD	Up to the fifth harmonic	-55°C to +125°C	01,02, 03	-70 typical		dB
Spuriuos-free dynamic range	SFDR		-55°C to +125°C	01,02, 03	70 typical		dB
Channel to channel crosstalk		65 kHz, 2.500 V_{P-P} 7/	-55°C to +125°C	01,02, 03	-75 typical		dB
Small signal bandwidth	SSBW	-3 dB rolloff	-55°C to +125°C	01,02, 03	2.25 typical		MHz
Full power bandwidth	FPBW		-55°C to +125°C	01,02, 03	1.0 typical		MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Conversion rate		See figure 7					
Conversion time 8/	t_{CONV}	Internal clock, $\overline{SHDN}$ = unconnected	-55°C to +125°C	01,02, 03	5.5	7.5	µs
		Internal clock, $\overline{SHDN}$ = V_{DD}			35	65	
		External clock = 2 MHz, 12 clocks/conversion			6		
Track/hold acquisition time	t_{ACQ}		-55°C to +125°C	01,02, 03		1.5	µs
Aperture delay			-55°C to +125°C	01,02, 03	30 typical		ns
Aperture jitter			-55°C to +125°C	01,02, 03	< 50 typical		ps
Internal clock frequency	f_{CLKI}	$\overline{SHDN}$ = unconnected	-55°C to +125°C	01,02, 03	1.8 typical		MHz
		$\overline{SHDN}$ = V_{DD}			0.225 typical		
External clock frequency	f_{CLKE}		-55°C to +125°C	01,02, 03	0.1	2.0	MHz
		Data transfer only			0	2.0	
Analog/com inputs							
Input voltage range, 9/ single ended and differential	V_{IN}	Unipolar, COM = 0 V	-55°C to +125°C	01,02, 03		0 to V_{REF}	V
		Bipolar, COM = $V_{REF}/2$				$\pm V_{REF}/2$	
Multiplexer leakage current	I_L	On/off leakage current, $V_{CH\_}$ = 0 V or V_{DD}	-55°C to +125°C	01,02, 03		±1	µA
Input capacitance	C_{IN}		-55°C to +125°C	01,02, 03	16 typical		pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Internal reference		(Reference buffer enabled)					
V_{REF} output voltage	V_{OUT}	10/	+25°C	01,02, 03	2.470	2.530	V
V_{REF} short circuit current	I_{OS}		-55°C to +125°C	01,02, 03		30	mA
V_{REF} temperature coefficient			-55°C to +125°C	01,02, 03	±30 typical		ppm/ °C
Load regulation 11/	LD	0 to 0.2 mA output load	-55°C to +125°C	01,02, 03	0.35 typical		mV
Capacitive bypass at V_{REF}	C_{BPV}	Internal compensation mode	-55°C to +125°C	01,02,	0		µF
		External compensation mode		03	4.7		
Capacitive bypass at REFADJ	C_{BPR}		-55°C to +125°C	01,02, 03	0.01		µF
REFADJ adjustment range			-55°C to +125°C	01,02, 03	±1.5 typical		%
External reference at V_{REF}		(Buffer disabled)					
V_{REF} input voltage range 12/	V_{IN}		-55°C to +125°C	01,02, 03	1.0	V_{DD} + 50 mV	V
V_{REF} input current	I_{IN}	V_{REF} = 2.500 V	-55°C to +125°C	01,02, 03		150	µA
V_{REF} input resistance	R_{IN}		-55°C to +125°C	01,02, 03	18		kΩ
Shutdown V_{REF} input current	I_{NSD}		-55°C to +125°C	01,02, 03		10	µA
REFADJ buffer disable threshold	V_{BDT}		-55°C to +125°C	01,02, 03	V_{DD} – 0.5		V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
External reference at REFADJ							
Capacitive bypass at V_{REF}	C_{BPV}	Internal compensation mode	-55°C to +125°C	01,02, 03	0		µF
		External compensation mode			4.7		
Reference buffer gain	ARB		-55°C to +125°C	01,02, 03	2.06 typical		V/V
REFADJ input current	I_{IN}		-55°C to +125°C	01,02, 03		±50	µA
Digital inputs		(DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$)					
DIN, SCLK, $\overline{CS}$, input high voltage	V_{IH}	$V_{DD} \leq 3.6$ V	-55°C to +125°C	01,02, 03	2.0		V
		$V_{DD} > 3.6$ V			3.0		
DIN, SCLK, $\overline{CS}$, input low voltage	V_{IL}		-55°C to +125°C	01,02, 03		0.8	V
DIN, SCLK, $\overline{CS}$, input hysteresis	V_{HYST}		-55°C to +125°C	01,02, 03	0.2 typical		V
DIN, SCLK, $\overline{CS}$, input leakage	V_{IN}	V_{IN} = 0 or V_{DD}	-55°C to +125°C	01,02, 03		±1	µA
DIN, SCLK, $\overline{CS}$, input capacitance	C_{IN}	13/	-55°C to +125°C	01,02, 03		15	pF
$\overline{SHDN}$ input high voltage	V_{SH}		-55°C to +125°C	01,02, 03	V_{DD} – 0.4		V
$\overline{SHDN}$ input mid voltage	V_{SM}		-55°C to +125°C	01,02, 03	1.1	V_{DD} – 1.1	V
$\overline{SHDN}$ input low voltage	V_{SL}		-55°C to +125°C	01,02, 03		0.4	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Digital inputs – continued.		(DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$)					
$\overline{SHDN}$ input current	I_S	$\overline{SHDN}$ = 0 or V_{DD}	-55°C to +125°C	01,02, 03		±4.0	µA
$\overline{SHDN}$ voltage, unconnected	V_{FLT}	$\overline{SHDN}$ = unconnected	-55°C to +125°C	01,02, 03	V_{DD}/2 typical		V
$\overline{SHDN}$ maximum allowed leakage, mid point	I_{LMP}	$\overline{SHDN}$ = unconnected	-55°C to +125°C	01,02, 03		±100	nA
Digital outputs		(DOUT, SSTRB)					
Output voltage low	V_{OL}	I_{SINK} = 5 mA	-55°C to +125°C	01,02,		0.4	V
		I_{SINK} = 16 mA		03		0.8	
Output voltage high	V_{OH}	I_{SOURCE} = 0.5 mA	-55°C to +125°C	01,02, 03	V_{DD} – 0.5		V
Three-state leakage current	I_L	$\overline{CS}$ = V_{DD}	-55°C to +125°C	01,02, 03		±10	µA
Three-state output capacitance	C_{OUT}	$\overline{CS}$ = V_{DD} 13/	-55°C to +125°C	01,02, 03		15	pF
Power requirements							
Positive supply voltage	V_{DD}		-55°C to +125°C	01,02, 03	2.70	5.25	V
Positive supply current	I_{DD}	V_{DD} = 5.25 V, operating mode, full scale input	-55°C to +125°C	01,02, 03		3.0	mA
		V_{DD} = 3.6 V, operating mode, full scale input				2.0	
		V_{DD} = 5.25 V, full power down				15	µA
		V_{DD} = 3.6 V, full power down				10	
		Fast power down				70	
Power supply rejection 14/	PSR	Full scale input, external reference = 2.500 V, V_{DD} = 2.7 V to 5.25 V	-55°C to +125°C	01,02, 03	±0.3 typical		mV

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing characteristics		See figure 7					
Acquisition time	t_{ACQ}		-55°C to +125°C	01,02, 03	1.5		µs
DIN to SCLK setup	t_{DS}		-55°C to +125°C	01,02, 03	100		ns
DIN to SCLK hold	t_{DH}		-55°C to +125°C	01,02, 03	0		ns
SCLK fall to output data valid	t_{DO}	See figure 5	-55°C to +125°C	01,02, 03	20	240	ns
$\overline{CS}$ fall to output enable	t_{DV}	See figure 5	-55°C to +125°C	01,02, 03		240	ns
$\overline{CS}$ rise to output disable	t_{TR}	See figure 6	-55°C to +125°C	01,02, 03		240	ns
$\overline{CS}$ to SCLK rise setup	t_{CSS}		-55°C to +125°C	01,02, 03	100		ns
$\overline{CS}$ to SCLK rise hold	t_{CSH}		-55°C to +125°C	01,02, 03	0		ns
SCLK pulse width high	t_{CH}		-55°C to +125°C	01,02, 03	200		ns
SCLK pulse width low	t_{CL}		-55°C to +125°C	01,02, 03	200		ns
SCLK fall to SSTRB	t_{SSTRB}	See figure 5	-55°C to +125°C	01,02, 03		240	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing characteristics – continued.		See figure 7					
$\overline{CS}$ fall to SSTRB output enable	t_{SDV}	External clock mode only, see figure 5	-55°C to +125°C	01,02, 03		240	ns
$\overline{CS}$ rise to SSTRB output disable	t_{STR}	External clock mode only, see figure 6	-55°C to +125°C	01,02, 03		240	ns
SSTRB rise to SCLK rise	t_{SCK}	Internal clock mode only 13/	-55°C to +125°C	01,02, 03	0		ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{DD} = +2.7 V to +5.25 V, COM = 0 V, f_{SCLK} = 2.0 MHz, external clock (50 % duty cycle), 15 clocks/conversion cycle (133 ksps), 4.7 μF capacitor at V_{REF} pin, V_{REF} = 2.500 V applied to V_{REF} pin.

3/ Tested at V_{DD} = 2.7 V, COM = 0 V, unipolar single ended input mode.

4/ Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full scale range has been calibrated.

5/ Internal reference, offset nulled.

6/ 10 kHz sine wave input, 0 V_{P-P} to 2.500 V_{P-P}, 133 ksps, 2.0 MHz external clock, bipolar input mode.

7/ Ground “on” channel, sine wave applied to all “off” channels.

8/ Conversion time defined as the number of clock cycles multiplied by the clock period, clock has 50 % duty cycle.

9/ The common mode range for the analog inputs is from AGND to V_{DD}.

10/ Sample tested to 0.1% acceptable quality level (AQL).

11/ External load should not change during conversion for specified accuracy.

12/ ADC performance is limited by the converter’s noise floor, typically 300 μV_{P-P}.

13/ Guaranteed by design. Not subject to production testing.

14/ Measured as | V_{FS}(2.7 V) – V_{FS}(5.25 V) |.

Case X

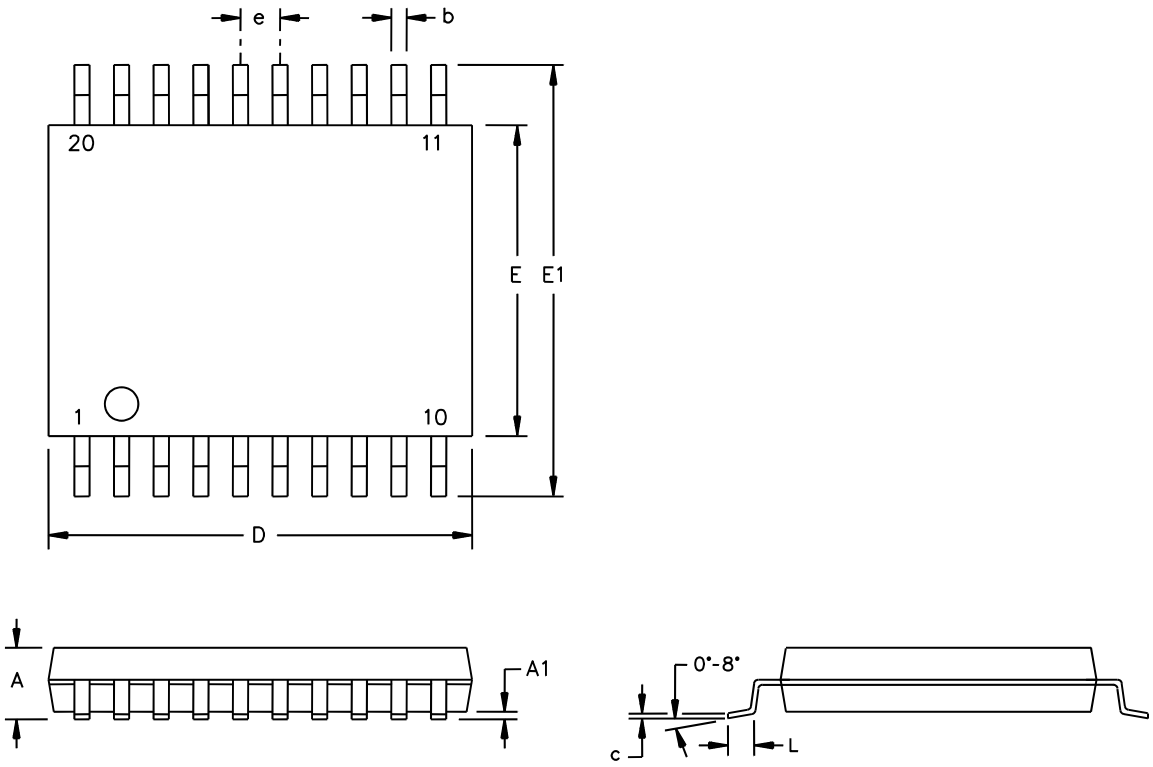


FIGURE 1. Case outline.

Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
b	0.010	0.015	0.25	0.38
c	0.004	0.008	0.09	0.20
D	0.278	0.289	7.07	7.33
E	0.205	0.212	5.20	5.38
E1	0.301	0.311	7.65	7.90
e	0.0256 BSC		0.65 BSC	
L	0.025	0.037	0.63	0.95
n	20		20	

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Dimensions D and E do not include mold flash. Mold flash or protrusion not to exceed 0.15 mm (0.006 inch).
3. Leads to be coplanar within 0.10 mm (0.003 inch).
4. Falls within reference to JEDEC MO-150.

FIGURE 1. Case outline - Continued.

Device types	01, 02, 03
Case outline	X
Terminal number	Terminal symbol
1	CH0
2	CH1
3	CH2
4	CH3
5	CH4
6	CH5
7	CH6
8	CH7
9	COM
10	$\overline{SHDN}$
11	VREF
12	REFADJ
13	AGND
14	DGND
15	DOUT
16	SSTRB
17	DIN
18	$\overline{CS}$
19	SCLK
20	V_{DD}

FIGURE 2. Terminal connections.

Terminal number	Terminal symbol	Function
1 – 8	CH0 – CH7	Sampling analog inputs.
9	COM	Ground reference for analog inputs. COM sets zero code voltage in single-ended mode. Must be stable to ±0.5 LSB.
10	$\overline{\text{SHDN}}$	Three-level shutdown input. Pulling $\overline{\text{SHDN}}$ low shuts the device down; otherwise, they are fully operational. Pulling $\overline{\text{SHDN}}$ high puts the reference-buffer amplifier in internal compensation mode. Leaving $\overline{\text{SHDN}}$ unconnected puts the reference-buffer amplifier in external compensation mode.
11	VREF	Reference-Buffer output/ADC reference input. Reference voltage for analog to digital conversion. In internal reference mode, the reference buffer provides a 2.500 V nominal output, externally adjustable at REFADJ. In external reference mode, disable the internal buffer by pulling REFADJ to V_{DD}.
12	REFADJ	Input to the reference-buffer amplifier. To disable the reference-buffer amplifier, tie REFADJ to V_{DD}.
13	AGND	Analog ground.
14	DGND	Digital ground.
15	DOUT	Serial data output. Data is clocked out at SCLK's falling edge. High impedance when $\overline{\text{CS}}$ is high.
16	SSTRB	Serial strobe output. In internal clock mode, SSTRB goes low when the device begins the A/D conversion, and goes high when the conversion is finished. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. High impedance when $\overline{\text{CS}}$ is high (external clock mode).
17	DIN	Serial data input. Data is clocked in at SCLK's rising edge.
18	$\overline{\text{CS}}$	Active low chip select. Data will not be clocked into DIN unless $\overline{\text{CS}}$ is low. When $\overline{\text{CS}}$ is high, DOUT is high impedance.
19	SCLK	Serial clock input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed. (Duty cycle must be 40% to 60%.)
20	V_{DD}	Positive supply voltage.

FIGURE 2. Terminal connections – continued.

Control byte format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
START	SEL2	SEL1	SEL0	UNI/$\overline{\text{BIP}}$	SGL/$\overline{\text{DIF}}$	PD1	PD0

BIT	NAME	DESCRIPTION		
7 (MSB)	START	The first logic "1" bit after $\overline{\text{CS}}$ goes low defines the beginning of the control byte.		
6	SEL2	These three bits select which of the eight channels are used for the conversion.		
5	SEL1			
4	SEL0			
3	UNI/$\overline{\text{BIP}}$	1 = unipolar, 0 = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, an analog input signal from 0 to VREF can be converted; in bipolar mode, the signal can range from –VREF/2 to +VREF/2.		
2	SGL/$\overline{\text{DIF}}$	1 = single ended, 0 = differential. Selects single ended or differential conversion. In single ended mode, input signal voltages are referred to COM. In differential mode, the voltage difference between two channels is measured.		
1	PD1	Selects clock and power down modes.		
0 (LSB)	PD0	PD1	PD0	Mode
		0	0	Full power down
		0	1	Fast power down
		1	0	Internal clock mode
		1	1	External clock mode

FIGURE 3. Truth tables.

Channel selection in single ended mode (SGL/$\overline{\text{DIF}}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	+								-
1	0	0		+							-
0	0	1			+						-
1	0	1				+					-
0	1	0					+				-
1	1	0						+			-
0	1	1							+		-
1	1	1								+	-

Channel selection in differential mode (SGL/$\overline{\text{DIF}}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+	-						
0	0	1			+	-				
0	1	0					+	-		
0	1	1							+	-
1	0	0	-	+						
1	0	1			-	+				
1	1	0					-	+		
1	1	1							-	+

FIGURE 3. Truth tables – continued.

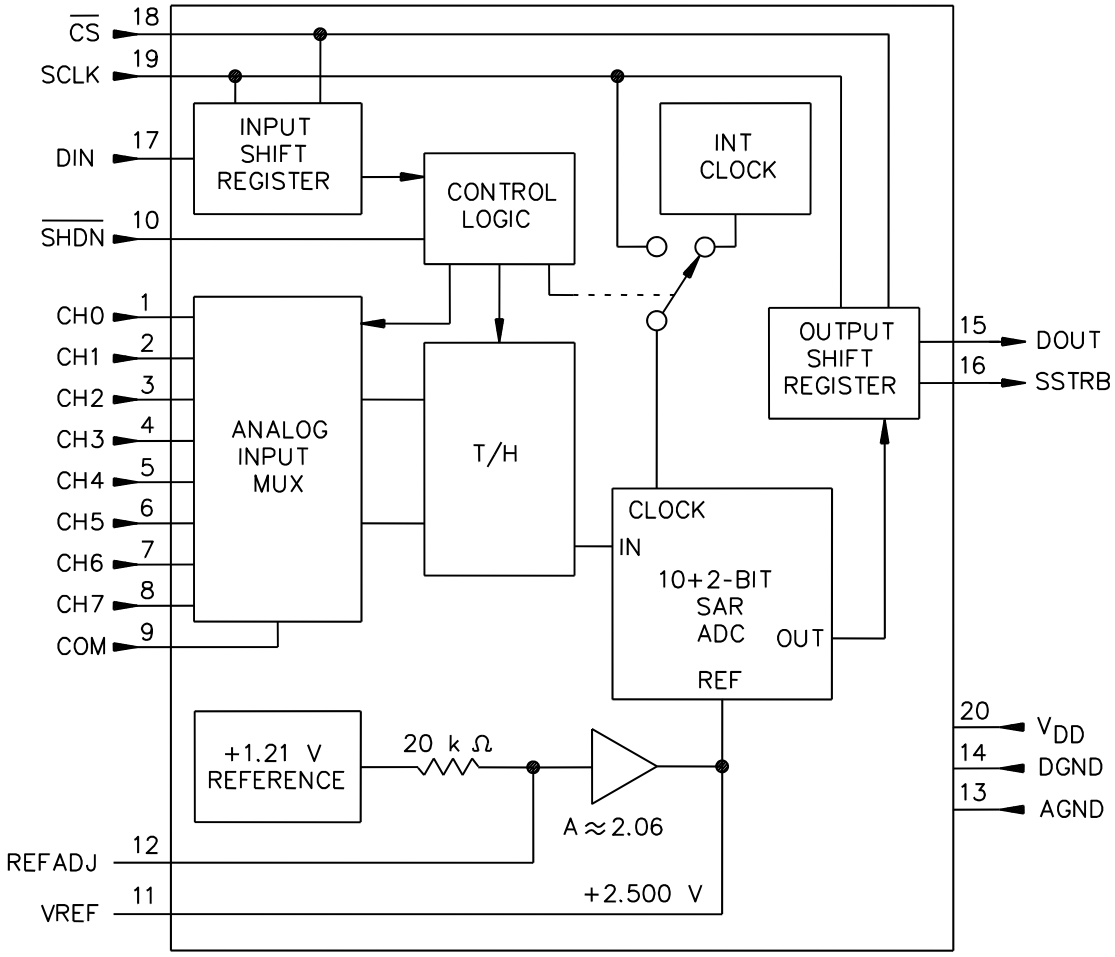


FIGURE 4. Block diagram.

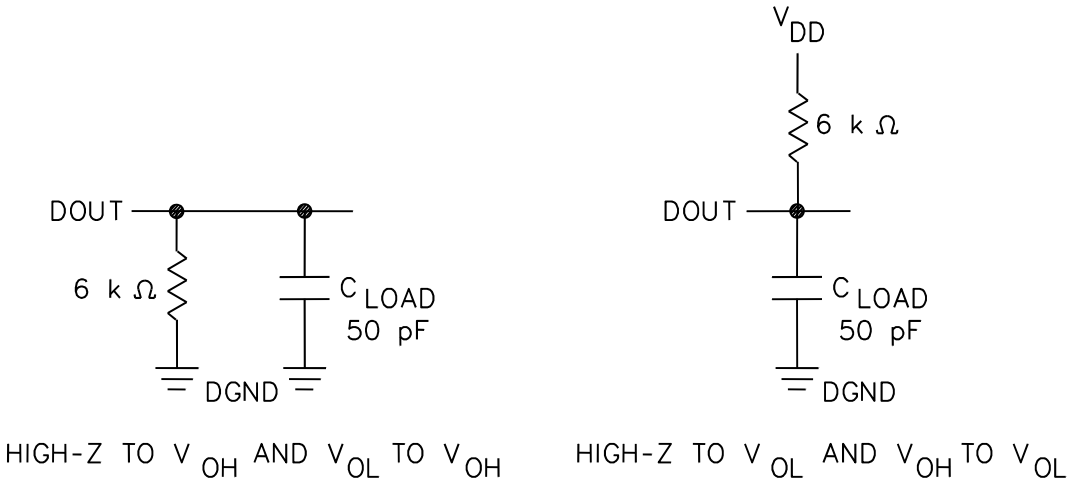


FIGURE 5. Load circuits for enable time.

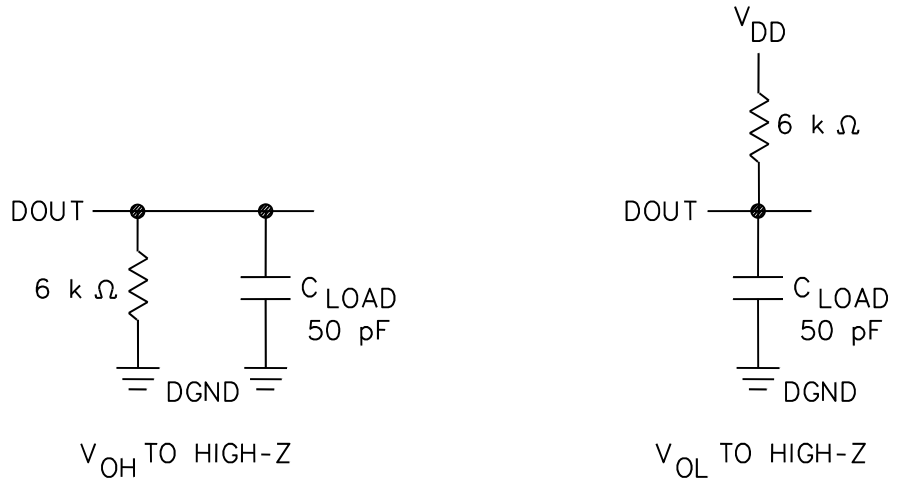
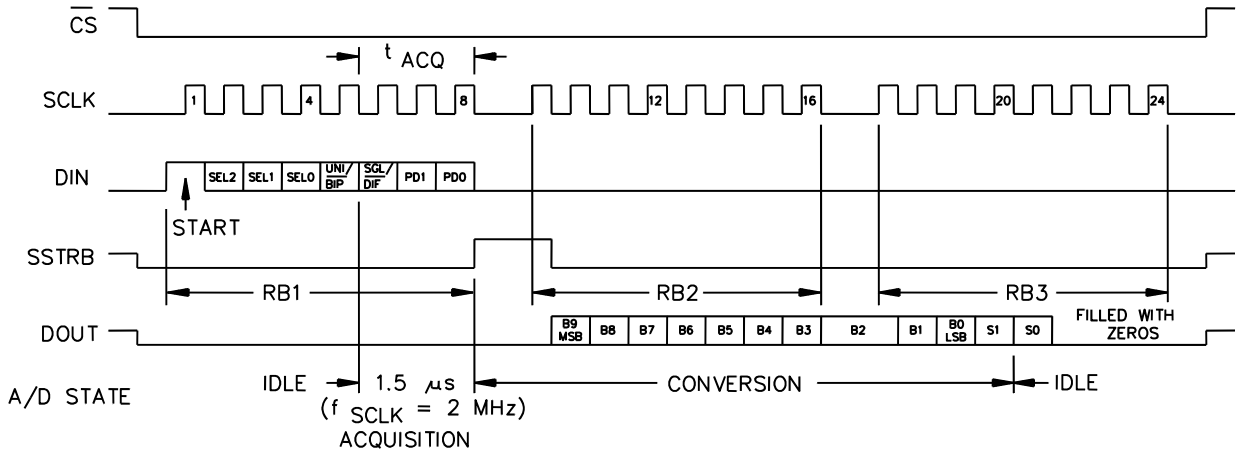
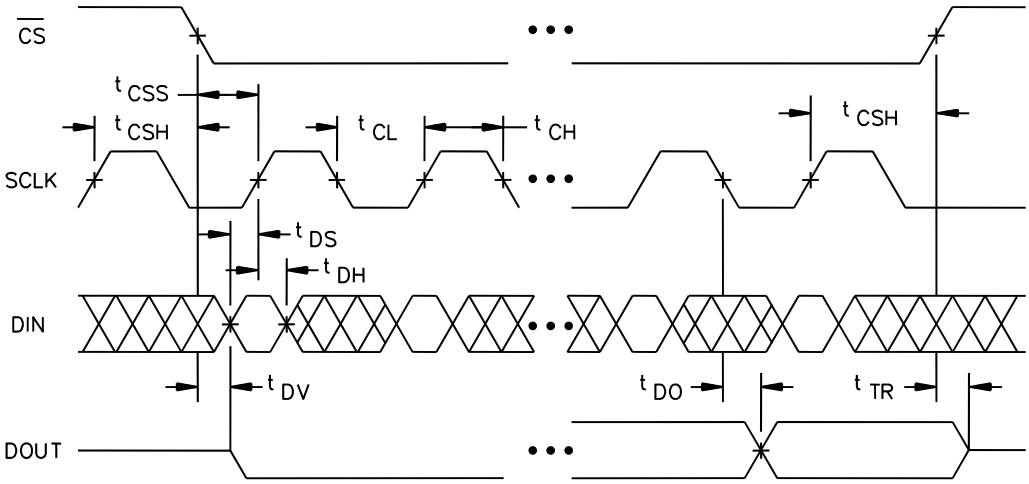


FIGURE 6. Load circuits for disable time.

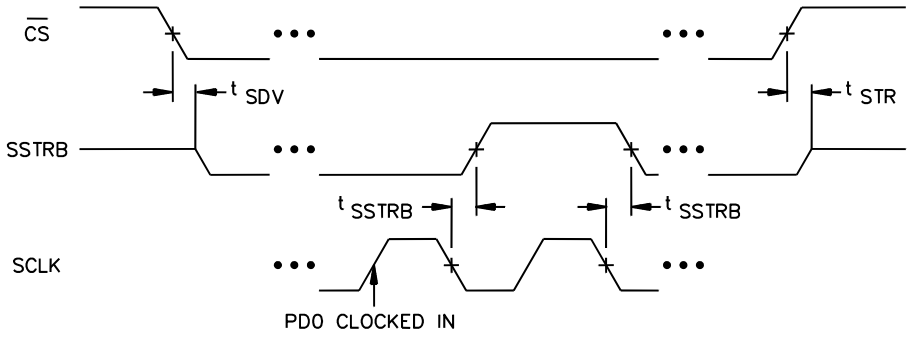


24 CLOCK EXTERNAL CLOCK MODE CONVERSION TIMING

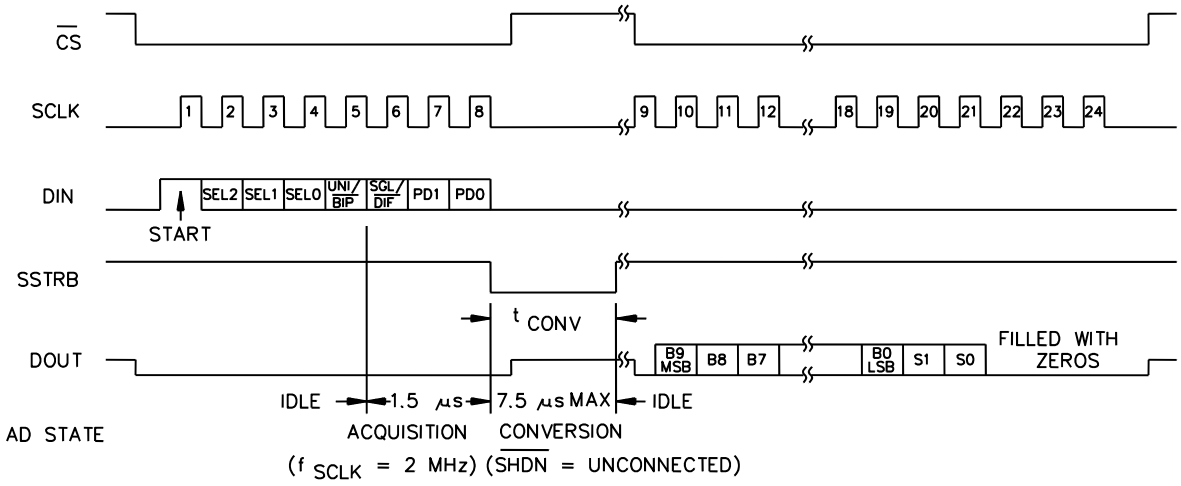


DETAILED SERIAL INTERFACE TIMING

FIGURE 7. Timing waveforms.

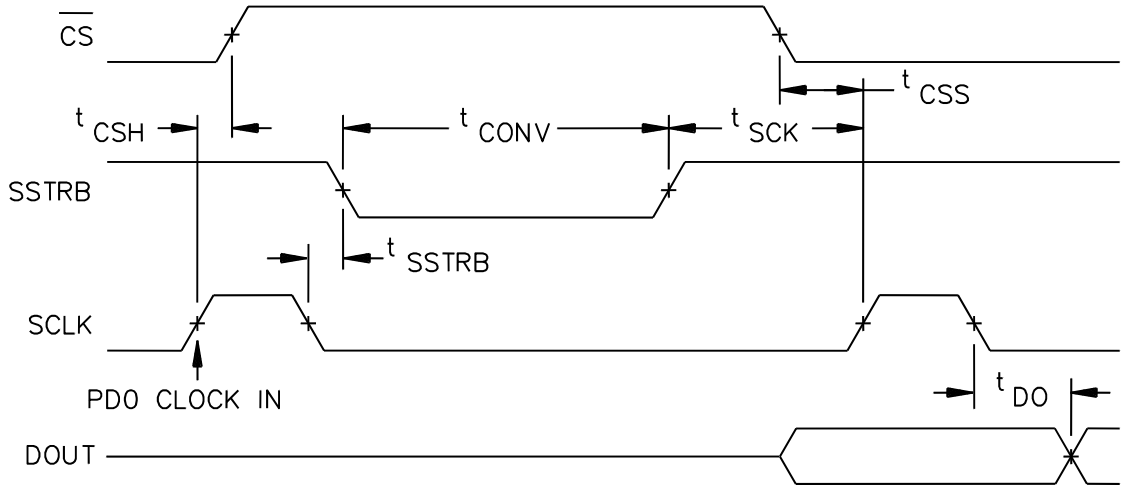


EXTERNAL CLOCK MODE SSTRB DETAILED TIMING



INTERNAL CLOCK MODE TIMING

FIGURE 7. Timing waveforms – continued.



INTERNAL CLOCK MODE SSTRB DETAILED TIMING

NOTE: For best noise performance keep SCLK low during conversion.

FIGURE 7. Timing waveforms – continued.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/ 2/	Device manufacturer CAGE code	Vendor part number 3/
V62/09628-01XB	1ES66	MAX149BMAP/PR
V62/09628-02XB	1ES66	MAX149BMAP/PR2
V62/09628-03XB	1ES66	MAX149BMAP/PR3

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For the latest package outline information and land patterns, go to website www.maxim-ic.com/packages.

3/ See paragraph 1.2.1 for information on /PR, /PR2, and /PR3 differences.

CAGE code	Source of supply
1ES66	Maxim Integrated 160 Rio Robles San Jose, CA 95134