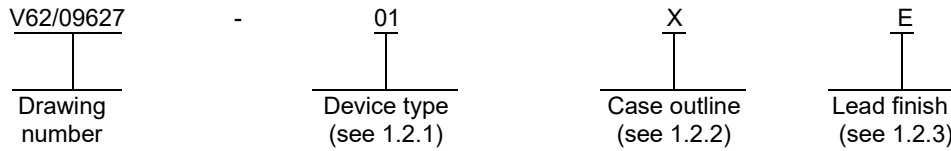


1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance digital receiver microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	TFP401A-EP	Digital receiver

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	100	MS-026	Plastic Quad Flatpack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage, (DV _{DD} , AV _{DD} , OV _{DD} , PV _{DD})	-0.3 V to 4.0 V	
Input voltage, logic/analog signals	-0.3 V to 4.0 V	
Storage temperature range (T _{STG}).....	-65°C to 150°C	2/
Operating temperature range	-55°C to 125°C	
Case temperature for 10 s	260°C	
Lead temperature (1.6 mm (1/16 in) from the case for 10 s)	260°C	
Maximum package power dissipation:		
Soldered	4.3 W	3/
Not soldered	2.7 W	4/
ESD protection, all pins	25 kV, Human Body model	
JEDEC latch up (EIA/JESD78)	100 mA	

1.4 Recommended operating conditions. 5/

Supply voltage V _{DD} , (DV _{DD} , AV _{DD} , PV _{DD} , OV _{DD})	3.0 V to 3.6 V	
Pixel time, (t _{pix})	6.06 ns to 40 ns	6/
Single ended analog input termination resistance,	45 Ω to 75 Ω	
Operating free air temperature, (T _A)	-55°C to 125°C	

-
- 1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
 - 2/ Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life.
 - 3/ Specified with the bond pad on the backside of the package soldered to a 2 oz. Cu plate PCB thermal plane. Specified at maximum allowed operating temperature, 70°C.
 - 4/ The bond pad on the backside of the package is not soldered to a thermal plane. Specified at maximum allowed operating temperature, 70°C.
 - 5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
 - 6/ t_{pix} is the pixel time defined as the period of the RxC clock input. The period of the output clock, ODCK is equal to t_{pix} when in 1-pixel/clock mode and 2t_{pix} when in 2-pixel/clock mode.

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2. APPLICABLE DOCUMENTS

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Timing diagram. The timing diagram shall be as shown in figure 4-10.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Limits		Unit
			Min	Max	
DC Specifications					
High level digital input voltage	V _{IH}		2	DV _{DD}	V
Low level digital input voltage	V _{IL}		0	0.8	
High level output drive current	I _{OH}	ST = High V _{OH} = 2.4 V	5	16.3	mA
		ST = Low V _{OH} = 2.4 V	3	10.3	
Low level output drive current	I _{OL}	ST = High V _{OL} = 0.8 V	8	19	
		ST = Low V _{OL} = 0.8 V	4	11	
Hi-Z output leakage current	IOZ	\overline{PD} = low or \overline{PDO} = Low	-1	1	μA
Analog input differential voltage 3/	V _{ID}		75	1200	mV
Analog input common mode voltage 3/	V _{IC}		AV _{DD} -300	AV _{DD} -37	mV
Open circuit analog input voltage	V _{I(OC)}		AV _{DD} -10	AV _{DD} +10	mV
Normal 2-pix/clock power supply current 4/	I _{DD(2PIX)}	ODCK = 82.5 MHz 2-pix/clock		370	mA
Power down current 5/	I _{PD}	\overline{PD} = low		10	mA
Output drive power down current 5/	I _{PDO}	\overline{PDO} = Low	35	TYP	mA
AC Specifications					
Differential input sensitivity 6/	V _{ID} 7/		150	1560	mVp-p
Analog input intra pair (+ to -) differential skew 7/	t _{ps}			0.4	t _{bit} 8/
Analog input inter pair or channel to channel skew 7/	t _{ccs}			1	t _{pix} 9/
Worse case differential input clock jitter tolerance 10/ 7/ 11/	t _{jitt}		50		ps
Fall time of data and control signals 12/ 13/ 11/	t _{f1}	ST = Low, CL = 5 pF		2.4	ns
		ST = High, CL = 10 pF		1.9	
Rise time of data and control signals 12/ 13/ 11/	t _{r1}	ST = Low, CL = 5 pF		2.4	
		ST = High, CL = 10 pF		1.9	
Rise time of ODCK clock 11/ 12/	t _{r2}	ST = Low, CL = 5 pF		2.4	
		ST = High, CL = 10 pF		1.9	
Fall time of ODCK clock 11/ 12/	t _{f2}	ST = Low, CL = 5 pF		2.4	
		ST = High, CL = 10 pF		1.9	
Setup time, data and control signal to falling edge of ODCK 11/	t _{su1}	1 pixel/clock, PIXS = low, OCK_INV = low		1.8	
		2 pixel/clock, PIXS = high, STAG = high, OCK_INV = low		3.8	
		2 pixel and \overline{STAG} , PIXS = high, \overline{STAG} = low, OCK_INV = low		0.6	

See footnotes at end of table.

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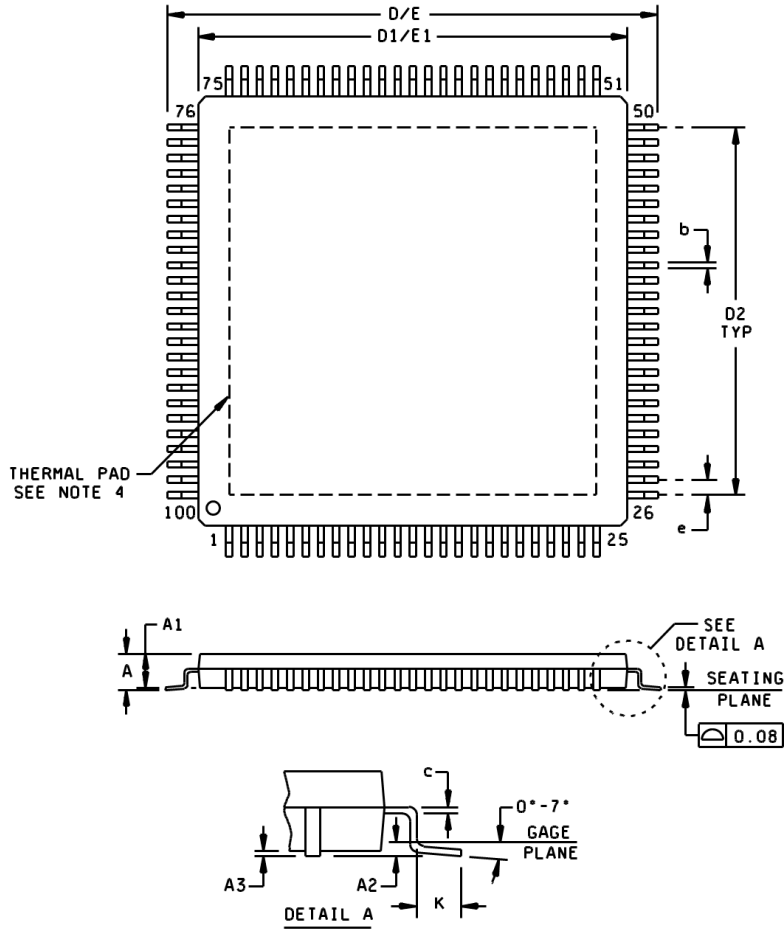
TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>2/</u>	Limits		Unit
			Min	Max	
AC Specifications					
Hold time, data and control signal to falling edge of ODCK <u>11/</u>	t_{h1}	1 pixel/clock, PIXS = low, OCK_INV = low	0.6		ns
		2 pixel and $\overline{\text{STAG}}$, PIXS = high, $\overline{\text{STAG}}$ = low, OCK_INV = low	2.5		
		2 pixel/clock, PIXS = high, $\overline{\text{STAG}}$ = high, OCK_INV = low	2.9		
Setup time, data and control signal to rising edge of ODCK <u>11/</u>	t_{su2}	1 pixel/clock, PIXS = low, OCK_INV = high	2.1		
		2 pixel/clock, PIXS = high, $\overline{\text{STAG}}$ = high, OCK_INV = high	4		
		2 pixel and $\overline{\text{STAG}}$, PIXS = high, $\overline{\text{STAG}}$ = low, OCK_INV = high	1.5		
Hold time, data and control signal to rising edge of ODCK <u>11/</u>	t_{h2}	1 pixel/clock, PIXS = low, OCK_INV = high	0.3		
		2 pixel and $\overline{\text{STAG}}$, PIXS = high, $\overline{\text{STAG}}$ = low, OCK_INV = high	2.4		
		2 pixel/clock, PIXS = high, $\overline{\text{STAG}}$ = high, OCK_INV = high	2.1		
ODCK frequency	f_{ODCK}	PIX = low (1-PIX/CLK)	25	165	MHz
		PIX = High (2-PIX/CLK)	12.5	82.5	
ODCK duty-cycle			45%	75%	
Propagation delay time from PD low to Hi-Z outputs <u>11/</u>	$t_{pd(\text{PDL})}$			9	ns

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Over operating free air temperature range, (unless otherwise noted).
- 3/ Specified as dc characteristic with no overshoot or undershoot.
- 4/ Alternating 2-pixel black/2-pixel white patter. ST = high, $\overline{\text{STAG}}$ = high, QE[23:0] and QO[23:0] CL = 10 pF.
- 5/ Analog inputs are open circuit (transmitter is disconnected from (TFP401A)).
- 6/ Specified as ac parameter to include sensitivity to overshoot, undershoot and reflection.
- 7/ By characterization.
- 8/ t_{bit} is 1/10 the pixel time, t_{pix} .
- 9/ t_{pix} is the pixel time defined as the period of the RxC input clock. The period of ODCK is equal to t_{pix} in 1-pixel/clock mode or $2t_{pix}$ when in 2-pixel/clock mode.
- 10/ Measured differentially at 50% crossing using ODCK output clock as trigger.
- 11/ Not production test.
- 12/ Rise and fall time measured as time between 20% and 80% of signal amplitude.
- 13/ Data and control signals are: QE[23:0], QO[23:0], DE, HSYNC, VSYNC and CTL[3:1].

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Case X



Dimension

Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	D/E	15.80	16.20
A1	0.95	1.05	D1/E1	13.80	14.20
A2	0.25	Typ	D2/E2	12.00	Typ
A3	0.05	0.15	e	0.50	NOM
b	0.17	0.27	L1	0.45	0.75
c	0.13	NOM			

NOTES:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion.
4. This package is designed to be soldered to a thermal pad on the board. Refer to the manufacturer data for information regarding recommended board layout.
5. Falls within JEDEC MS-026.

FIGURE 1. Case outline.

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Case X

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DFO	26	QE14	51	QO2	76	OGND
2	$\overline{\text{PD}}$	27	QE15	52	QO3	77	QO23
3	ST	28	OGND	53	QO4	78	OVDD
4	PIXS	29	OVDD	54	QO5	79	AGND
5	GND	30	QE16	55	QO6	80	Rx2+
6	DVDD	31	QE17	56	QO7	81	Rx2-
7	$\overline{\text{STAG}}$	32	QE18	57	OVDD	82	AVDD
8	SCDT	33	QE19	58	OGND	83	AGND
9	$\overline{\text{PDO}}$	34	QE20	59	QO8	84	AVDD
10	QE0	35	QE21	60	QO9	85	Rx1+
11	QE1	36	QE22	61	QO10	86	Rx1-
12	QE2	37	QE23	62	QO11	87	AGND
13	QE3	38	DVDD	63	QO12	88	AVDD
14	QE4	39	GND	64	QO13	89	AGND
15	QE5	40	CTL1	65	QO14	90	Rx0+
16	QE6	41	CTL2	66	QO15	91	Rx0-
17	QE7	42	CTL3	67	DVDD	92	AGND
18	OVDD	43	OVDD	68	GND	93	RxC+
19	OGND	44	ODCK	69	QO16	94	RxC-
20	QE8	45	OGND	70	QO17	95	AVDD
21	QE9	46	DE	71	QO18	96	EXT RES
22	QE10	47	VSYNC	72	QO19	97	PVDD
23	QE11	48	HSYNC	73	QO20	98	PGND
24	QE12	49	QO0	74	QO21	99	RSVD
25	QE13	50	QO1	75	QO22	100	OCK_INV

FIGURE 2. Terminal connections.

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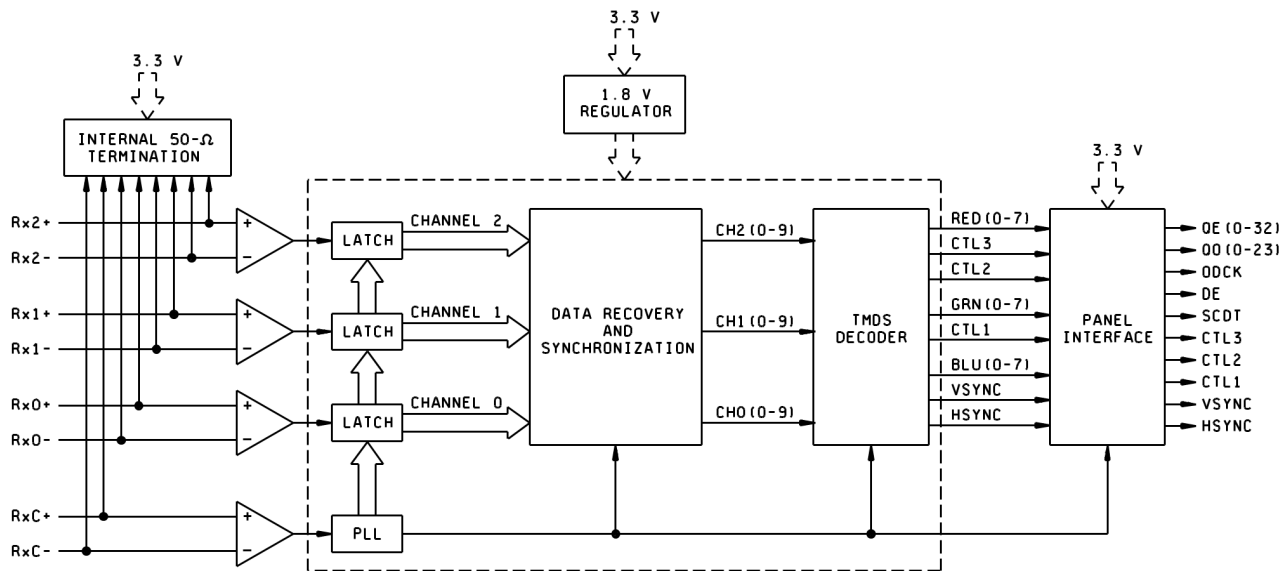
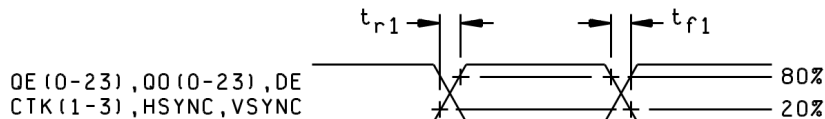
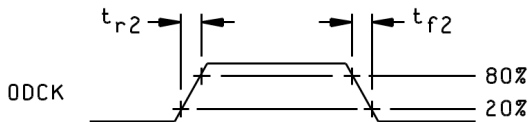


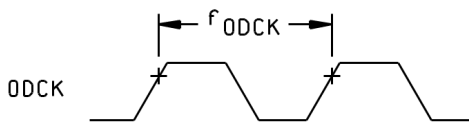
FIGURE 3. Functional block diagram.



RISE AND FALL TIME OF DATA AND CONTROL SIGNALS



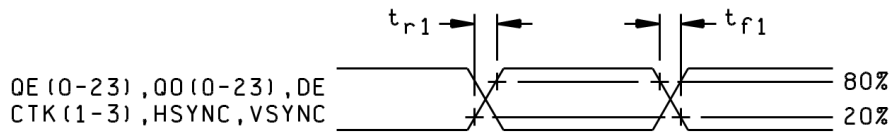
RISE AND FALL TIME OF OOCK



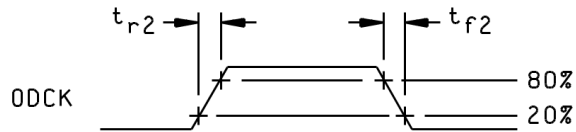
OOCK FREQUENCY

FIGURE 4. Timing diagram.

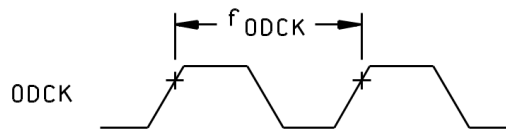
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RISE AND FALL TIME OF DATA
AND CONTROL SIGNALS

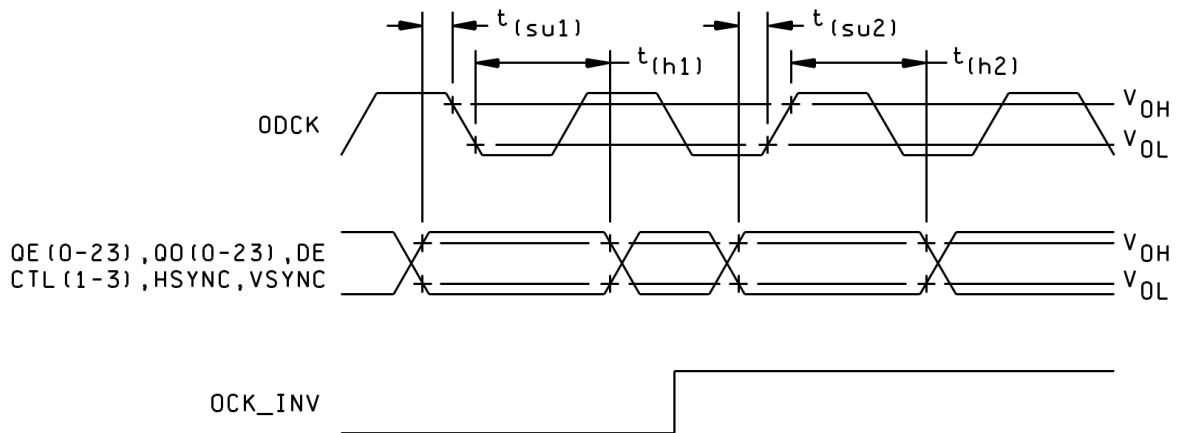


RISE AND FALL TIME OF ODCK



ODCK FREQUENCY

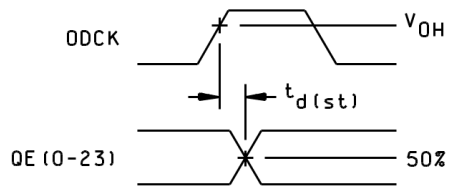
FIGURE 5. Timing diagram.



DATA SETUP AND HOLD TIME TO RISING
AND FALLING EDGE OF ODCK

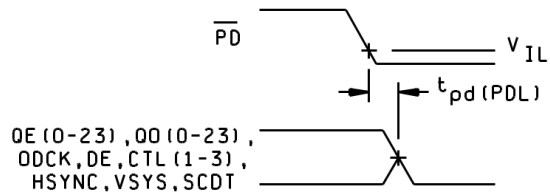
FIGURE 6. Timing diagram.

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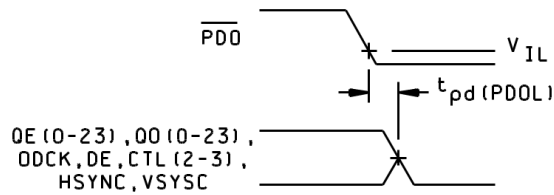


ODCK HIGH TO OE[23:0] STAGGERED DATA OUTPUT

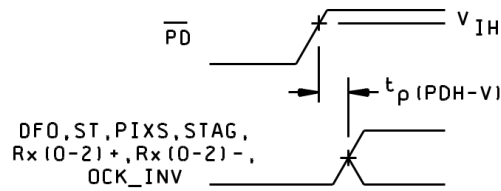
FIGURE 7. Timing diagram.



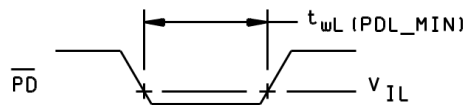
DELAY FROM PD LOW TO HI-Z OUTPUTS



DELAY FROM PDO LOW TO HI-Z OUTPUTS



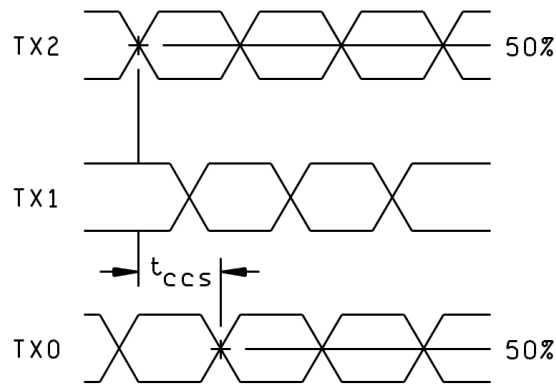
DELAY FROM PD LOW TO HIGH BEFORE INPUTS ARE ACTIVE



MINIMUM TIME PD LOW

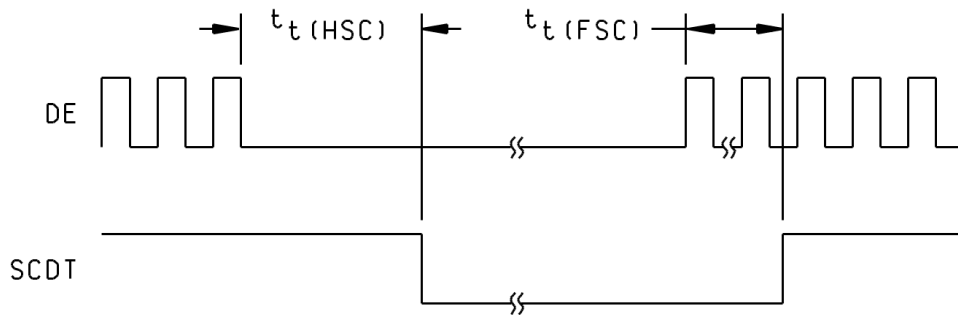
FIGURE 8. Timing diagram.

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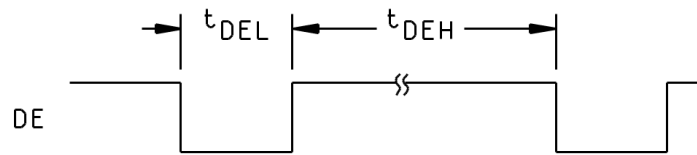


ANALOG INPUT CHANNEL-TO-CHANNEL SKEW

FIGURE 9 Timing diagram.



TIME BETWEEN DE TRANSITIONS TO SCDT LOW AND SCDT HIGH



MINIMUM DE LOW AND MAXIMUM DE HIGH

FIGURE 10 Timing diagram.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number
V62/09627-01XE	01295	TFP401AMPZPEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

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