REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add device type 02 and case outline Y. - ro	10-01-07	C. SAFFLE
B	Make changes to the Temperature sensor reading, coefficient parameter as specified under Table I. Make correction to note 1 for case Y as specified under figure 1. Update document paragraphs to current requirements. - ro	16-07-07	C. SAFFLE
C	Update document paragraphs to current requirements. - ro	22-01-13	J. ESCHMEYER

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV	C	C	C	C	C																
PAGE	18	19	20	21	22																

REV STATUS OF PAGES	**REV**	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990** https://www.dla.mil/landandmaritime
Original date of drawing YY-MM-DD 09-05-12	**CHECKED BY** RAJESH PITHADIA	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, 16 CHANNEL, 24 BIT ANALOG TO DIGITAL CONVERTER, MONOLITHIC SILICON
	APPROVED BY JOSEPH D. RODENBECK	
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** V62/09626
	REV C	**PAGE** 1 **OF** 22

AMSC N/A

5962-V107-21

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance16 channel, 24 bit analog to digital converter (ADC) microcircuit, with an operating temperature range of -55°C to +125°C for device type 01 and -40°C to +105°C for device type 02.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/09626	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Temperature range	Circuit function
01	ADS1258M-EP	-55°C to +125°C	16 channel, 24 bit analog to digital converter
02	ADS1258IP-EP	-40°C to +105°C	16 channel, 24 bit analog to digital converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	48	See figure 1	Plastic square leadless chip carrier with thermal pad
Y	48	MS-026	Plastic quad flat pack with thermal pad

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Positive analog power supply (AV_{DD}) to negative analog power supply (AV_{SS})	-0.3 V to 5.5 V
AV_{SS} to digital ground (DGND)	-2.8 V to 0.3 V
Digital power supply (DV_{DD}) to DGND	-0.3 V to 5.5 V
Input current, momentary	100 mA
Input current, continuous	10 mA
Analog input voltage	AV_{SS} – 0.3 V to AV_{DD} + 0.3 V
Digital input voltage to DGND	-0.3 V to DV_{DD} + 0.3 V
Maximum junction temperature (T_J)	+150°C
Storage temperature range	-60°C to +150°C
Thermal resistance, junction to case (θ_{JC})	20°C/W
Thermal resistance, junction to ambient (θ_{JA}) :	
High K	33°C/W 2/
Low K	75°C/W 3/

1.4 Recommended operating conditions. 4/

AV_{DD}	+2.5 V
AV_{SS}	-2.5 V
DV_{DD}	+3.3 V
Operating temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ High K specifies values determined on a JESD 51-7 highly conductive printed circuit board.
3/ Low K specifies values determined on a JESD 51-3 low conductive printed circuit board.
4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

EIA/JEDEC 51-3 – Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
EIA/JEDEC 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Analog multiplexer inputs section							
Absolute input voltage	V_{IN}	AIN0-AIN15, AINCOM with respect to DGND	-55°C to +125°C	01	AV_{SS} – 100 mV	AV_{DD} + 100 mV	V
			-40°C to +105°C	02	AV_{SS} – 100 mV	AV_{DD} + 100 mV	
On channel resistance	R_{ON}		-55°C to +125°C	01	80 typical		Ω
			-40°C to +105°C	02	80 typical		
Crosstalk	CT	f_{IN} = 1 kHz	-55°C to +125°C	01	-110 typical		dB
			-40°C to +105°C	02	-110 typical		
Sensor bias (current source)	SBCS	SBCS[1:0] = 01	-55°C to +125°C	01	1.5 typical		μA
			-40°C to +105°C	02	1.5 typical		
		SBCS[1:0] = 11	-55°C to +125°C	01	24 typical		
			-40°C to +105°C	02	24 typical		
1.5 μA:24 μA ratio error	RE		-55°C to +125°C	01	1 typical		%
			-40°C to +105°C	02	1 typical		
ADC input section							
Full scale input voltage	V_{FS}	V_{IN} = ADCINP – ADCINN	-55°C to +125°C	01	$\pm 1.0\overline{6}$ V_{REF} typical		V
			-40°C to +105°C	02	$\pm 1.0\overline{6}$ V_{REF} typical		
Absolute input voltage	V_{IN}	ADCINP, ADCINN	-55°C to +125°C	01	AV_{SS} – 100 mV	AV_{DD} + 100 mV	V
			-40°C to +105°C	02	AV_{SS} – 100 mV	AV_{DD} + 100 mV	
Differential input impedance	Z_{DIN}		-55°C to +125°C	01	65 typical		kΩ
			-40°C to +105°C	02	65 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
System performance section							
Resolution	RES	No missing codes	-55°C to +125°C	01	24		Bits
			-40°C to +105°C	02	24		
Data rate, fixed channel mode	DRF		-55°C to +125°C	01	1.953	125	kSPS
			-40°C to +105°C	02	1.953	125	
Data rate, auto scan mode	DRA		-55°C to +125°C	01	1.805	23.739	kSPS
			-40°C to +105°C	02	1.805	23.739	
Integral nonlinearity 3/	INL	Differential input	-55°C to +125°C	01	0.0003	0.0010	% of
			-40°C to +105°C	02	0.0003	0.0010	FSR 4/
Offset error, chopping off	OE	Shorted inputs	-55°C to +125°C	01	20 typical		µV
			-40°C to +105°C	02	20 typical		
Offset error, chopping on	OE	Shorted inputs	-55°C to +125°C	01	-650	650	µV
			-40°C to +105°C	02		10	
Offset drift, chopping off	OD	Shorted inputs	-55°C to +125°C	01	0.5 typical		µV/°C
			-40°C to +105°C	02	0.5 typical		
Offset drift, chopping on	OD	Shorted inputs	-55°C to +125°C	01		0.1	µV/°C
			-40°C to +105°C	02		01	
Gain error	GE		-55°C to +125°C	01	-0.5	0.5	%
			-40°C to +105°C	02		0.5	
Gain drift	GD		-55°C to +125°C	01	0.4 typical		ppm /
			-40°C to +105°C	02		2	°C
Noise	N		-55°C to +125°C	01	See table II		
			-40°C to +105°C	02	See table II		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
System performance section - continued.							
Common mode rejection ratio	CMRR	f_{CM} = 60 Hz	-55°C to +125°C	01	90		dB
			-40°C to +105°C	02	90		
Power supply rejection ratio, AV_{DD}, AV_{SS}	PSRR	f_{PS} = 60 Hz	-55°C to +125°C	01	70		dB
			-40°C to +105°C	02	70		
Power supply rejection ratio, DV_{DD}	PSRR	f_{PS} = 60 Hz	-55°C to +125°C	01	80		dB
			-40°C to +105°C	02	80		
Voltage reference input section							
Reference input voltage	V_{REF}	$V_{REF} = V_{REFP} - V_{REFN}$	-55°C to +125°C	01	0.5	AV_{DD} - AV_{SS}	V
			-40°C to +105°C	02	0.5	AV_{DD} - AV_{SS}	
Negative reference input	V_{REFN}		-55°C to +125°C	01	AV_{SS} – 0.1	V_{REFP} – 0.5	V
			-40°C to +105°C	02	AV_{SS} – 0.1	V_{REFP} – 0.5	
Positive reference input	V_{REFP}		-55°C to +125°C	01	V_{REFN} + 0.5	AV_{DD} + 0.1	V
			-40°C to +105°C	02	V_{REFN} + 0.5	AV_{DD} + 0.1	
Reference input impedance	Z_{RIN}		-55°C to +125°C	01	40 typical		kΩ
			-40°C to +105°C	02	40 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
System parameters section							
External reference reading error			-55°C to +125°C	01		3	%
			-40°C to +105°C	02		3	
Analog supply reading error			-55°C to +125°C	01		3	%
			-40°C to +105°C	02		3	
Temperature sensor reading, voltage			+25°C	01	168 typical		mV
				02	168 typical		
Temperature sensor reading, coefficient		Only device temperature forced; test printed circuit board (PCB) in free air.	+25°C	01	394 typical		µV/°C
				02	394 typical		
		Device and test PCB temperatures forced together.		01	563 typical		
				02	563 typical		
Digital input / output section							
Logic levels	V_{IH}		-55°C to +125°C	01	0.7 DV_{DD}	DV_{DD}	V
			-40°C to +105°C	02	0.7 DV_{DD}	DV_{DD}	
	V_{IL}		-55°C to +125°C	01	DGND	0.3 DV_{DD}	V
			-40°C to +105°C	02	DGND	0.3 DV_{DD}	
	V_{OH}	I_{OH} = 2 mA	-55°C to +125°C	01	0.8 DV_{DD}	DV_{DD}	V
			-40°C to +105°C	02	0.8 DV_{DD}	DV_{DD}	
	V_{OL}	I_{OL} = 2 mA	-55°C to +125°C	01	DGND	0.2 DV_{DD}	V
			-40°C to +105°C	02	DGND	0.2 DV_{DD}	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Digital input / output section - continued.							
Input leakage	I_{INL}	V_{IN} = DV_{DD}, GND	-55°C to +125°C	01		10	µA
			-40°C to +105°C	02		10	
Master clock input	CLKIO	Frequency	-55°C to +125°C	01	0.1	16	MHz
			-40°C to +105°C	02	0.1	16	
Master clock input	CLKIO	Duty cycle	-55°C to +125°C	01	40	60	%
			-40°C to +105°C	02	40	60	
Crystal oscillator							
Crystal frequency	f_{CRY}		-55°C to +125°C	01	32.768 typical		kHz
			-40°C to +105°C	02	32.768 typical		
Clock output frequency	f_{COUT}		-55°C to +125°C	01	15.729 typical		MHz
			-40°C to +105°C	02	15.729 typical		
Start up time, clock output valid			-55°C to +125°C	01	150 typical		ms
			-40°C to +105°C	02	150 typical		
Clock output duty cycle			-55°C to +125°C	01	40	60	%
			-40°C to +105°C	02	40	60	
Power supply section							
Digital supply voltage	DV_{DD}		-55°C to +125°C	01	2.7	5.25	V
			-40°C to +105°C	02	2.7	5.25	
Negative analog power supply	AV_{SS}		-55°C to +125°C	01	-2.6	0	V
			-40°C to +105°C	02	-2.6	0	
Positive analog power supply	AV_{DD}		-55°C to +125°C	01	AV_{SS} + 4.75	AV_{SS} + 5.25	V
			-40°C to +105°C	02	AV_{SS} + 4.75	AV_{SS} + 5.25	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power supply section – continued.							
DV_{DD} supply current							
External clock operation	I_{EC}		-55°C to +125°C	01		0.75	mA
			-40°C to +105°C	02		0.6	
Internal oscillator operation, clock output disabled	I_{OED}		-55°C to +125°C	01	0.04 typical		mA
			-40°C to +105°C	02	0.04 typical		
Internal oscillator 5/ operation, clock output enabled	I_{COE}		-55°C to +125°C	01	1.4 typical		mA
			-40°C to +105°C	02	1.4 typical		
Power down 6/	I_{PD}		-55°C to +125°C	01		25	µA
			-40°C to +105°C	02		25	
AV_{DD}, AV_{SS} supply current							
Converting	I_C		-55°C to +125°C	01		12	mA
			-40°C to +105°C	02		12	
Standby	I_{SB}		-55°C to +125°C	01	5.6 typical		mA
			-40°C to +105°C	02	5.6 typical		
Sleep	I_{SL}		-55°C to +125°C	01	2.1 typical		mA
			-40°C to +105°C	02	2.1 typical		
Power down	I_{PD}		-55°C to +125°C	01		85	µA
			-40°C to +105°C	02		85	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power dissipation section							
Converting	P_C		-55°C to +125°C	01		62	mW
			-40°C to +105°C	02		62	
Standby	P_{SB}		-55°C to +125°C	01	29 typical		mW
			-40°C to +105°C	02	29 typical		
Sleep	P_{SL}		-55°C to +125°C	01	11 typical		mW
			-40°C to +105°C	02	11 typical		
Power down	P_D		-55°C to +125°C	01	14 typical		µW
			-40°C to +105°C	02	14 typical		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, AV_{DD} = +2.5 V, AV_{SS} = -2.5 V, DV_{DD} = +3.3 V, f_{CLK} = 16 MHz (external clock) or f_{CLK} = 15.729 MHz (internal clock), an OPA227 device buffer between multiplexer differential (MUX) outputs and ADC inputs, V_{REF} = +4.096 V, and V_{REFN} = -2.5 V.

3/ Best straight line fit method provides information about offset (intercept) and gain (slope) error. It determines in the form of a straight line, the closet approximation to the analog to digital converter actual transfer function. This approach yields the best repeatability and true representation of linearity.

4/ Full scale range (FSR) = $2.1\overline{3}\ V_{REF}$.

5/ CLKIO load = 20 pF.

6/ No clock applied to CLKIO.

Case X

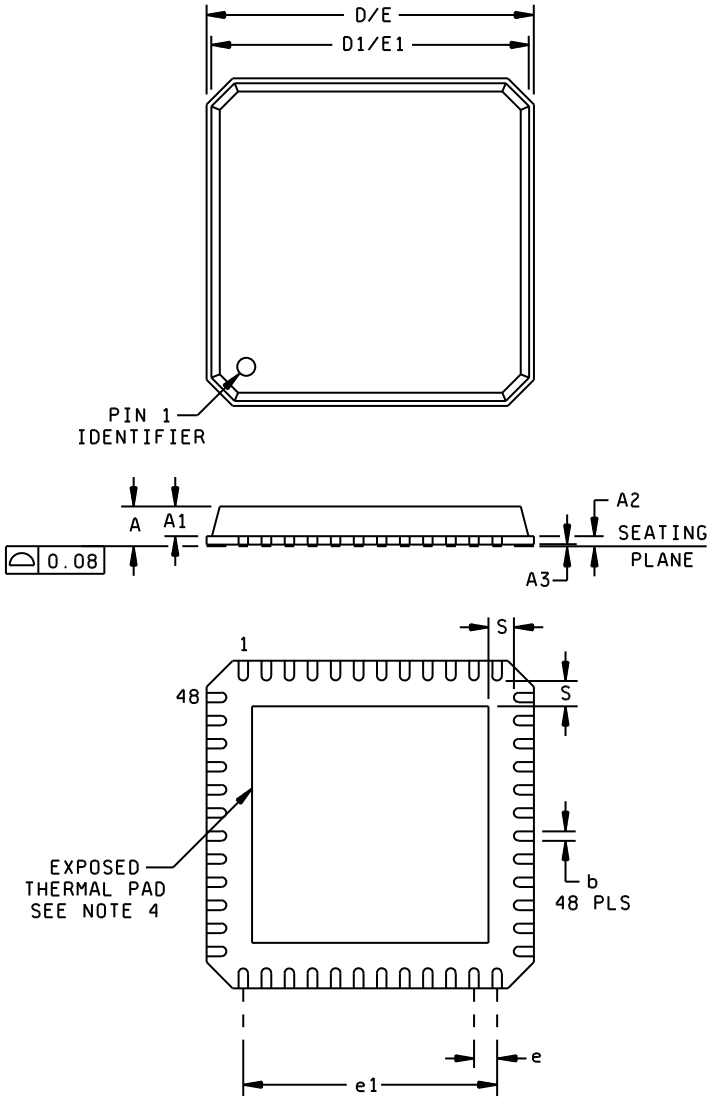


FIGURE 1. Case outlines.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.035	---	0.90
A1	---	.027	---	0.70
A2	.007 reference		0.20 reference	
A3	.000	.001	0.00	0.05
b	.007	.011	0.18	0.30
D / E	.271	.279	6.90	7.10
D1 / E1	.261	.269	6.65	6.85
e	.019 BSC		0.50 BSC	
e1	.216 reference		5.50 reference	
s	.009	---	0.25	---
n	48		48	

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. This drawing is subject to change without notice.
3. QFN (quad flat pack with no loads) package configuration.
4. The package thermal pad must be soldered to the board for thermal and mechanical performance.

FIGURE 1. Case outlines - Continued.

Case Y

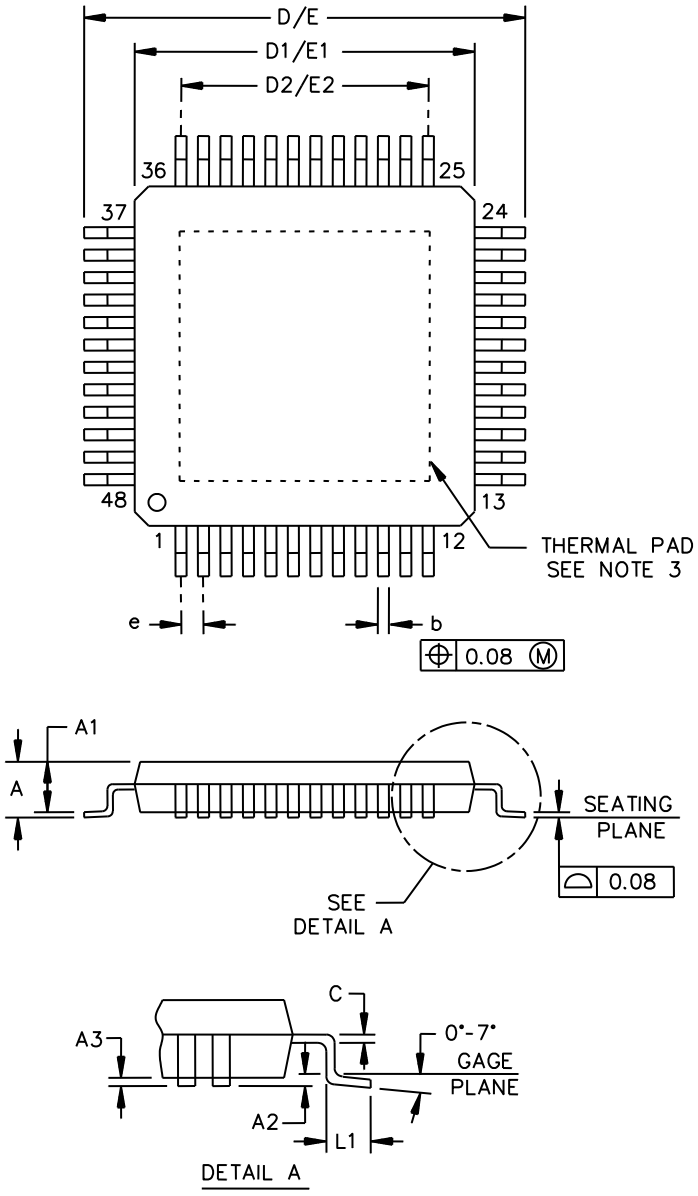


FIGURE 1. Case outlines - continued.

Case Y - continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.047	---	1.20
A1	.037	.041	0.95	1.05
A2	.009	---	0.25	---
A3	.001	.005	0.05	0.15
b	.006	.010	0.17	0.27
c	.005	---	0.13	---
D	.346	.362	8.80	9.20
D1	.267	.283	6.80	7.20
D2	.216	---	5.50	---
E	.346	.362	8.80	9.20
E1	.267	.283	6.80	7.20
E2	.216	---	5.50	---
e	.019 BSC		0.50 BSC	
L1	.017	.029	0.45	0.75

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. D1/E1 body dimensions do not include mold flash, protrusion, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm (.006 inch) per side.
3. This package is designed to be soldered to a thermal pad on the board. Refer to technical brief, powerpad thermally enhanced package, manufacturer's literature number SLMA002 for information regarding recommended board layout.
4. Falls within JEDEC MS-026.

FIGURE 1. Case outlines – Continued.

Device types	01 and 02		
Case outlines	X and Y		
Terminal number	Terminal symbol	Analog / Digital Input / Output	Description
1	AIN3	Analog input	Analog input 3: single ended channel 3, differential channel 1 (-)
2	AIN2	Analog input	Analog input 2: single ended channel 2, differential channel 1 (+)
3	AIN1	Analog input	Analog input 1: single ended channel 1, differential channel 0 (-)
4	AIN0	Analog input	Analog input 0: single ended channel 0, differential channel 0 (+)
5	AV_{SS}	Analog	Negative analog power supply: 0 V for unipolar operation, -2.5 V for bipolar operation. (internally connected to exposed thermal pad of case outline X.)
6	AV_{DD}	Analog	Positive analog power supply: 5 V for unipolar operation, 2.5 V for bipolar operation.
7	PLLCAP	Analog	Phase locked loop (PLL) bypass capacitor: connect 22 nF capacitor to AV_{SS} when using crystal oscillator.
8	XTAL1	Analog	32.768 kHz crystal oscillator input 1. See crystal oscillator section of manufacturer's datasheet.
9	XTAL2	Analog	32.768 kHz crystal oscillator input 2. See crystal oscillator section of manufacturer's datasheet.
10	$\overline{PWDN}$	Digital input	Power down input: hold low for minimum of two f_{CLK} cycles to engage low power mode.
11	$\overline{RESET}$	Digital input	Reset input: hold low for minimum of two f_{CLK} cycles to reset the device.
12	CLKSEL	Digital input	Clock select input: Low = activates crystal oscillator, f_{CLK} output on CLKIO. High = disables crystal oscillator, apply f_{CLK} to CLKIO.
13	CLKIO	Digital I/O	System clock input/output (see CLKSEL pin).
14	GPIO0	Digital I/O	General purpose digital input/output 0.
15	GPIO1	Digital I/O	General purpose digital input/output 1.
16	GPIO2	Digital I/O	General purpose digital input/output 2.
17	GPIO3	Digital I/O	General purpose digital input/output 3.
18	GPIO4	Digital I/O	General purpose digital input/output 4.
19	GPIO5	Digital I/O	General purpose digital input/output 5.
20	GPIO6	Digital I/O	General purpose digital input/output 6.
21	GPIO7	Digital I/O	General purpose digital input/output 7.

FIGURE 2. Terminal connections.

Device types	01 and 02		
Case outlines	X and Y		
Terminal number	Terminal symbol	Analog / Digital Input / Output	Description
22	SCLK	Digital input	Serial peripheral interface (SPI) clock input: data clocked in on rising edge, clocked out on falling edge.
23	DIN	Digital input	SPI interface data input: data is input to the device .
24	DOUT	Digital output	SPI interface data output: data is output from the device.
25	$\overline{\text{DRDY}}$	Digital output	Data ready output: active low.
26	START	Digital input	Start conversion input: active high.
27	$\overline{\text{CS}}$	Digital input	SPI interface chip select input: active low.
28	DVDD	Digital	Digital power supply: 2.7 V to 5.25 V
29	DGND	Digital	Digital ground.
30	VREFN	Analog input	Reference input negative.
31	VREFP	Analog input	Reference input positive.
32	AINCOM	Analog input	Analog input common: Common input pin to all single ended inputs.
33	AIN15	Analog input	Analog input 15: single ended channel 15, differential channel 7 (-).
34	AIN14	Analog input	Analog input 14: single ended channel 14, differential channel 7 (+).
35	AIN13	Analog input	Analog input 13: single ended channel 13, differential channel 6 (-).
36	AIN12	Analog input	Analog input 12: single ended channel 12, differential channel 6 (+).
37	AIN11	Analog input	Analog input 11: single ended channel 11, differential channel 5 (-).
38	AIN10	Analog input	Analog input 10: single ended channel 10, differential channel 5 (+).
39	AIN9	Analog input	Analog input 9: single ended channel 9, differential channel 4 (-).
40	AIN8	Analog input	Analog input 8: single ended channel 8, differential channel 4 (+).
41	ADCINN	Analog input	ADC differential input (-)
42	ADCINP	Analog input	ADC differential input (+)
43	MUXOUTN	Analog output	Multiplexer differential output (-)
44	MUXOUTP	Analog output	Multiplexer differential output(+)
45	AIN7	Analog input	Analog input 7: single ended channel 7, differential channel 3 (-).
46	AIN6	Analog input	Analog input 6: single ended channel 6, differential channel 3 (+).
47	AIN5	Analog input	Analog input 5: single ended channel 5, differential channel 2 (-).
48	AIN4	Analog input	Analog input 4: single ended channel 4, differential channel 2 (+).

FIGURE 2. Terminal connections – continued.

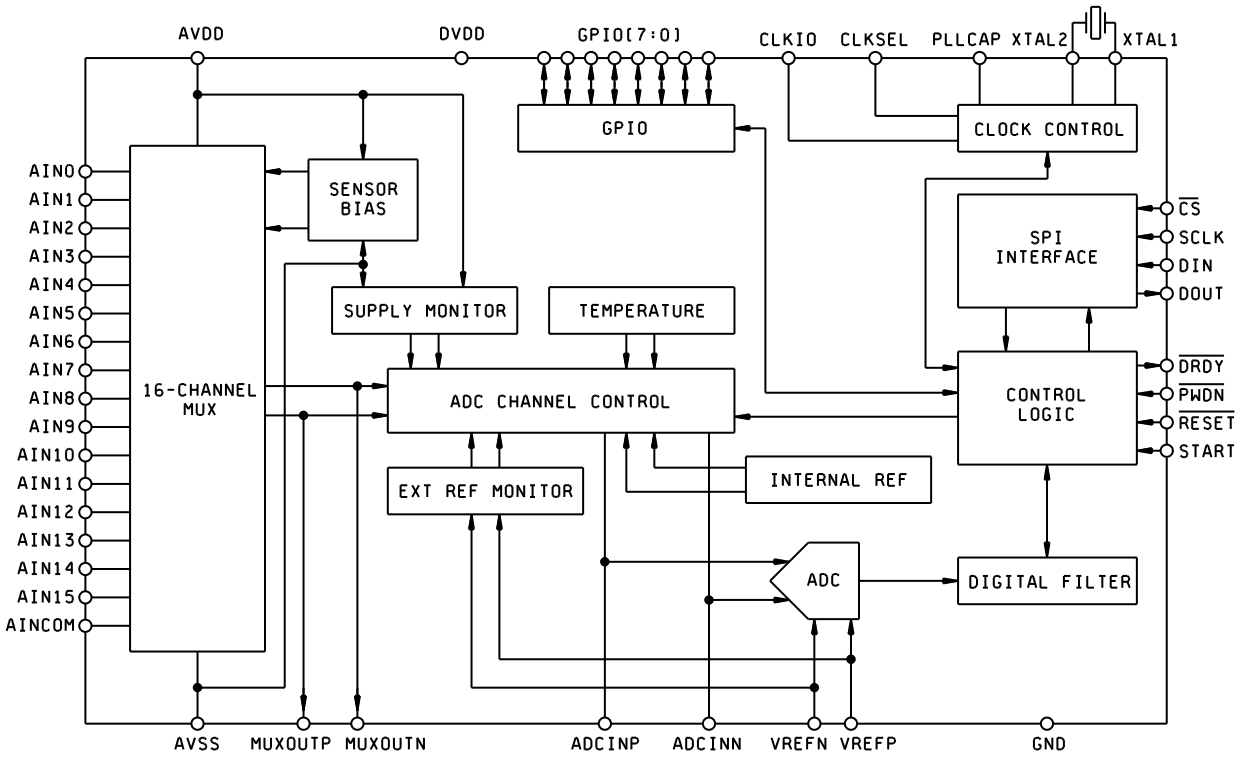
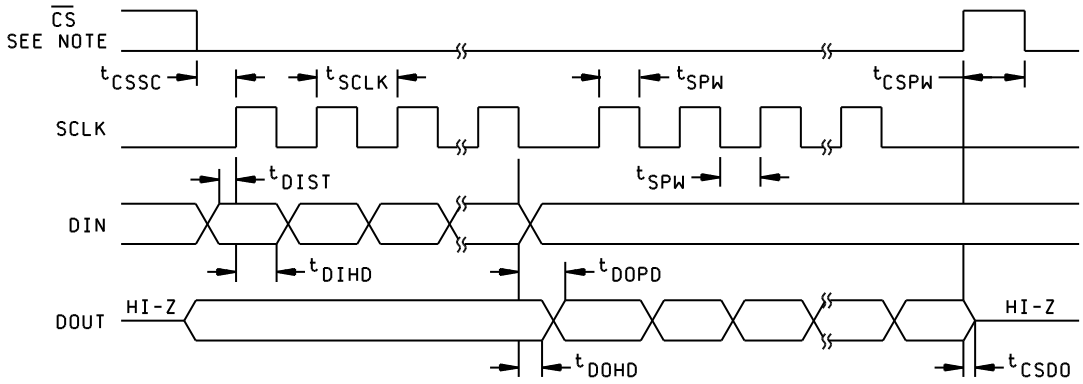


FIGURE 3. Block diagram.



Serial interface timing characteristics. 1/

Symbol	Description	Min	Max	Units
t_{SCLK}	SCLK period	2		τ_{CLK} 2/
t_{SPW}	SCLK high or low pulse width (exceeding maximum resets SPI interface)	0.8	4096 3/	τ_{CLK}
t_{CSSC}	$\overline{CS}$ low to first SCLK: setup time 4/	2.5		τ_{CLK}
t_{DIST}	Valid DIN to SCLK rising edge: setup time	10		ns
t_{DIHD}	Valid DIN to SCLK rising edge: hold time	5		ns
t_{DOPD}	SCLK falling edge to valid new DOUT: 5/ propagation delay		20	ns
t_{DOHD}	SCLK falling edge to old DOUT invalid: hold time	0		ns
t_{CSDO}	$\overline{CS}$ high to DOUT invalid (tri-state)		5	τ_{CLK}
t_{CSPW}	$\overline{CS}$ pulse width high	2		τ_{CLK}

1/ Unless otherwise specified, T_A = -40°C to +105°C ensured by characterization only and DV_{DD} = 2.7 V to 5.25 V

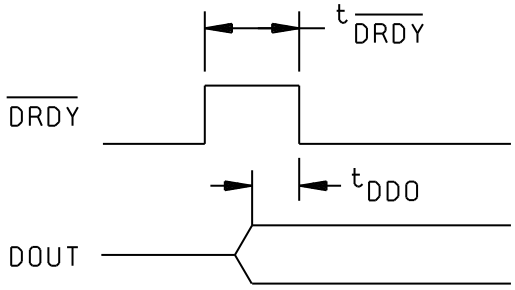
2/ τ_{CLK} = master clock period = $1/f_{CLK}$.

3/ Programmable to 256 τ_{CLK}.

4/ $\overline{CS}$ can be tied low.

5/ DOUT load = 20 pF || 100 kΩ to DGND.

FIGURE 4. Timing waveforms.



$\overline{DRDY}$ update timing characteristics

Symbol	Description	Typical	Units
$t_{\overline{DRDY}}$	$\overline{DRDY}$ high pulse width without data read	1	τ_{CLK}
t_{DDO}	Valid DOUT to $\overline{DRDY}$ falling edge ($\overline{CS}$ = 0)	0.5	τ_{CLK}

FIGURE 4. Timing waveforms – continued.

TABLE II. Noise performance. 1/

DRATE[1:0]	Data rate auto scan mode (SPS)	Data rate fixed channel mode (SPS)	Input referred noise (μV_{RMS})	Noise free resolution (Bits)	Effective number of bits (ENOB)
11	23739	125000	12	16.8	19.5
10	15123	31250	7.9	17.4	20.1
01	6168	7813	4.5	18.2	20.9
00	1835	1953	2.8	18.9	21.6

1/ V_{REF} = 4.096 V, f_{CLK} = 16 MHZ, chop = 0, delay = 0, inputs shorted, and 2048 sample size.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/ 2/	Device manufacturer CAGE code	Package 3/		Top side marking	Vendor part number
V62/09626-01XE	01295	48 / RTC	Tape and reel of 250	1258MEP	ADS1258MRTCTEP
V62/09626-01YE	01295	48 / PHP	Tray of 250	ADS1258MEP	ADS1258MPHPTEP
V62/09626-02YE	01295	48 / PHP	Tape and reel of 250	ADS1258IEP	ADS1258IPHPREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet.
3/ Package drawings, standard packaging quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available from the manufacturer.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243