REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 09-07-21	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL, MIXED SIGNAL MICROCONTROLLER, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/09620**
	REV	**PAGE** 1 **OF** 47

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance mixed signal microcontroller microcircuit, with an operating temperature range of -40°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/09620	-	01	X	A
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	MSP430F2618-EP	Mixed signal microcontroller

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	113	JEDEC MO-225	Plastic ball grid array

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Voltage applied at V_{CC} to V_{SS} ..... -0.3 V to 4.1 V
Voltage applied to any pin ..... -0.3 V to V_{CC} + 0.3 V 2/
Diode current at any device terminal ..... ±2 mA
Storage temperature range, T_{STG} (Unprogrammed device) ..... -55°C to 150°C 3/
Storage temperature range, T_{STG} (Programmed device) ..... -40°C to 105°C 3/

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ All voltages referenced to V_{SS}. The JTAG fuse blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.

3/ Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

1.4 Recommended operating conditions.

Supply voltage during program execution (V_{CC}) ..... 1.8 V to 3.6 V 4/
Supply voltage during flash memory programming (V_{CC}) ..... 2.2 V to 3.6 V 4/
Supply voltage (V_{SS}) ..... 0.0 V 5/
Processor frequency f_{SYSTEM} range (Maximum MCLK frequency): 6/ 7/ See figure 4.
V_{CC} = 1.8 V, Duty Cycle 50% ±10% ..... dc to 4.15 MHz
V_{CC} = 2.7 V, Duty Cycle 50% ±10% ..... dc to 12 MHz
V_{CC} ≥ 3.3 V, Duty Cycle 50% ±10% ..... dc to 16 MHz
Operating free air temperature range, T_A ..... -40°C to 105°C

2. APPLICABLE DOCUMENTS

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
JEDEC J-STD-020 – Joint IPC/JEDEC standard for moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices.

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

4/ AV_{CC} = DV_{CC} = V_{CC}. It is recommended to power AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power-up.
5/ AV_{SS} = DV_{SS} = V_{SS}.
6/ The CPU is clocked directly with MCLK.
7/ Modules might have a different maximum input clock specification. Refer to the data sheet from the manufacturer.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Operating area. The operating area shall be as shown in figure 4.

3.5.5 Active mode supply current. The active mode supply current shall be as shown in figure 5.

3.5.6 POR/Brownout reset. The POR/Brownout reset shall be as shown in figures 6 -8.

3.5.7 Test circuits and timing waveforms. The test circuits and timing waveforms shall be as shown in figures 9-24.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	T_A	V_{CC}	Limits		Unit
					Min	Max	
Active mode supply current into V_{CC} excluding external current 3/ 4/ See figure 5.							
Active mode (AM) current (1 MHz)	$I_{AM,}$ 1 MHz	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 1$ MHz, $f_{ACLK} = 32{,}768$ Hz, Program executes from flash, BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	-40°C to 85°C	2.2 V		395	µA
			105°C			420	
			-40°C to 85°C	3 V		560	
			105°C			595	
Active mode (AM) current (1 MHz)	$I_{AM,}$ 1 MHz	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 1$ MHz, $f_{ACLK} = 32{,}768$ Hz, Program executes in RAM, BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	-40°C to 85°C	2.2 V		370	µA
			105°C			390	
			-40°C to 85°C	3 V		495	
			105°C			520	
Active mode (AM) current (4 kHz)	$I_{AM,}$ 4 kHz	$f_{MCLK} = f_{SMCLK} = f_{ACLK} = 32{,}768$ Hz/8 = 4096 Hz, $f_{DCO} = 0$ Hz, Program executes in flash, SELMx = 11, SELS = 1, DIVMx = DIVSx = DIVAx = 11, CPUOFF = 0, SCGO = 0, SCG1 = 0, OSCOFF = 0	-40°C to 85°C	2.2 V		9	µA
			105°C			31	
			-40°C to 85°C	3 V		11	
			105°C			32	
Active mode (AM) current (100 kHz)	$I_{AM,}$ 100 kHz	$f_{MCLK} = f_{SMCLK} = f_{DCO(0,0)} \approx 100$ kHz, $f_{ACLK} = 0$ Hz, Program executes in flash, RSELx = 0, DCOx = 0, CPUOFF = 0, SCGO = 0, SCG1 = 0, OSCOFF = 1	-40°C to 85°C	2.2 V		86	µA
			105°C			99	
			-40°C to 85°C	3 V		107	
			105°C			128	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	T_A	V_{CC}	Limits		Unit
					Min	Max	
Low-power mode supply current into V_{CC} excluding external current 3/ 4/							
Low power mode 0, (LPM0) current 5/	$I_{LPM0,}$ 1 MHz	f_{MCLK} = 0 MHz, f_{SMCLK}= f_{DCO} = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	-40°C to 85°C	2.2 V		83	µA
			105°C			98	
			-40°C to 85°C	3 V		105	
			105°C			125	
Low power mode 0, (LPM0) current 5/	$I_{LPM0,}$ 100 kHz	f_{MCLK} = 0 MHz, f_{SMCLK}= $f_{DCO(0,0)}$ ≈ 100 kHz, f_{ACLK} = 0 Hz, RSELx = 0, DCOx = 0, CPUOFF = 1, SCGO = 0, SCG1 = 0, OSCOFF = 1	-40°C to 85°C	2.2 V		49	µA
			105°C			62	
			-40°C to 85°C	3 V		55	
			105°C			73	
Low power mode 2 (LPM2) current 6/	I_{LPM2}	f_{MCLK} = f_{SMCLK}= 0 MHz, f_{DCO} = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	-40°C to 85°C	2.2 V		33	µA
			105°C			46	
			-40°C to 85°C	3 V		36	
			105°C			55	
Low power mode 3 (LPM3) current 6/	$I_{LPM3,}$ LFXT1	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32,768 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-40°C	2.2 V		1.2	µA
			25°C			1.3	
			85°C			7	
			105°C			24	
			-40°C	3 V		1.3	
			25°C			1.5	
			85°C			8	
			105°C			30	
Low power mode 3 current (LPM3) 6/	$I_{LPM3,}$ VLO	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-40°C	2.2 V		1.0	µA
			25°C			1.0	
			85°C			6.5	
			105°C			24	
			-40°C	3 V		1.2	
			25°C			1.2	
			85°C			7.5	
			105°C			29.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	T_A	V_{CC}	Limits		Unit
					Min	Max	
Low-power mode supply current into V_{CC} excluding external current - Continued. 3/ 4/							
Low power mode 4 current (LPM4) 7/	I_{LPM4}	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 0$ MHz, $f_{ACLK} = 0$ Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	-40°C	2.2 V		0.5	µA
			25°C			0.5	
			85°C			6	
			105°C			23	
			-40°C	3 V		0.5	
			25°C			0.5	
			85°C			7	
			105°C			24	
Schmitt-trigger inputs - ports P1 through P8, RST/$\overline{NMI}$, JTAG, XIN, and XT2IN 8/							
Positive-going input threshold voltage	V_{IT+}		-40°C to 105°C		0.45 x V_{CC}	0.75 x V_{CC}	V
				2.2 V	1.0	1.65	
				3 V	1.35	2.25	
Negative-going input threshold voltage	V_{IT-}		-40°C to 105°C		0.25 x V_{CC}	0.55 x V_{CC}	V
				2.2 V	0.55	1.2	
				3 V	0.75	1.65	
Input voltage hysteresis ($V_{IT+} - V_{IT-}$)	Vhys		-40°C to 105°C	2.2 V	0.2	1.0	V
				3 V	0.3	1.0	
Pullup/Pulldown resistor	R_{Pull}	Pullup: $V_{IN} = V_{SS}$, Pulldown: $V_{IN} = V_{CC}$	-40°C to 105°C		20	50	kΩ
Input capacitance	C_I	$V_{IN} = V_{SS}$ or V_{CC}	-40°C to 105°C		5 TYP		pF
Input - ports P1 and P2							
External interrupt timing	$t_{(int)}$	Port P1, P2: P1.x to P2.x, external trigger pulse width to set interrupt flag. 9/	-40°C to 105°C	2.2 V/ 3 V	20		ns
Leakage current - ports P1 through P8							
High-impedance leakage current	$I_{lkg(Px.x)}$	10/ 11/	-40°C to 105°C	2.2 V/ 3 V		±50	nA
Standard inputs – $\overline{RST}$ /NMI							
Low-level input voltage	V_{IL}		-40°C to 105°C	2.2 V/ 3 V	V_{SS}	V_{SS} + 0.6	V
High-level input voltage	V_{IH}		-40°C to 105°C	2.2 V/ 3 V	0.8 x V_{CC}	V_{CC}	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	T_A	V_{CC}	Limits		Unit
					Min	Max	
Outputs - ports P1 through P8							
High-level output voltage	V_{OH}	$I_{OH(max)}$ = -1.5 mA 12/	-40°C to 105°C	2.2 V	V_{CC} – 0.25	V_{CC}	V
		$I_{OH(max)}$ = -6 mA 13/			V_{CC} – 0.6	V_{CC}	
		$I_{OH(max)}$ = -1.5 mA 12/		3 V	V_{CC} – 0.25	V_{CC}	
		$I_{OH(max)}$ = -6 mA 13/			V_{CC} – 0.6	V_{CC}	
Low-level output voltage	V_{OL}	$I_{OL(max)}$ = 1.5 mA 12/	-40°C to 105°C	2.2 V	V_{SS}	V_{SS} + 0.25	V
		$I_{OL(max)}$ = 6 mA 13/			V_{SS}	V_{SS} + 0.6	
		$I_{OL(max)}$ = 1.5 mA 12/		3 V	V_{SS}	V_{SS} + 0.25	
		$I_{OL(max)}$ = 6 mA 13/			V_{SS}	V_{SS} + 0.6	
Output frequency - ports P1 through P8							
Port output frequency with load	$f_{Px.y}$	P1.4/SMCLK, C_L = 20 pF, R_L = 1 kΩ 14/ 15/	-40°C to 105°C	2.2 V	dc	10	MHz
				3 V	dc	12	
Clock output frequency	f_{Port_CLK}	P2.0/ACLK/CA2, P1.4/SMCLK, CL = 20 pF 15/	-40°C to 105°C	2.2 V	dc	12	MHz
				3 V	dc	16	
Duty cycle of output frequency	$t_{(Xdc)}$	P5.6/ACLK, C_L = 20 pF, LF mode	-40°C to 105°C		30	70	%
		P5.6/ACLK, C_L = 20 pF, XT1 mode			40	60	
		P5.4/MCLK, C_L = 20 pF, XT1 mode			40	60	
		P5.4/MCLK, C_L = 20 pF, DCO			50% - 15 ns	50% + 15 ns	
		P1.4/SMCLK, C_L = 20 pF, XT2 mode			40	60	%
		P1.4/SMCLK, C_L = 20 pF, DCO			50% - 15 ns	50% + 15 ns	
POR/brownout reset (BOR) 16/ 17/ See figure 6 - 8.							
Operating voltage	$V_{CC(start)}$	$dV_{CC}/dt \leq 3$ V/s	-40°C to 105°C		0.7 x $V_{(B_IT-)}$ TYP		V
Negative going V_{CC} reset threshold voltage	$V_{(B_IT-)}$	$dV_{CC}/dt \leq 3$ V/s	-40°C to 105°C			1.71	V
V_{CC} reset threshold hysteresis	$V_{hys(B_IT-)}$	$dV_{CC}/dt \leq 3$ V/s	-40°C to 105°C		70	210	mV
BOR reset release delay time	$t_{d(BOR)}$		-40°C to 105°C			2000	µs
Pulse length at $\overline{RST}$/NMI pin to accept a reset	$t_{(reset)}$		-40°C to 105°C	2.2 V/ 3V	2		µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified		T_A	V_{CC}	Limits Min	Limits Max	Unit
SVS (Supply voltage supervisor/monitor)								
	$t_{(SVSR)}$	$dV_{CC}/dt > 30$ V/ms See figure 9.		-40°C to 105°C		5	150	µs
		$dV_{CC}/dt \leq 30$ V/ms					2000	
	$t_{d(SVSon)}$	SVSON, switch from VLD = 0 to VLD ≠ 0		-40°C to 105°C	3 V	20	150	µs
	t_{settle}	VLD ≠ 0 18/		-40°C to 105°C			12	µs
	$V_{(SVSstart)}$	VLD ≠ 0, $V_{CC}/dt \leq 3$ V/s See figure 9.		-40°C to 105°C			1.7	V
	$V_{hys(SVS_IT-)}$	$V_{CC}/dt \leq 3$ V/s See figure 9.	VLD = 1	-40°C to 105°C		70	210	mV
			VLD = 2 to 14			$V_{(SVS_IT-)}$ x 0.004	$V_{(SVS_IT-)}$ x 0.016	V
		$V_{CC}/dt \leq 3$ V/s See figure 9. External voltage applied on A7.	VLD = 15			4.4	20	mV
	$V_{(SVS_IT-)}$	$V_{CC}/dt \leq 3$ V/s See figure 9 and figure 10.	VLD = 1	-40°C to 105°C		1.8	2.05	V
			VLD = 2			1.94	2.25	
			VLD = 3			2.05	2.37	
			VLD = 4			2.14	2.48	
			VLD = 5			2.24	2.6	
			VLD = 6			2.33	2.71	
			VLD = 7			2.46	2.86	
			VLD = 8			2.58	3	
			VLD = 9			2.69	3.13	
			VLD = 10			2.83	3.29	
			VLD = 11			2.94	3.42	
			VLD = 12			3.11	3.61 19/	
			VLD = 13			3.24	3.76 19/	
			VLD = 14			3.43	3.99 19/	
		$V_{CC}/dt \leq 3$ V/s See figure 9 and figure 10. External voltage applied on A7.	VLD = 15			1.1	1.3	
	$I_{CC(SVS)}$ 20/	VLD ≠ 0		-40°C to 105°C	2.2 V/ 3 V		15	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	T_A	V_{CC}	Limits		Unit
					Min	Max	
DCO frequency							
Supply voltage range	V_{CC}	RSELx < 14	-40°C to 105°C		1.8	3.6	V
		RSELx = 14			2.2	3.6	
		RSELx = 15			3.0	3.6	
DCO frequency (0, 0)	$f_{DCO(0, 0)}$	RSELx = 0, DCOx = 0, MODx = 0	-40°C to 105°C	2.2 V/ 3 V	0.06	0.14	MHz
DCO frequency (0, 3)	$f_{DCO(0, 3)}$	RSELx = 0, DCOx = 3, MODx = 0			0.07	0.17	
DCO frequency (1, 3)	$f_{DCO(1, 3)}$	RSELx = 1, DCOx = 3, MODx = 0			0.10	0.20	
DCO frequency (2, 3)	$f_{DCO(2, 3)}$	RSELx = 2, DCOx = 3, MODx = 0			0.14	0.28	
DCO frequency (3, 3)	$f_{DCO(3, 3)}$	RSELx = 3, DCOx = 3, MODx = 0			0.20	0.40	
DCO frequency (4, 3)	$f_{DCO(4, 3)}$	RSELx = 4, DCOx = 3, MODx = 0			0.28	0.54	
DCO frequency (5, 3)	$f_{DCO(5, 3)}$	RSELx = 5, DCOx = 3, MODx = 0			0.39	0.77	
DCO frequency (6, 3)	$f_{DCO(6, 3)}$	RSELx = 6, DCOx = 3, MODx = 0			0.54	1.06	
DCO frequency (7, 3)	$f_{DCO(7, 3)}$	RSELx = 7, DCOx = 3, MODx = 0			0.80	1.50	
DCO frequency (8, 3)	$f_{DCO(8, 3)}$	RSELx = 8, DCOx = 3, MODx = 0			1.10	2.10	
DCO frequency (9, 3)	$f_{DCO(9, 3)}$	RSELx = 9, DCOx = 3, MODx = 0			1.60	3.00	
DCO frequency (10, 3)	$f_{DCO(10, 3)}$	RSELx = 10, DCOx = 3, MODx = 0			2.50	4.30	
DCO frequency (11, 3)	$f_{DCO(11, 3)}$	RSELx = 11, DCOx = 3, MODx = 0			3.00	5.50	
DCO frequency (12, 3)	$f_{DCO(12, 3)}$	RSELx = 12, DCOx = 3, MODx = 0			4.30	7.30	
DCO frequency (13, 3)	$f_{DCO(13, 3)}$	RSELx = 13, DCOx = 3, MODx = 0			6.00	9.60	
DCO frequency (14, 3)	$f_{DCO(14, 3)}$	RSELx = 14, DCOx = 3, MODx = 0			8.60	13.9	
DCO frequency (15, 3)	$f_{DCO(15, 3)}$	RSELx = 15, DCOx = 3, MODx = 0		3 V	12.0	18.5	
DCO frequency (15, 7)	$f_{DCO(15, 7)}$	RSELx = 15, DCOx = 7, MODx = 0			16.0	26.0	
Frequency step between range RSEL and RSEL+1	S_{RSEL}	SRSEL = $f_{DCO(RSEL+1, DCO)}/f_{DCO(RSEL, DCO)}$	-40°C to 105°C	2.2 V/ 3 V		1.55	ratio
Frequency step between tap DCO and DCO+1	S_{DCO}	SDCO = $f_{DCO(RSEL, DCO+1)}/f_{DCO(RSEL, DCO)}$	-40°C to 105°C	2.2 V/ 3 V	1.05	1.12	ratio
Duty cycle		Measured at P1.4/SMCLK	-40°C to 105°C	2.2 V/ 3 V	40	60	%

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	T_A	V_{CC}	Limits		Unit
					Min	Max	
Calibrated DCO frequencies - tolerance at calibration							
Frequency tolerance at calibration			25°C	3 V	-1	1	%
1 MHz calibration value	$f_{CAL(1\ MHz)}$	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, Gating time: 5 ms	25°C	3 V	0.990	1.010	MHz
8 MHz calibration value	$f_{CAL(8\ MHz)}$	BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz, Gating time: 5 ms	25°C	3 V	7.920	8.080	MHz
12 MHz calibration value	$f_{CAL(12\ MHz)}$	BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz, Gating time: 5 ms	25°C	3 V	11.88	12.12	MHz
16 MHz calibration value	$f_{CAL(16\ MHz)}$	BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz, Gating time: 2 ms	25°C	3 V	15.84	16.16	MHz
Calibrated DCO frequencies - tolerance over temperature range 0°C to 85°C							
1 MHz tolerance over temperature			0°C to 85°C	3 V	-2.5	2.5	%
8 MHz tolerance over temperature			0°C to 85°C	3 V	-2.5	2.5	%
12 MHz tolerance over temperature			0°C to 85°C	3 V	-2.5	2.5	%
16 MHz tolerance over temperature			0°C to 85°C	3 V	-3.0	3.0	%
1 MHz calibration value	$f_{CAL(1\ MHz)}$	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, Gating time: 5 ms	0°C to 85°C	2.2 V	0.970	1.030	MHz
				3V	0.975	1.025	
				3.6 V	0.970	1.030	
8 MHz calibration value	$f_{CAL(8\ MHz)}$	BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz, Gating time: 5 ms	0°C to 85°C	2.2 V	7.760	8.400	MHz
				3V	7.800	8.200	
				3.6 V	7.600	8.240	
12 MHz calibration value	$f_{CAL(12\ MHz)}$	BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz, Gating time: 5 ms	0°C to 85°C	2.2 V	11.64	12.36	MHz
				3V	11.64	12.36	
				3.6 V	11.64	12.36	
16 MHz calibration value	$f_{CAL(16\ MHz)}$	BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz, Gating time: 2 ms	0°C to 85°C	3V	15.52	16.48	MHz
				3.6 V	15.00	16.48	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	T_A	V_{CC}	Limits		Unit
					Min	Max	
Calibrated DCO frequencies - tolerance over supply voltage V_{CC}							
1 MHz tolerance over V_{CC}			25°C	1.8 V to 3.6 V	-3	3	%
8 MHz tolerance over V_{CC}			25°C	1.8 V to 3.6 V	-3	3	%
12 MHz tolerance over V_{CC}			25°C	2.2 V to 3.6 V	-3	3	%
16 MHz tolerance over V_{CC}			25°C	3 V to 3.6 V	-3	3	%
1 MHz calibration value	$f_{CAL(1\ MHz)}$	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, Gating time: 5 ms	25°C	1.8 V to 3.6 V	0.970	1.030	MHz
8 MHz calibration value	$f_{CAL(8\ MHz)}$	BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz, Gating time: 5 ms	25°C	1.8 V to 3.6 V	7.760	8.240	MHz
12 MHz calibration value	$f_{CAL(12\ MHz)}$	BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz, Gating time: 5 ms	25°C	2.2 V to 3.6 V	11.64	12.36	MHz
16 MHz calibration value	$f_{CAL(16\ MHz)}$	BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz, Gating time: 2 ms	25°C	3 V to 3.6 V	15.00	16.48	MHz
Calibrated DCO frequencies - overall tolerance							
1 MHz tolerance overall			-40°C to 105°C	1.8 V to 3.6 V	-5	+5	%
8 MHz tolerance overall			-40°C to 105°C	1.8 V to 3.6 V	-5	+5	%
12 MHz tolerance overall			-40°C to 105°C	2.2 V to 3.6 V	-5	+5	%
16 MHz tolerance overall			-40°C to 105°C	3 V to 3.6 V	-6	+6	%
1 MHz calibration value	$f_{CAL(1\ MHz)}$	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, Gating time: 5 ms	-40°C to 105°C	1.8 V to 3.6 V	0.950	1.050	MHz
8 MHz calibration value	$f_{CAL(8\ MHz)}$	BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz, Gating time: 5 ms	-40°C to 105°C	1.8 V to 3.6 V	7.600	8.400	MHz
12 MHz calibration value	$f_{CAL(12\ MHz)}$	BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz, Gating time: 5 ms	-40°C to 105°C	2.2 V to 3.6 V	11.40	12.60	MHz
16 MHz calibration value	$f_{CAL(16\ MHz)}$	BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz, Gating time: 2 ms	-40°C to 105°C	3 V to 3.6 V	15.00	17.00	MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	T_A	V_{CC}	Limits Min	Limits Max	Unit
Wake up from lower power modes (LPM3/LPM4)							
DCO clock wake up time from LPM3/LPM4 21/	$t_{DCO,LPM3/4}$	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz	-40°C to 105°C	2.2 V/ 3 V		2	µs
		BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz		2.2 V/ 3 V		1.5	
		BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz		2.2 V/ 3 V		1	
		BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz		3 V		1	
CPU wake-up time from LPM3/LPM4 22/	$t_{CPU,LPM3/4}$		-40°C to 105°C		$1/f_{MCLK} + t_{Clock,LPM3/4}$ TYP		
DCO with external resistor R_{OSC} 23/							
DCO output frequency with R_{OSC}	$f_{DCO,ROSC}$	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	25°C	2.2 V	1.8 TYP		MHz
				3 V	1.95 TYP		
Temperature drift	D_t	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	-40°C to 105°C	2.2 V/ 3 V	±0.1 TYP		%/°C
Drift with V_{CC}	D_V	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	-40°C to 105°C	2.2 V/ 3 V	10 TYP		%/V
Crystal Oscillator, LFXT1, low frequency modes 24/							
LFXT1 oscillator crystal frequency, LF mode 0/1	$f_{LFXT1,LF}$	XTS = 0, LFXT1Sx = 0 or 1	-40°C to 105°C	1.8 V to 3.6 V	32,768 TYP		Hz
LFXT1 oscillator logic level square wave input frequency, LF mode	$f_{LFXT1,LF,logic}$	XTS = 0, LFXT1Sx = 3, XCAPx = 0	-40°C to 105°C	1.8 V to 3.6 V	10,000	50,000	Hz
Oscillation allowance for LF crystal	OA_{LF}	XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32,768 Hz, $C_{L,eff}$ = 6 pF	-40°C to 105°C		500		kΩ
		XTS = 0, LFXT1Sx = 0; $f_{LFXT1,LF}$ = 32,768 Hz, $C_{L,eff}$ = 12 pF			200		
Integrated effective load capacitance, LF mode 25/	$C_{L,eff}$	XTS = 0, XCAPx = 0	-40°C to 105°C		1 TYP		pF
		XTS = 0, XCAPx = 1			5.5 TYP		
		XTS = 0, XCAPx = 2			8.5 TYP		
		XTS = 0, XCAPx = 3			11 TYP		
LF mode duty cycle	Duty cycle	XTS = 0, measured at P1.4/ACLK, $f_{LFXT1,LF}$ = 32,768 Hz	-40°C to 105°C	2.2 V/ 3 V	30	70	%
Oscillator fault frequency, LF mode 26/	$f_{Fault,LF}$	XTS = 0, LFXT1Sx = 3, XCAPx = 0 27/	-40°C to 105°C	2.2 V/ 3 V	10	10,000	Hz

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	T_A	V_{CC}	Limits Min	Limits Max	Unit
Internal very low power, Low frequency oscillator (VLO)							
VLO frequency	f_{VLO}		-40°C to 85°C	2.2 V/ 3 V	4	20	kHz
			105°C			22	
VLO frequency temperature drift	df_{VLO}/dT	28/		2.2 V/ 3 V	0.5 TYP		%/°C
VLO frequency supply voltage drift	df_{VLO}/dV_{CC}	29/	25°C	1.8 V to 3.6 V	4 TYP		%/V
Crystal oscillator, LFXT1, high frequency modes 24/							
LFXT1 oscillator crystal frequency, HF mode 0	$f_{LFXT1,HF0}$	XTS = 1, LFXT1Sx = 0, XCAPx = 0	-40°C to 105°C	1.8 V to 3.6 V	0.4	1	MHz
LFXT1 oscillator crystal frequency, HF mode 1	$f_{LFXT1,HF1}$	XTS = 1, LFXT1Sx = 1, XCAPx = 0	-40°C to 105°C	1.8 V to 3.6 V	1	4	MHz
LFXT1 oscillator crystal frequency, HF mode 2	$f_{LFXT1,HF2}$	XTS = 1, LFXT1Sx = 2, XCAPx = 0	-40°C to 105°C	1.8 V to 3.6 V	2	10	MHz
				2.2 V to 3.6 V	2	12	
				3 V to 3.6 V	2	16	
LFXT1 oscillator logic level square wave input frequency, HF mode	$f_{LFXT1,HF,logic}$	XTS = 1, LFXT1Sx = 3, XCAPx = 0	-40°C to 105°C	1.8 V to 3.6 V	0.4	10	MHz
				2.2 V to 3.6 V	0.4	12	
				3 V to 3.6 V	0.4	16	
Oscillation allowance for HF crystals See figure 11.	OA_{HF}	XTS = 1, XCAPx = 0, $C_{L,eff}$ = 15 pF, LFXT1Sx = 0, $f_{LFXT1,HF}$ = 1 MHz	-40°C to 105°C		2700 TYP		Ω
		XTS = 1, XCAPx = 0, $C_{L,eff}$ = 15 pF LFXT1Sx = 1, $f_{LFXT1,HF}$ = 4 MHz			800 TYP		
		XTS = 1, XCAPx = 0, $C_{L,eff}$ = 15 pF LFXT1Sx = 2, $f_{LFXT1,HF}$ = 16 MHz			300 TYP		
Integrated effective load capacitance, HF mode 25/	$C_{L,eff}$	XTS = 1, XCAPx = 0 30/	-40°C to 105°C		1 TYP		pF
HF mode duty cycle	Duty cycle	XTS = 1, XCAPx = 0, measured at P1.4/ACLK, $f_{LFXT1,HF}$ = 10 MHz	-40°C to 105°C	2.2 V/ 3 V	40	60	%
		XTS = 1, XCAPx = 0, measured at P1.4/ACLK, $f_{LFXT1,HF}$ = 16 MHz		2.2 V/ 3 V	40	60	
Oscillator fault frequency, HF mode 26/	$f_{Fault,HF}$	XTS = 1, LFXT1Sx = 3, XCAPx = 0 27/	-40°C to 105°C	2.2 V/ 3 V	30	300	kHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	V_{CC}	Limits		Unit
				Min	Max	
XT2 oscillator crystal frequency, mode 0	f_{XT2}	XT2Sx = 0	1.8 V to 3.6 V	0.4	1	MHz
XT2 oscillator crystal frequency, mode 1	f_{XT2}	XT2Sx = 1	1.8 V to 3.6 V	1	4	MHz
XT2 oscillator crystal frequency, mode 2	f_{XT2}	XT2Sx = 2	1.8 V to 3.6 V	2	10	MHz
			2.2 V to 3.6 V	2	12	
			3 V to 3.6 V	2	16	
XT2 oscillator logic level square wave input frequency	f_{XT2}	XT2Sx = 3	1.8 V to 3.6 V	0.4	10	MHz
			2.2 V to 3.6 V	0.4	12	
			3 V to 3.6 V	0.4	16	
Oscillation allowance See figure 12.	OA	XT2Sx = 0, f_{XT2} = 1 MHz, $C_{L,eff}$ = 15 pF		2700 TYP		Ω
		XT2Sx = 1, f_{XT2} = 4 MHz, $C_{L,eff}$ = 15 pF		800 TYP		
		XT2Sx = 2, f_{XT2} = 16 MHz, $C_{L,eff}$ = 15 pF		300 TYP		
Integrated effective load capacitance, HF mode 25/	$C_{L,eff}$	30/		1 TYP		pF
HF mode duty cycle	Duty cycle	XTS = 1, XCAPx = 0, measured at P1.4/ACLK, $f_{LFXT1,HF}$ = 10 MHz	2.2 V/3 V	40	60	%
		XTS = 1, XCAPx = 0, measured at P1.4/ACLK, $f_{LFXT1,HF}$ = 16 MHz	2.2 V/3 V	40	60	
Oscillator fault frequency, HF mode 31/	$f_{Fault,HF}$	XTS = 1, LFXT1Sx = 3, XCAPx = 0 32/	2.2 V/3 V	30	300	kHz
Timer_A						
Timer_A clock frequency	f_{TA}	Internal: SMCLK, ACLK, External: TACLK, INCLK, Duty cycle = 50% ±10%	2.2 V		10	MHz
			3 V		16	
Timer_A, capture timing	$f_{TA,cap}$	TA0, TA1, TA2	2.2 V/3 V	20		ns
Timer_B						
Timer_B clock frequency	f_{TB}	Internal: SMCLK, ACLK, External: TBCLK, Duty cycle = 50% ±10%	2.2 V		10	MHz
			3 V		16	
Timer_B, capture timing	$f_{TB,cap}$	TB0, TB1, TB2	2.2 V/3 V	20		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ -55°C ≤ T_A ≤ 125°C unless otherwise specified	V_{CC}	Limits Min	Limits Max	Unit
USCI (UART mode)						
USCI input clock frequency	f_{USCI}	Internal: SMCLK, ACLK, External: TBCLK, Duty cycle = 50% ±10%			f_{SYSTEM}	MHz
BITCLK clock frequency (equals baud rate in MBaud)	f_{BITCLK}		2.2 V/3 V		1	
UART receive deglitch time 33/	t_{ζ}		2.2 V	50	600	ns
			3 V	50	600	
USCI (SPI Master mode) See figure 13						
USCI input clock frequency		SMCLK, ACLK, Duty cycle = 50% ±10%			f_{SYSTEM}	MHz
SOMI input data setup time	$t_{SU,MI}$		2.2 V	110		ns
			3 V	75		
SOMI input data hold time	$t_{HD,MI}$		2.2 V	0		
			3 V	0		
SIMO output data valid	$t_{VALID,MO}$	UCLK edge to SIMO valid, C_L = 20 pF	2.2 V		30	
			3 V		20	
USCI (SPI Slave mode) See figure 14						
STE lead time, STE low to clock	$t_{STE,LEAD}$		2.2 V/3 V	50 TYP		ns
STE lag time, last clock to STE high	$t_{STE,LAG}$		2.2 V/3 V	10		
STE access time, STE low to SOMI data out	$t_{STE,ACC}$		2.2 V/3 V	50 TYP		
STE disable time, STE high to SOMI high impedance	$t_{STE,DIS}$		2.2 V/3 V	50 TYP		
SIMO input data setup time	$t_{SU,SI}$		2.2 V	20		
			3 V	15		
SIMO input data hold time	$t_{HD,SI}$		2.2 V	10		
			3 V	10		
SOMI output data valid	$t_{VALID,SO}$	UCLK edge to SOMI valid, C_L = 20 pF	2.2 V		110	
			3 V		75	
USCI (I2C mode) See figure 15						
USCI clock frequency	f_{USCI}	Internal: SMCLK, ACLK, External: UCLK, Duty cycle = 50% ±10%		$f_{SYSTEM\ TYP}$		MHz
SCL clock frequency	f_{SCL}		2.2 V/3 V	0	400	µs
Hold time (repeated) START	$t_{HD,STA}$	f_{SCL} ≤ 100 kHz	2.2 V/3 V	4.0		
		f_{SCL} > 100 kHz		0.6		
Setup time for a repeated START	$t_{SU,STA}$	f_{SCL} ≤ 100 kHz	2.2 V/3 V	4.7		
		f_{SCL} > 100 kHz		0.6		
Data hold time	$t_{HD,DAT}$		2.2 V/3 V	0		ns
Data setup time	$t_{SU,DAT}$		2.2 V/3 V	250		
Setup time for STOP	$t_{SU,STO}$		2.2 V/3 V	4.0		µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	V_{CC}	Limits		Unit
				Min	Max	
USCI (I2C mode) - Continued						
Pulse width of spikes suppressed by input filter	t_{SP}		2.2 V	50	600	ns
			3 V	50	600	
Comparator_A+ 36/						
	$I_{(DD)}$	CAON = 1, CARSEL = 0, CAREF = 0	2.2 V		40	µA
			3 V		60	
	$I_{(Refladder/Refdiode)}$	CAON = 1, CARSEL = 0, CAREF = 1/2/3, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V		50	µA
			3 V		71	
Common mode input voltage	$V_{(IC)}$	CAON = 1	2.2 V/3 V	0	V_{CC} - 1	V
$\frac{\text{Voltage at } 0.25\ V_{CC} \text{ node}}{V_{CC}}$	$V_{(Ref025)}$	PCA0 = 1, CARSEL = 1, CAREF = 1, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V/3 V	0.23	0.25	V
$\frac{\text{Voltage at } 0.50\ V_{CC} \text{ node}}{V_{CC}}$	$V_{(Ref050)}$	PCA0 = 1, CARSEL = 1, CAREF = 2, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V/3 V	0.47	0.5	V
See figure 17	$V_{(RefVT)}$	PCA0 = 1, CARSEL = 1, CAREF = 3, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2, T_A = 85°C	2.2 V	390	540	mV
			3 V	400	550	
Offset voltage	$V_{(offset)}$	37/	2.2 V/3 V	-30	30	mV
Input hysteresis	V_{hys}	CAON = 1	2.2 V/3 V	0	1.4	mV
Response time, low to high and high to low 38/	$t_{(response)}$	T_A = 25°C, Overdrive 10 mV, Without filter; CAF = 0	2.2 V	80	300	ns
			3 V	70	240	
		T_A = 25°C, Overdrive 10 mV, With filter; CAF = 1	2.2 V	1.4	2.8	µs
			3 V	0.9	2.2	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified		V_{CC}	Limits Min	Limits Max	Unit
12 bit ADC, Power supply and input range conditions 39/							
Analog supply voltage	AVCC	AV_{CC} and DV_{CC} are connected together, AV_{SS} and DV_{SS} are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V			2.2	3.6	V
Analog input voltage 40/	$V_{(P6.x/AX)}$	All P6.0/A0 to P6.7/A7 terminals. Analog inputs selected in ADC12MCTLx register and P6Sel.x = 1, $0 \le x \le 7$, $V_{(AVSS)} \le V_{P6.x/Ax} \le V_{(AVCC)}$			0	V_{AVCC}	V
Operating supply current into AV_{CC} terminal 41/	I_{ADC12}	$f_{ADC12CLK}$ = 5 MHz, ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0		2.2 V		0.8	mA
				3 V		1.0	
Operating supply current into AV_{CC} terminal 42/	I_{REF+}	$f_{ADC12CLK}$ = 5 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 1		3 V		0.7	mA
		$f_{ADC12CLK}$ = 5 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 0		2.2 V		0.7	
				3 V		0.7	
Input capacitance	C_I 43/	Only one terminal can be selected at one time, P6.x/Ax		2.2 V		40	pF
Input MUX ON resistance	R_I 43/	$0 \le V_{Ax} \le V_{AVCC}$		3 V		2000	Ω
12 bit ADC external reference 44/							
Positive external reference voltage input	V_{eREF+}	$V_{eREF+} > V_{REF-}/V_{eREF-}$ 45/			1.4	V_{AVCC}	V
Negative external reference voltage input	V_{REF-}/V_{eREF-}	$V_{eREF+} > V_{REF-}/V_{eREF-}$ 46/			0	1.2	V
Differential external reference voltage input	$(V_{eREF+} - V_{REF-}/V_{eREF-})$	$V_{eREF+} > V_{REF-}/V_{eREF-}$ 47/			1.4	V_{AVCC}	V
Static input current	I_{VeREF+}	$0 \text{ V} \le V_{eREF+} \le V_{AVCC}$		2.2 V/3 V		±1	µA
Static input current	$I_{VREF-/VeREF-}$	$0 \text{ V} \le V_{eREF+} \le V_{AVCC}$		2.2 V/3 V		±1	µA
12 bit ADC built-in reference							
Positive built-in reference voltage output	V_{REF+}	REF2_5V = 1 (2.5 V) $I_{VREF+}max \le I_{VREF+} \le I_{VREF+}min$	T_A = -40°C to 85°C	3 V	2.4	2.6	V
			T_A = 105°C		2.37	2.64	
		REF1_5V = 1 (2.5 V) $I_{VREF+}max \le I_{VREF+} \le I_{VREF+}min$	T_A = -40°C to 85°C	2.2 V/3 V	1.44	1.56	
			T_A = 105°C		1.42	1.57	
AV_{CC} minimum voltage, positive built-in reference active	$AV_{CC(min)}$	REF2_5V = 0 $I_{VREF+}max \le I_{VREF+} \le I_{VREF+}min$			2.2		V
		REF2_5V = 1 $-0.5 \text{ mA} \le I_{VREF+} \le I_{VREF+}min$			2.8		
		REF2_5V = 1 $-1 \text{ mA} \le I_{VREF+} \le I_{VREF+}min$			2.9		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	V_{CC}	Limits		Unit
				Min	Max	
12 bit ADC built-in reference - Continued						
Load current out of V_{REF+} terminal	$I_{(VREF)+}$ 48/		2.2 V	0.01	-0.5	mA
			3 V	0.01	-1	
Load current regulation, V_{REF+} terminal	$I_{L(VREF)+}$ 43/	I_{VREF+} = 500 µA +/-100 µA, Analog input voltage ~0.75 V, REF2_5V = 0	2.2 V		±2	LSB
			3 V		±2	
		I_{VREF+} = 500 µA ±100 µA, Analog input voltage ~1.25 V, REF2_5V = 1	3 V		±2	
Load current regulation V_{REF+} terminal	$I_{DL(VREF)+}$ 43/	I_{VREF+} = 100 µA → 900 µA, C_{VREF+} = 5 µF, at ~0.5 V_{REF+}, Error of conversion result ≤ 1 LSB	3 V		20	ns
Capacitance at pin V_{REF+} 49/	C_{VREF+}	REFON = 1, 0 mA ≤ I_{VREF+} ≤I_{VREF+}max	2.2 V/3 V	5		µF
Temperature coefficient of built-in reference	T_{REF+} 48/	I_{VREF+} is a constant in the range of 0 mA ≤ I_{VREF+} ≤ 1 mA	2.2 V/3 V		±100	ppm/°C
Settle time of internal reference voltage (See figure 19 and 50/)	t_{REFON} 48/	I_{VREF+} = 0.5 mA, C_{VREF+} = 10 µF, V_{REF+} = 1.5 V, V_{AVCC} = 2.2 V			17	ms
12 bit ADC timing parameters						
	$f_{ADC12CLK}$	For specified performance of ADC12 linearity parameters	2.2 V/3 V	0.45	6.3	MHz
Internal ADC12 oscillator	$f_{ADC12OSC}$	ADC12DIV = 0, $f_{ADC12CLK}$ = $f_{ADC12OSC}$	2.2 V/3 V	3.7	6.3	MHz
Conversion time	$t_{CONVERT}$	C_{VREF+} ≥ 5 µF, Internal oscillator, $f_{ADC12OSC}$ = 3.7 MHz to 6.3 MHz	2.2 V/3 V	2.06	3.51	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK or SMCLK, ADC12SSEL ≠ 0		13 x ADC12DIV x 1/$f_{ADC12CLK}$		
Turn-on setting time of the ADC	$t_{ADC12ON}$	43/ 51/			100	ns
Sampling time	t_{Sample} 43/	R_S = 400 Ω, R_I = 1000 Ω, C_I = 30 pF, τ = [R_S + R_I] x C_I; 52/	3 V	1220		ns
			2.2 V	1400		
12 bit ADC linearity parameters						
Integral linearity error	E_I	1.4 V ≤ (V_{eREF+} - V_{REF-}/V_{eREF-})min ≤ 1.6 V	2.2 V/3 V		±2	LSB
		1.6 V ≤ (V_{eREF+} - V_{REF-}/V_{eREF-})min ≤ V_{AVCC}			±1.7	
Differential linearity error	E_D	(V_{eREF+} - V_{REF-}/V_{eREF-})$_{min}$ ≤ (V_{eREF+} - V_{REF-}/V_{eREF-}), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±1	
Offset error	E_O	(V_{eREF+} - V_{REF-}/V_{eREF-})$_{min}$ ≤ (V_{eREF+} - V_{REF-}/V_{eREF-}), Internal impedance of sopurce R_S < 100 Ω, C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±4	
Gain error	E_G	(V_{eREF+} - V_{REF-}/V_{eREF-})$_{min}$ ≤ (V_{eREF+} - V_{REF-}/V_{eREF-}), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±2	
Total unadjusted error	E_T	(V_{eREF+} - V_{REF-}/V_{eREF-})$_{min}$ ≤ (V_{eREF+} - V_{REF-}/V_{eREF-}), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	V_{CC}	Limits Min	Limits Max	Unit
12 bit ADC temperature sensor and built-in V_{MID}						
Operating supply current into AV_{CC} terminal 53/	I_{SENSOR}	REFON = 0, INCH = 0Ah, ADC12ON = 1, T_A = 25°C	2.2 V		120	µA
			3 V		160	
54/	V_{SENSOR} 48/	ADC12ON = 1, INCH = 0Ah, T_A = 25°C	2.2 V	986 TYP		mV
			3 V	986 TYP		
	TC_{SENSOR} 48/	ADC12ON = 1, INCH = 0Ah	2.2 V	3.55 TYP		mV/°C
			3 V	3.55 TYP		
Sample time required if channel 10 is selected 55/	$t_{SENSOR(sample)}$ 48/	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	30		µs
			3 V	30		
Current into divider at channel 11 56/	I_{VMID}	ADC12ON = 1, INCH = 0Bh	2.2 V		NA	µA
			3 V		NA	
AVCC divider at channel 11	V_{MID}	ADC12ON = 1, INCH = 0Bh, V_{MID} is ~0.5 x V_{AVCC}	2.2 V		1.1±0.04	V
			3 V		1.5±0.04	
Sample time required if channel 11 is selected 57/	$t_{VMID(sample)}$	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V	1400		ns
			3 V	1200		
12 bit DAC supply specifications						
Analog supply voltage	AV_{CC}	$AV_{CC} = DV_{CC}$, $AV_{SS} = DV_{SS} = 0$		2.20	3.60	V
Supply current, single DAC channel 58/ 59/	I_{DD}	DAC12AMPx = 2, DAC12IR = 0 DAC12_xDAT = 0x0800; T_A = -40°C to 85°C	2.2 V/3 V		110	µA
		DAC12AMPx = 2, DAC12IR = 0 DAC12_xDAT = 0x0800; T_A = 105°C	2.2 V/3 V		150	
		DAC12AMPx = 2, DAC12IR = 1 DAC12_xDAT = 0x0800, $V_{eREF+} = V_{REF+} = AV_{CC}$	2.2 V/3 V		130	
		DAC12AMPx = 5, DAC12IR = 1 DAC12_xDAT = 0x0800, $V_{eREF+} = V_{REF+} = AV_{CC}$	2.2 V/3 V		440	
		DAC12AMPx = 7, DAC12IR = 1 DAC12_xDAT = 0x0800, $V_{eREF+} = V_{REF+} = AV_{CC}$	2.2 V/3 V		1500	
Power supply rejection ratio 60/ 61/	PSRR	DAC12_xDAT = 800h, V_{REF} = 1.5 V, ΔAV_{CC} = 100 mV	2.2 V	70 TYP		dB
		DAC12_xDAT = 800h, V_{REF} = 1.5 V or 2.5 V, ΔAV_{CC} = 100 mV	3 V			

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	V_{CC}	Limits		Unit
				Min	Max	
12 bit DAC linearity specifications (See figure 20)						
Resolution		12 bit monotonic				bits
Integral nonlinearity 62/	INL	V_{REF} =1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V		±8.0	LSB
		V_{REF} =2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V			
Differential nonlinearity 62/	DNL	V_{REF} =1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V		±1.0	LSB
		V_{REF} =2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V			
Offset voltage without calibration 62/ 63/	E_O	V_{REF} =1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V		±21	mV
		V_{REF} =2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V			
Offset voltage with calibration 62/ 63/		V_{REF} =1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V		±2.5	
		V_{REF} =2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V			
Offset error temperature coefficient	$d_{E(O)}/d_T$		2.2 V/3 V	30 TYP		µV/C
Gain error	E_G	V_{REF} =1.5 V	2.2 V		±3.5	% FSR
		V_{REF} =2.5 V	3 V			
Gain temperature coefficient 62/	$d_{E(G)}/d_T$		2.2 V/3 V	10 TYP		ppm of FSR/°C
Time for offset calibration 64/	t_{Offset_Cal}	DAC12AMPx = 2	2.2 V/3 V		100	ms
		DAC12AMPx = 3, 5			32	
		DAC12AMPx = 4, 6, 7			6	
12 bit DAC output specifications						
Output voltage range 65/ See figure 21	V_O	No load, V_{eREF+} = AV_{CC}, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7	2.2 V/3 V	0	0.005	V
		No load, V_{eREF+} = AV_{CC}, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7		AV_{CC}-0.05	AV_{CC}	
		R_{Load} = 3 kΩ, V_{eREF+} = AV_{CC}, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7		0	0.1	
		R_{Load} = 3 kΩ, V_{eREF+} = AV_{CC}, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7		AV_{CC}-0.13	AV_{CC}	
Max DAC12 load capacitance	$C_{L(DAC12)}$		2.2 V/3 V		100	pF
Max DAC12 load current	$I_{L(DAC12)}$		2.2 V	-0.5	+0.5	mA
			3 V	-1.0	+1.0	
Output resistance See figure 21	$R_{O/P(DAC12)}$	R_{Load} = 3 kΩ, $V_{O/P(DAC12)}$ = AV_{CC}, DAC12AMPx = 7, DAC12_xDAT = 0h	2.2 V/3 V		250	Ω
		R_{Load} = 3 kΩ, $V_{O/P(DAC12)}$ = AV_{CC}, DAC12AMPx = 7, DAC12_xDAT = 0FFFh			250	
		R_{Load} = 3 kΩ, DAC12AMPx = 7, 0.3 V ≤$V_{O/P(DAC12)}$ ≤ AV_{CC} – 0.3 V			4	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified		V_{CC}	Limits Min	Limits Max	Unit
12 bit DAC reference input specifications							
Reference input voltage range	V_{eREF+}	DAC12IR = 0, 66/ 67/		2.2V/3 V		AV_{CC} + 0.2	V
		DAC12IR = 1, 68/ 69/				AV_{CC} + 0.2	
Reference input resistance	$Ri_{(VREF+)}$, $Ri_{(VeREF+)}$	DAC12_0 IR = DAC1_21 IR = 0		2.2V/3 V	20		MΩ
		DAC12_0 IR =1, DAC1_21 IR = 0			40	56	kΩ
		DAC12_0 IR =0, DAC1_21 IR = 1					
		DAC12_0 IR = DAC1_21 IR = 1, DAC12_0 SREFx = DAC12_1 SREFx 69/			20	28	
12 bit DAC dynamic specifications, Vref = V_{CC}, DAC12IR = 1 (See figure 22)							
DAC12 on time	t_{ON}	DAC12_xDAT = 800h, $Error_{V(O)}$ < ±0.5 LSB See figure 22 71/	DAC12AMPx = 0 → {2, 3, 4}	2.2V/3 V		120	µs
			DAC12AMPx = 0 → {5, 6}			30	
			DAC12AMPx = 0 → 7			12	
Setting time, full scale	$t_{S(FS)}$	DAC12_xDAT = 80h → F7Fh → 80h	DAC12AMPx = 2	2.2V/3 V		200	µs
			DAC12AMPx = 3, 5			80	
			DAC12AMPx = 4, 6, 7			30	
Setting time, code to code	$t_{S(C-C)}$	DAC12_xDAT = 3F8h → 408h → 3F8h BF8h → C08h → BF8h	DAC12AMPx = 2	2.2V/3 V	5 TYP		µs
			DAC12AMPx = 3, 5		2 TYP		
			DAC12AMPx = 4, 6, 7		1 TYP		
Slew rate	SR	DAC12_xDAT = 80h → F7Fh → 80h	DAC12AMPx = 2	2.2V/3 V	0.05		V/µs
			DAC12AMPx = 3, 5		0.35		
			DAC12AMPx = 4, 6, 7		1.5		
Glitch energy, full scale		DAC12_xDAT = 3F8h → 408h → 3F8h BF8h → C08h → BF8h	DAC12AMPx = 2	2.2V/3 V	600 TYP		nV-s
			DAC12AMPx = 3, 5		150 TYP		
			DAC12AMPx = 4, 6, 7		30 TYP		
12 bit DAC dynamic specifications (continued) (TA = 25°C, unless otherwise noted)							
3-dB bandwidth, V_{DC} = 1.5 V, V_{AC} = 0.1 V_{PP} See figure 23	BW_{-3dB}	DAC12AMPx = {2, 3, 4}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h		2.2V/3 V	40		kHz
		DAC12AMPx = {5, 6}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h			180		
		DAC12AMPx = 7, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h			550		
Channel-to-channel crosstalk See figure 24 73/		DAC12_0DAT = 80h, No load, DAC12_1DAT = 80h < - >F7Fh, R_{Load} = 3 kΩ, f_{DAC12_1OUT} = 10 kHz, Duty cycle = 50%		2.2V/3 V	-80 TYP		dB
		DAC12_0DAT = 80h, No load, DAC12_1DAT = 80h < - >F7Fh, R_{Load} = 3 kΩ, f_{DAC12_1OUT} = 10 kHz, Duty cycle = 50%			-80 TYP		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	V_{CC}	Limits		Unit
				Min	Max	
Flash memory						
Program and erase supply voltage	$V_{CC(PGM/ERASE)}$			2.2	3.6	V
Flash timing generator frequency	f_{FTG}			257	476	kHz
Supply current from DV_{CC} during program	I_{PGM}		2.2 V/3.6 V		5	mA
Supply current from DV_{CC} during erase	I_{ERASE}		2.2 V/3.6 V		7	mA
Cumulative program time	t_{CPT}	74/	2.2 V/3.6 V		10	ms
Cumulative mass erase time	$t_{CMErase}$	75/	2.2 V/3.6 V	200		ms
Program/Erase endurance				10^4		cycles
Data retention duration	$t_{Retention}$	T_J = 25°C		100		years
Word or byte program time	t_{Word}	76/		35 TYP		t_{FTG}
Block program time for first byte or word	$t_{Block, 0}$	76/		30 TYP		
Block program time for each additional byte or word	$t_{Block, 1-63}$	76/		21 TYP		
Block program end-sequence wait time	$t_{Block, End}$	76/		6 TYP		
Mass erase time 77/	$t_{Mass\ Erase}$	76/		10593 TYP		
Segment erase time	$t_{Seg\ Erase}$	76/		4819 TYP		
RAM						
78/	VRAMh	CPU halted		1.6		V
JTAG interface						
TCK input frequency	f_{TCK}	79/	2.2 V	0	5	MHz
			3 V	0	10	
Internal pullup resistance on TMS, TCK, TDI/TCLK	$R_{Internal}$	80/	2.2 V/3 V	25	90	kΩ
JTAG fuse 81/						
Supply voltage during fuse blow condition	$V_{CC(FB)}$	T_A = 25°C		2.5		V
Voltage level on TDI/TCLK for fuse blow	V_{FB}			6	7	V
Supply current into TDI/TCLK during fuse blow	I_{FB}				100	mA
Time to blow fuse	t_{FB}				1	ms

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ Over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted).
3/ All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
4/ The current are characterized micro crystal. See the manufacturer data sheet for more information.

5/ Current for brownout and WDT+ is included. The WDT+ is clocked by SMCLK.
6/ Current for brownout and WDT+ is included. The WDT+ is clocked by ACLK.
7/ Current for brownout included.
8/ XIN and XT2IN in bypass mode only.
9/ The external signal sets the interrupt flag every time the minimum $t_{(int)}$ are met. It may be set with trigger signals shorter than $t_{(int)}$.
10/ The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
11/ The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.
12/ The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
13/ The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
14/ A resistive divider with 2 times 0.5 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
15/ The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.
16/ The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B_IT-)} + V_{hys(B_IT-)}$ is ≤ 1.8 V.
17/ During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B_IT-)} + V_{hys(B_IT-)}$, The default DCO settings must not be changed until $V_{CC} \geq V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency.
18/ tsettle is the setting time that the comparator o/p needs to have a stable level after VLD is switched VLD ≠ 0 to a different VLD value between 2 and 15. The overdrive is assumed to be > 50 mV.
19/ The recommended operating voltage range is limited to 3.6 V.
20/ The current consumption of the SVS module is not included in the I_{CC} current consumption data.
21/ The DCO clock wake up time is measured from the edge of an external wake up signal (e.g., port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK)
22/ Parameter applicable only if DCOCLK is used for MCLK.
23/ R_{OSC} = 100kΩ. Metal film resistor, type 0257. 0.6 watt with 1% tolerance and TK = ±50ppm/°C.
24/ To improve EMI on the LFXT1 oscillator the following guidelines should be observed:
   a. Keep as short of a trace as possible between the device and the crystal.
   b. Design a good ground plane around the oscillator pin.
   c. Prevent crosstalk from other clock or data lines into oscillator pin XIN and XOUT.
   d. Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   e. Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   f. If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between oscillator pins.
   g. Do not rout the XOUT line to the JTAG header to support the serial programming adapter as shown in other data. This signal is no longer required for the serial programming adapter.
25/ Includes parasitic bond and package capacitance (approximately 2 pF per pin). Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification on the used crystal.
26/ Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
27/ Measured with logic level input frequency, but also applies to operation with crystals.

TABLE I. Electrical performance characteristics – Continued. 1/

28/ Calculated using the box method:
I version: [MAX(-40°C to 85°C) – MIN(-40°C to 85°C)]/ MIN(-40°C to 85°C)]/[85°C – (-40°C)]
T version: [MAX(-40°C to 105°C) – MIN(-40°C to 105°C)]/ MIN(-40°C to 105°C)]/[105°C – (-40°C)]

29/ Calculated using the box method:[Max(1.8V to 3.6V) – MIN(1.8V to 3.6 V)]/MIN(1.8V to 3.6 V)/(3.6 V – 1.8 V)

30/ Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

31/ frequencies below MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag, and frequencies in between might set the flag.

32/ Measured with logic level input frequency but also applies to operation with crystals.

33/ Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that the pulses correctly recognized, their width should exceed the maximum specification of the deglitch time.

34/ $f_{UCxCLK} = \frac{1}{2t_{LO/HI}}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(USCI)} + t_{VALID,SO(slave)})$
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.

35/ $f_{UCxCLK} = \frac{1}{2t_{LO/HI}}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$
For the master parameters $t_{SU,SI(Master)}$ and $t_{VALID,SO(Master)}$, see the SPI parameters of the attached master.

36/ The leakage current for the Comparator_A+ terminals is identical to $I_{lkg(Px.x)}$ specification.

37/ The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A+ inputs on successive measurements. The two successive measurements are then summed together.

38/ The response time is measured at P2.2/CAOUT/TA0/CA4 with an input voltage step, with Comparator_A+ already enabled (CAON = 1). If CAON is set at the same time, a setting time of up to 300 ns is added to the response time.

39/ The leakage current is defined in the leakage current table with P6.x/Ax parameter.

40/ The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion result.

41/ The internal reference supply current is not included in current consumption parameter I_{ADC12}.

42/ The internal reference current is supplied via terminal AV_{CC}. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables the built in reference to settle before starting an A/D conversion.

43/ Limits verified by design.

44/ The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog source impedance to allow the change to settle for 12 bit accuracy.

45/ The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.

46/ The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.

47/ The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

48/ Limits characterized.

49/ The internal buffer operational amplifier and the accuracy specifications require an external capacitor. All INL and DNL tests use two capacitors between pins V_{REF+} and AV_{SS} and V_{REF-}/V_{eREF-} and AV_{SS}: 10 µF tantalum and 100 nF ceramic.

50/ The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The setting time depends on the external capacitive load.

51/ The condition is that the error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.

52/ Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB:
$t_{Sample} = \ln(2^{n+1}) \times (R_S = R_I) \times C_I + 800$ ns where n = ADC resolution = 12, R_S = external source resistance.

53/ The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON =1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is included in I_{REF+}.

54/ The temperature sensor offset can be as much as ±20°C. A single point calibration is recommended to minimize the offset error of the built-in temperature sensor.

55/ The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor on time $t_{SENSOR(on)}$.

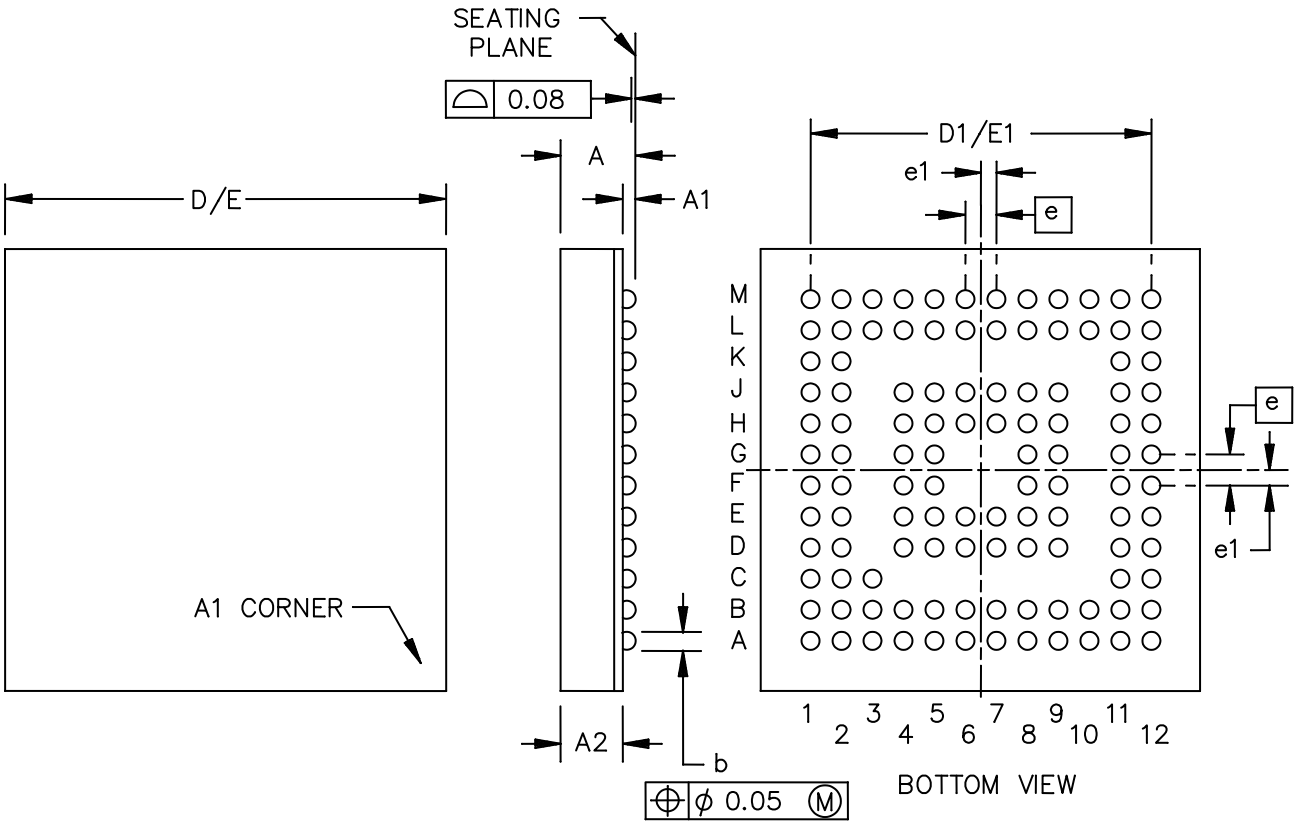
56/ No additional current is needed. The VMID is used during sample.

57/ The on time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

TABLE I. Electrical performance characteristics – Continued. 1/

58/ No load at the output pin, DAC12_0 or DAC12_1, assuming that the control bits for the shared pins are set properly.
59/ Current into reference terminals not included. If DAC12IR = 1 current flows through the input divider; see manufacturer reference for more information.
60/ PSRR = 20 x log{$\Delta AV_{CC}/\Delta V_{DAC12_xOUT}$}.
61/ V_{REF} is applied externally. The internal reference is not used.
62/ Parameters calculated from the best fit curve from 0x0A to 0xFFF. The best fit curve method is used to deliver coefficients “a” and “b” of the first order equation: y = a + bx. $V_{DAC12_xOUT} = E_O + (1 + E_G) \times (V_{eREF+}/4095) \times$ DAC12_xDAT, DAC12IR = 1.
63/ The offset calibration works on the output operation amplifier. Offset calibration is triggered setting bit DAC12CALON.
64/ The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operation is switched off with DAC12AMPx = {0, 1}. The DAC12 module should be configured prior to initiating calibration. Port activity during calibration may affect accuracy and is not recommended.
65/ Data is valid after the offset calibration of the output amplifier.
66/ For a full scale output, the reference input voltage can be as high as 1/3 of the maximum output voltage swing (AV_{CC}).
67/ The maximum voltage applied at reference input voltage terminal $V_{eREF+} = [AV_{CC} – V_{E(O)}] / [3*(1+E_G)]$.
68/ For a full scale output, the reference input voltage can be as high as of the maximum output voltage swing (AV_{CC}).
69/ The maximum voltage applied at reference input voltage terminal $V_{eREF+} = [AV_{CC} – V_{E(O)}] / (1+E_G)$.
70/ When DAC12IR = 1 and DAC12SREFx = 0 or 1 for both channels, the reference input resistive divider for each DAC are in parallel reducing the reference input resistance.
71/ RLoad and CLoad are connected to AVSS (not AVCC/2) in figure 22.
72/ Slew rate applied to output voltage step ≥ 200 mV.
73/ RLoad = 3 kΩ, CLoad = 100 pF.
74/ The cumulative program time must not be exceeded when writing to a 64 byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
75/ The mass erase duration generated by the flash timing generator is at least 11.1 ms (= 5297x1/f_{FGT}, max = 5297 x 1/476 kHz). To achieve the required cumulative mass erase time, the Flash Controller’s mass erase operation can be repeated until this time is met. A worst case minimum of 19 cycles is required.
76/ These values are hardwired into the Flash Controller’s state machine ($t_{FTG} = 1/f_{FTG}$).
77/ To erase the complete code area, the mass erase must be performed once with a dummy address in the range og the lower 64 kB flash address and once with the dummy address in the upper 64 kB flash addresses.
78/ This parameter defines the minimum supply voltage when the data in program memory RAM remain unchaged. No program execution should take place during this supply voltage condition.
79/ f_{TCK} may be restricted to meet the timing requirements of the module selected.
80/ TMS, TDI/TCLK, and TCK pullup resistor are implemented in all versions.
81/ Once the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.

Case X



Dimension					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.00	D/E	6.90	7.10
A1	0.15	0.25	e	0.50 BSC	
A2	0.71	0.77	e1	0.25 BSC	
b	0.25	0.35			

NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Falls within JEDEC MO-225.

FIGURE 1. Case outline.

Case outline X					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	DV_{CC1}	B1	P6.3/A3	C1	P6.4/A4
A2	AV_{CC}	B2	AV_{SS}	C2	P6.5/A5/DAC1
A3	DV_{SS1}	B3	AV_{SS}	C3	P6.5/A5/DAC1
A4	P6.1/A1	B4	P6.2/A2	C11	P7.4
A5	TCK	B5	$\overline{RST}$/NMI	C12	P7.3
A6	TDI/TCLK	B6	TMS		
A7	P8.7/XT2IN	B7	TDO/TDI		
A8	P8.6/XT2OUT	B8	P8.5		
A9	P8.3	B9	P8.4		
A10	P8.1	B10	P8.0		
A11	P7.7	B11	Reserved		
A12	P7.6	B12	P7.5		
D1	P6.6/A6/DAC0	E1	XIN	F1	XOUT
D2	P6.7/A7/DAC1/SVSIN	E2	V_{REF+}	F2	Ve_{REF+}/DAC0
D4	P6.0/A0	E4	Reserved	F4	Reserved
D5	Reserved	E5	Reserved	F5	Reserved
D6	Reserved	E6	Reserved	F8	Reserved
D7	Reserved	E7	Reserved	F9	Reserved
D8	Reserved	E8	Reserved	F11	P5.7/TBOUTH/SVSOUT
D9	P8.2	E9	Reserved	F12	DV_{CC2}
D11	P7.2	E11	P7.0		
D12	P7.1	E12	DV_{SS2}		

FIGURE 2. Terminal connections.

Case outline X (continued)					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
G1	V_{REF-}/Ve_{REF-}	H1	P1.1/TA0	J1	P1.3/TA2
G2	P1.0/TACLK/CAOUT	H2	P1.2/TA1	J2	P1.4/SMCLK
G4	Reserved	H4	Reserved	J4	P2.6/ADC12CLK/DMAE0/CA6
G5	Reserved	H5	Reserved	J5	Reserved
G8	Reserved	H6	Reserved	J6	Reserved
G9	Reserved	H7	Reserved	J7	Reserved
G11	P5.5/SMCLK	H8	Reserved	J8	Reserved
G12	P5.6/ACLK	H9	Reserved	J9	P4.1/TB1
		H11	P5.3/UCB1CLK/UCA1STE	J11	P5.1/UCB1SIMO/UCB1SDA
		H12	P5.4/MCLK	J12	P5.2/UCB1SIMO/UCB1SCL
K1	P1.5/TA0	L1	P1.7/TA2	M1	P2.0/ACLK/CA2
K2	P1.6/TA1	L2	Reserved	M2	P2.1/TAINCLK/CA3
K11	P4.7/TBCLK	L3	P2.3/CA0/TA1	M3	P2.2/CAOUT/TA0/CA4
K12	P5.0/UCB1STE/UCA1CLK	L4	P2.4/CA1/TA2	M4	P2.5/R_{OSC}/CA5
		L5	P2.7/TA0/CA7	M5	P3.0/UCBOSTE/UCA0CLK
		L6	P3.1/UCB0SIMO/UCB0SCL	M6	P3.2/UCB0SOMI/UCB0SCL
		L7	P3.3/UCB0CLK/UCA0STE	M7	P3.4/UCA0TXD/UCA0SIMO
		L8	P3.5/UCA0RXD/UCA0SOMI	M8	P3.6/UCA1TXD/UCA1SIMO
		L9	P3.7/UCA1RXD/UCA1SOMI	M9	P4.0/TB0
		L10	P4.3/TB3	M10	P4.2/TB2
		L11	Reserved	M11	P4.4/TB4
		L12	P4.6/TB6	M12	P4.5/TB5

FIGURE 2. Terminal connections - Continued.

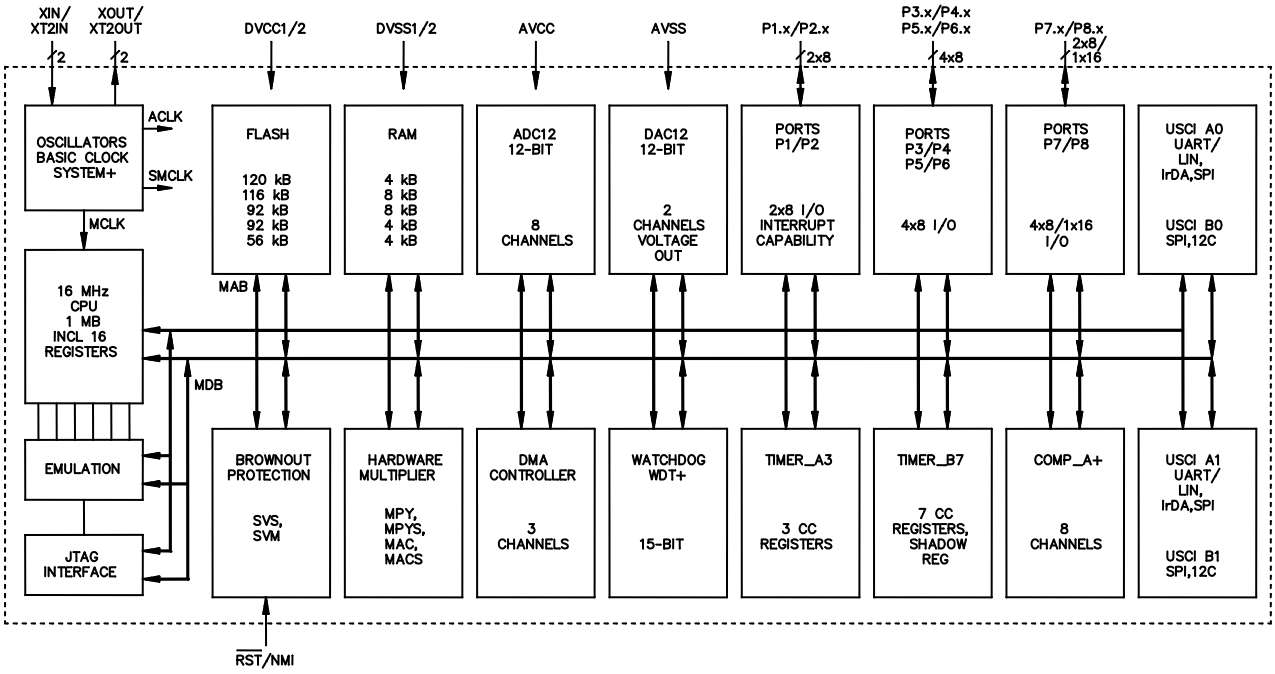
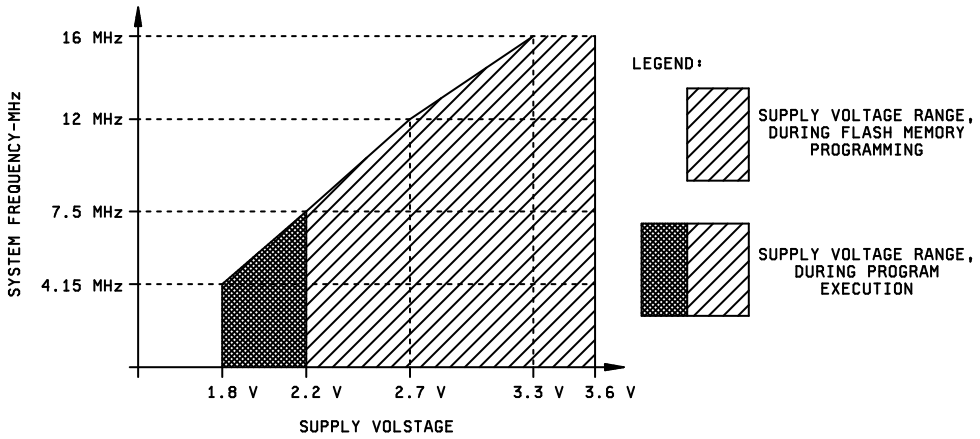
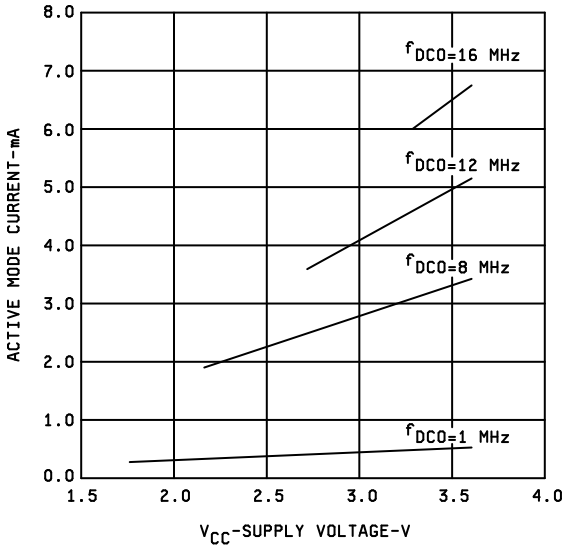


FIGURE 3. Functional block diagram.

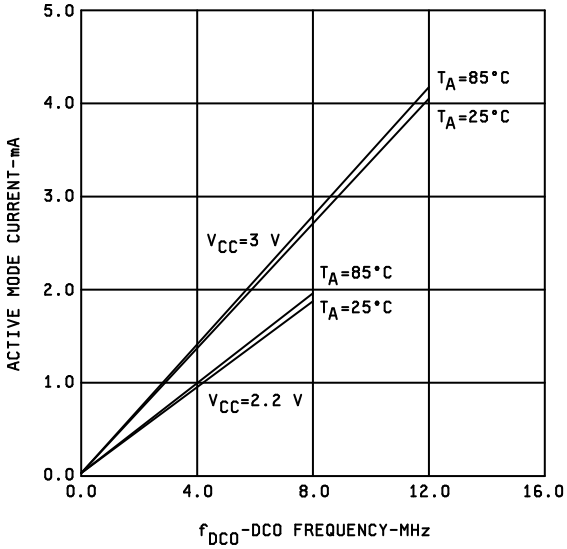


NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

FIGURE 4. Operating area.



ACTIVE-MODE CURRENT vs V_{CC}, T_A=25°C



ACTIVE-MODE CURRENT vs DCO FREQUENCY

FIGURE 5. Active mode supply current.

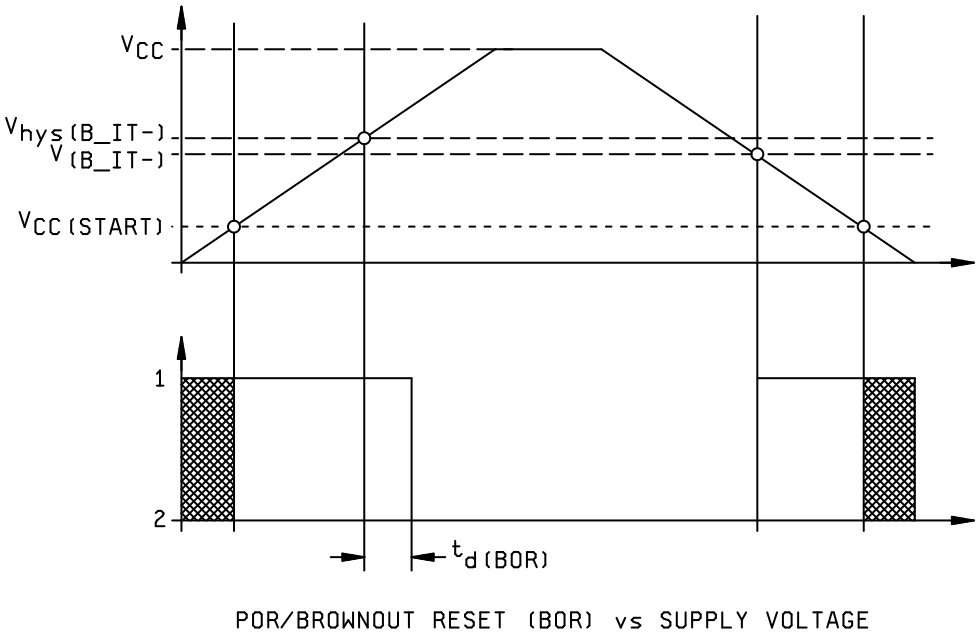
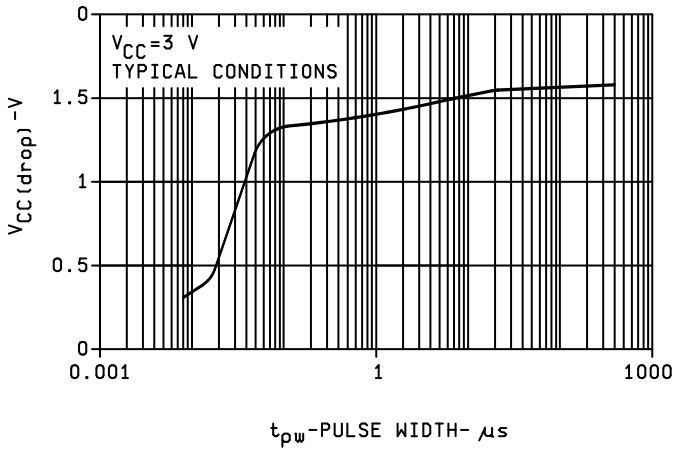
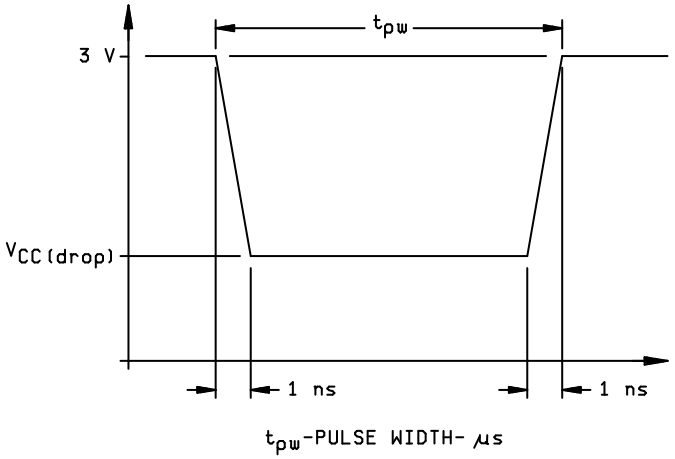


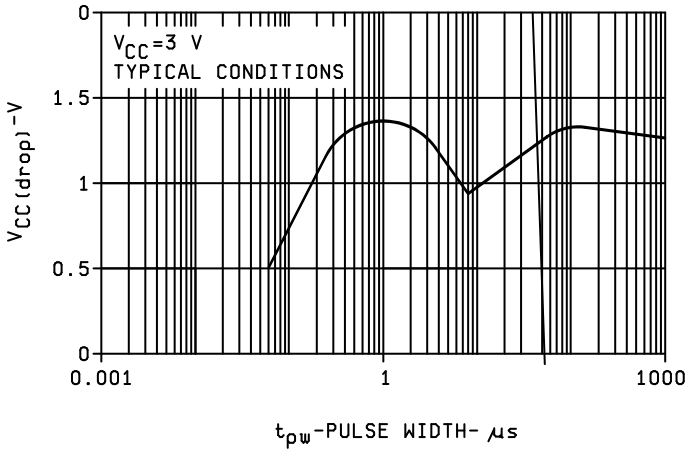
FIGURE 6. POR/Brownout reset.

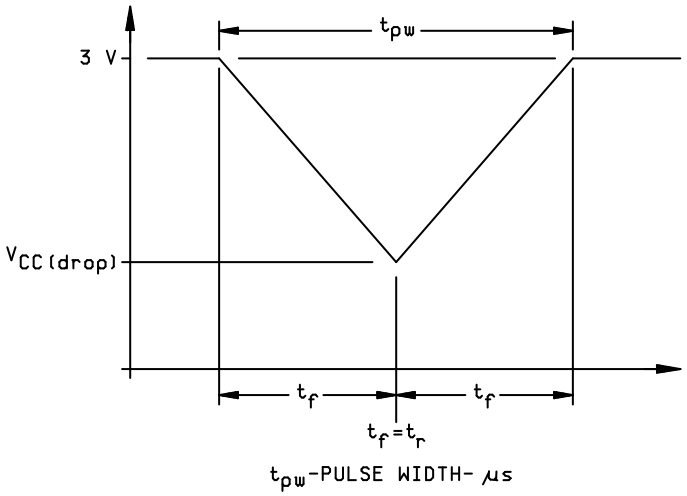




$V_{CC(drop)}$ LEVEL WITH A SQUARE VOLTAGE DROP TO GENERATE A POR/BROWNOUT SIGNAL

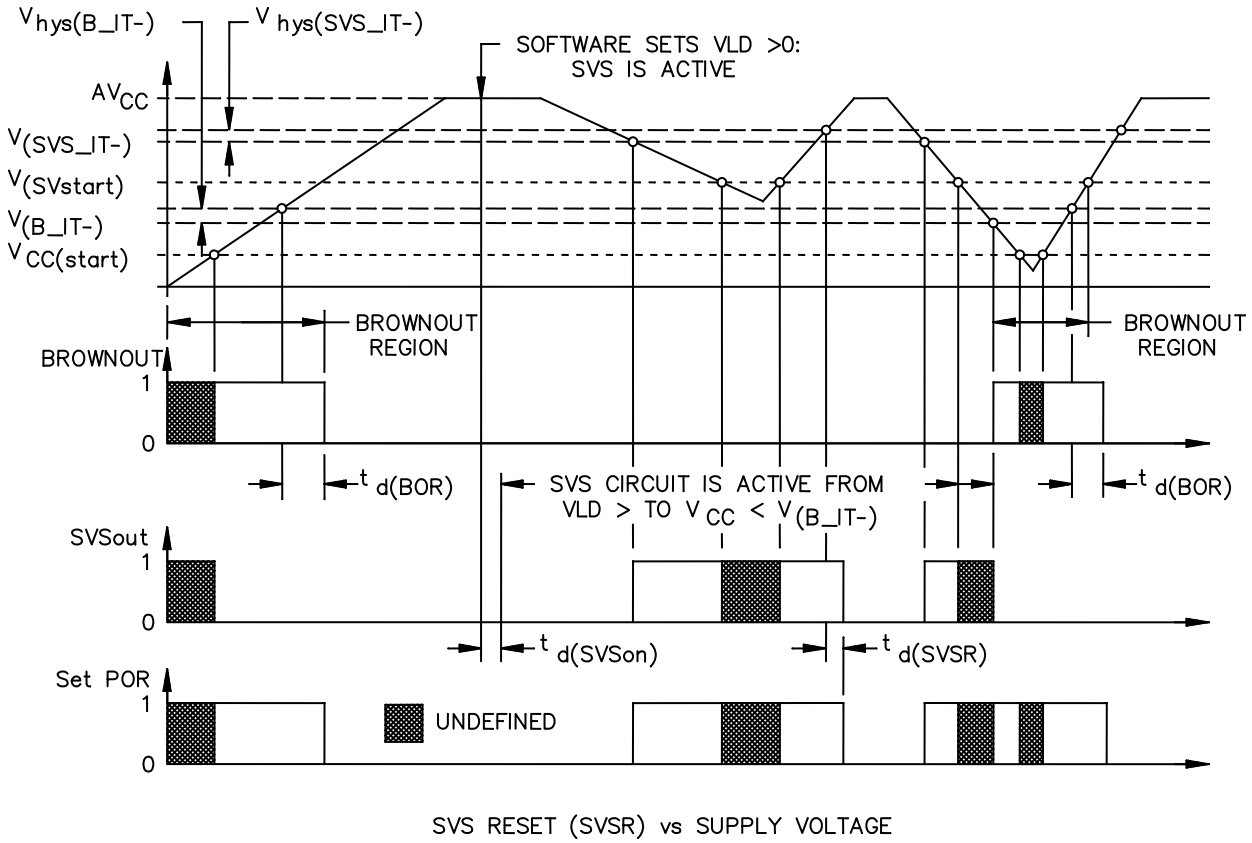
FIGURE 7. POR/Brownout reset.





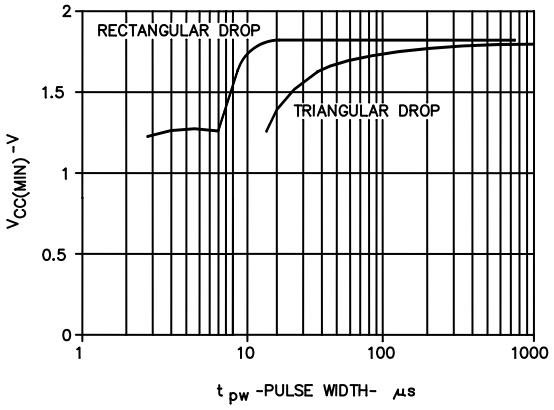
$V_{CC(drop)}$ LEVEL WITH A TRIANGLE VOLTAGE DROP TO GENERATE A POR/BROWNOUT SIGNAL

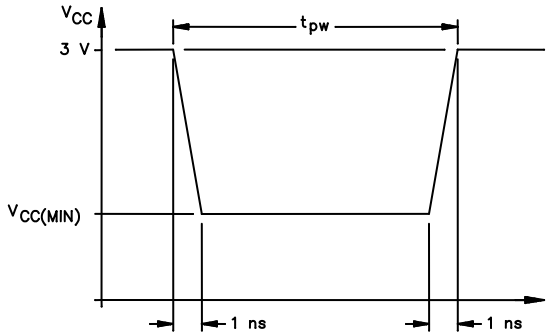
FIGURE 8. POR/Brownout reset.

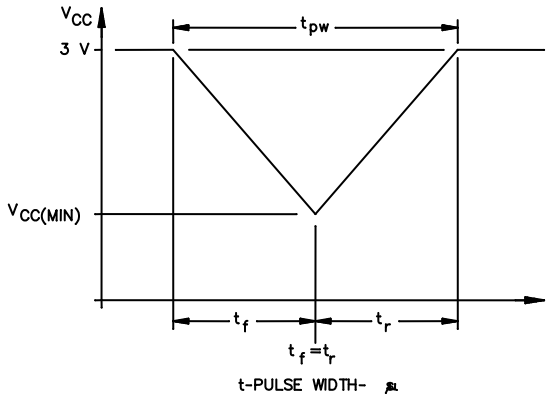


SVS RESET (SVSR) vs SUPPLY VOLTAGE

FIGURE 9. Test circuits and timing waveforms

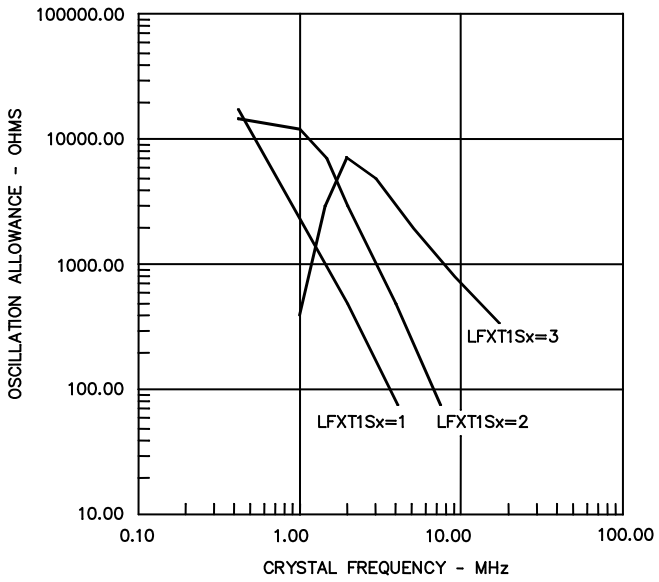




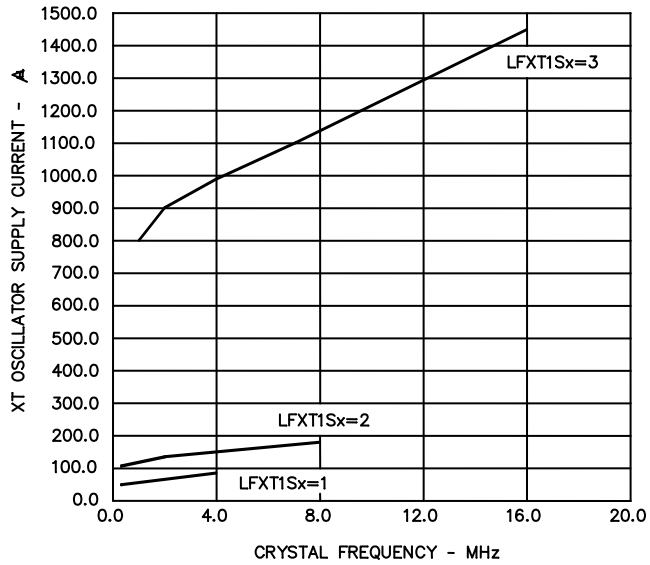


$V_{CC(MIN)}$:SQUARE VOLTAGE DROP AND TRIANGLE VOLTAGE DROP TO GENERATE AN SVS SIGNAL(VLD=1)

FIGURE 10. Test circuits and timing waveforms

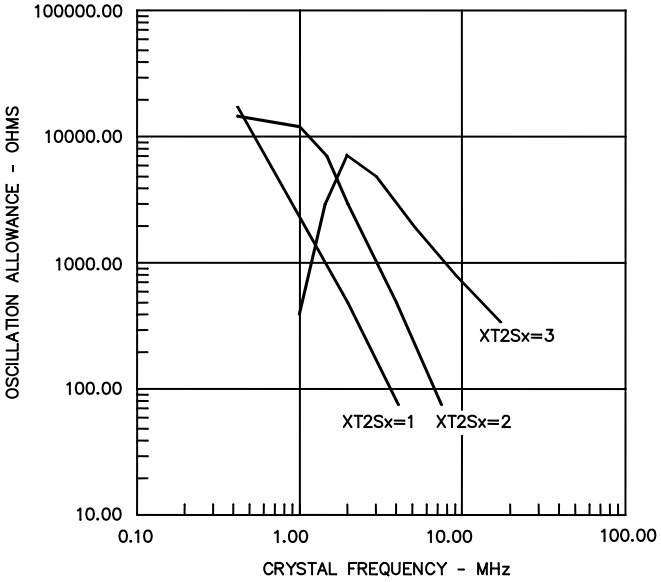


OSCILLATION ALLOWANCE vs CRYSTAL FREQUENCY,
$C_{L,eff}$ =15 pF, T_A =25°C

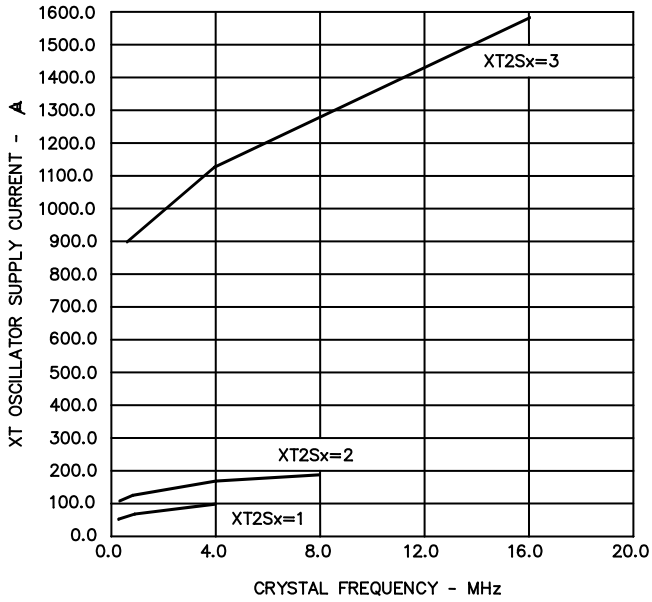


XT OSCILLATOR SUPPLY CURRENT vs CRYSTAL FREQUENCY,
$C_{L,eff}$ =15 pF T_A =25°C

FIGURE 11. Test circuits and timing waveforms

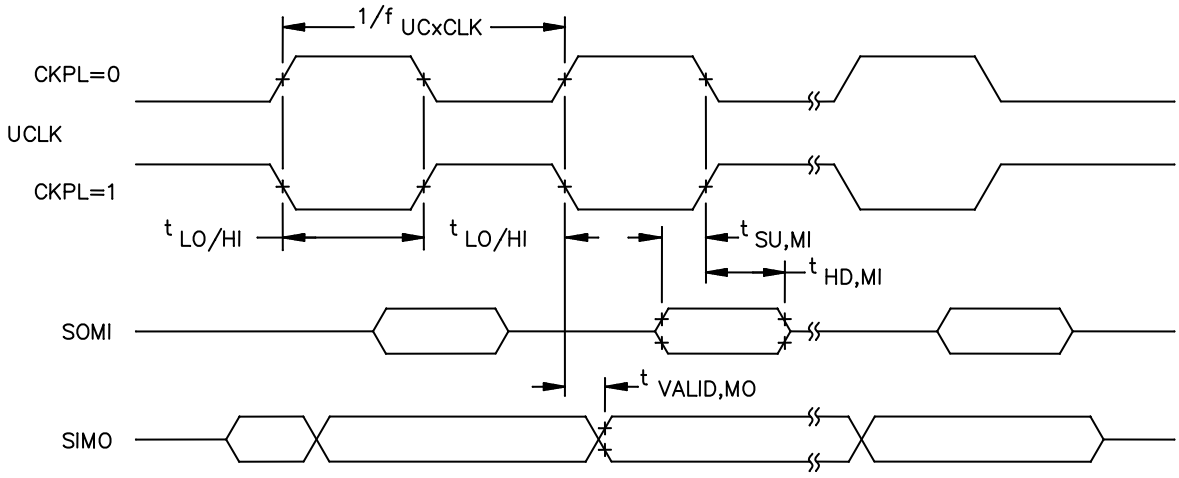


OSCILLATION ALLOWANCE vs CRYSTAL FREQUENCY, $C_{L,eff}$ =15 pF, T_A =25°C

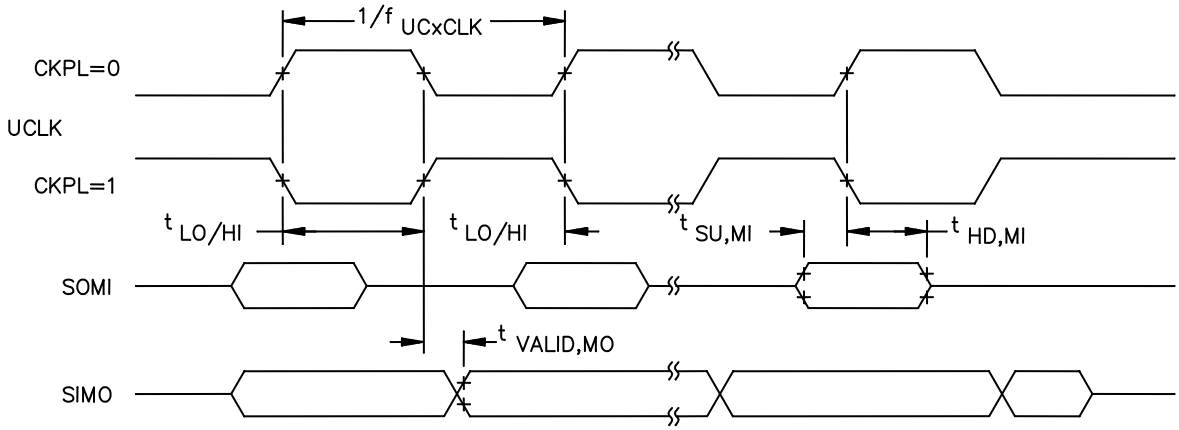


XT2 OSCILLATOR SUPPLY CURRENT vs CRYSTAL FREQUENCY, $C_{L,eff}$ =15 pF, T_A =25°C

FIGURE 12. Test circuits and timing waveforms

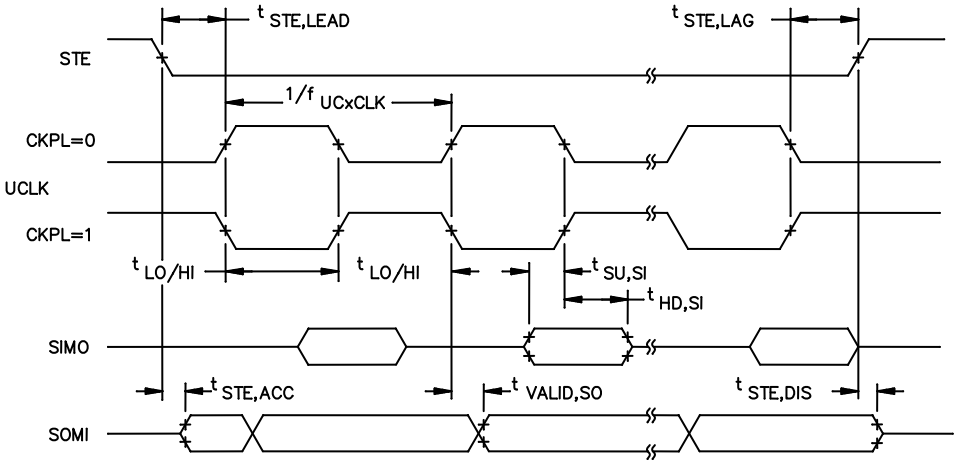


SPI SLAVE MODE, CKPH = 0

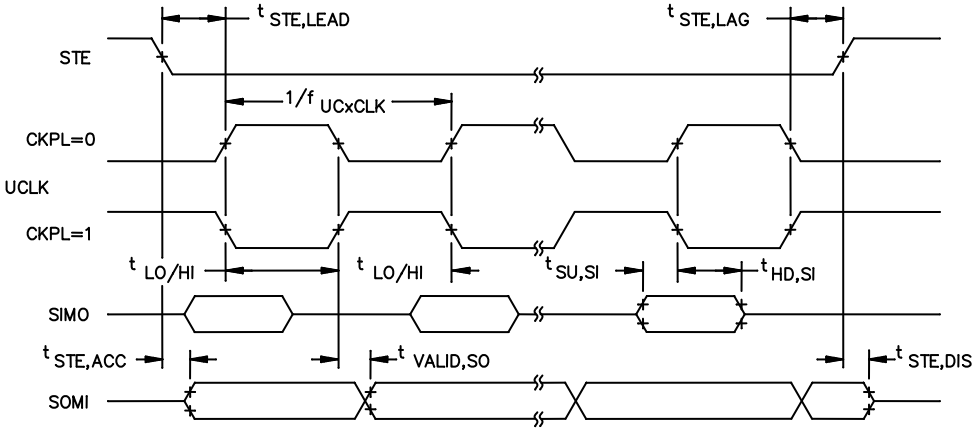


SPI SLAVE MODE, CKPH = 1

FIGURE 13. Test circuits and timing waveforms

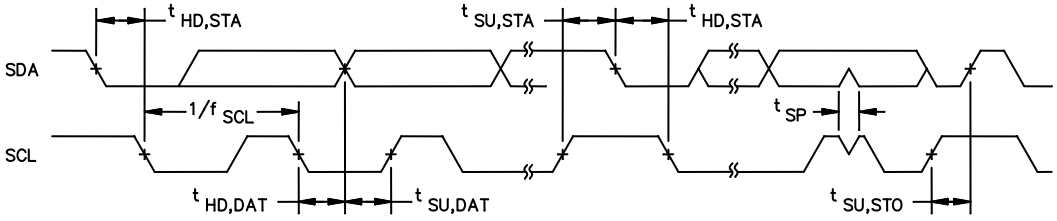


SPI SLAVE MODE, CKPH = 0



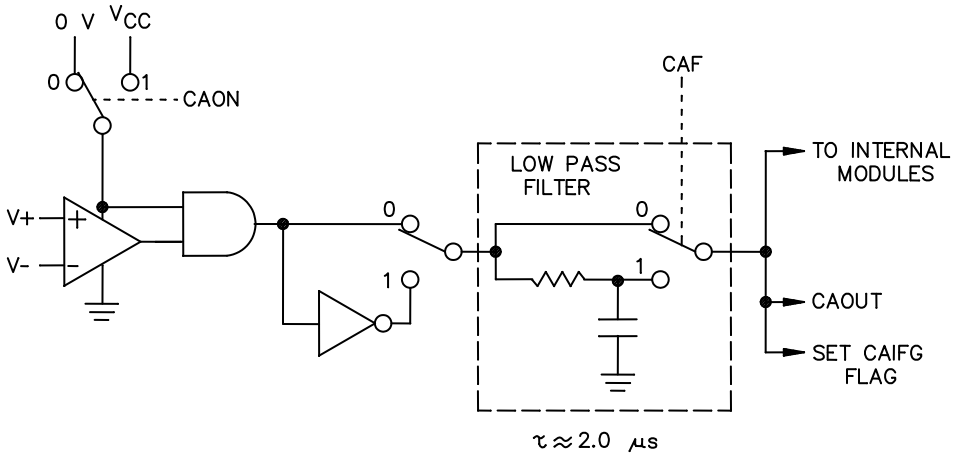
SPI SLAVE MODE, CKPH = 1

FIGURE 14. Test circuits and timing waveforms

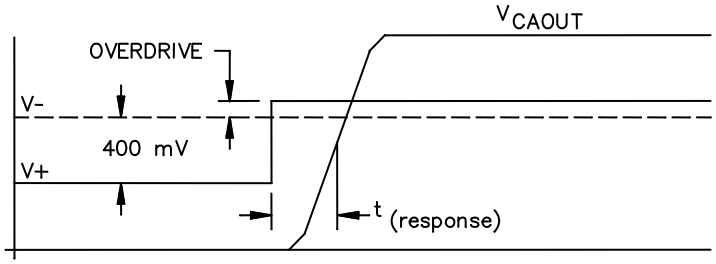


I2C MODE TIMING

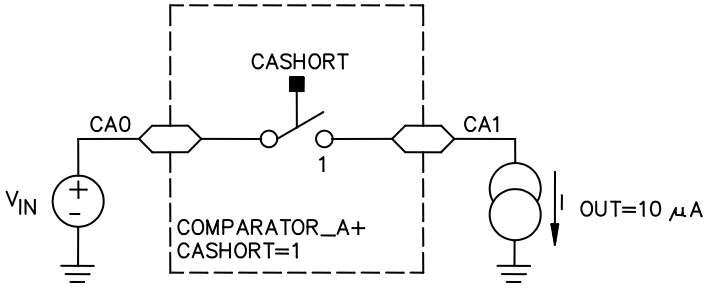
FIGURE 15. Test circuits and timing waveforms



BLOCK DIAGRAM OF COMPARATOR_A MODULE

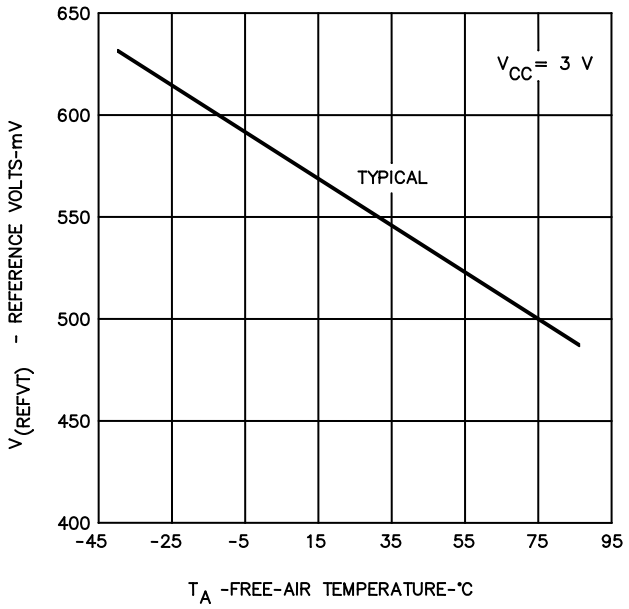


OVERDRIVE DEFINITION

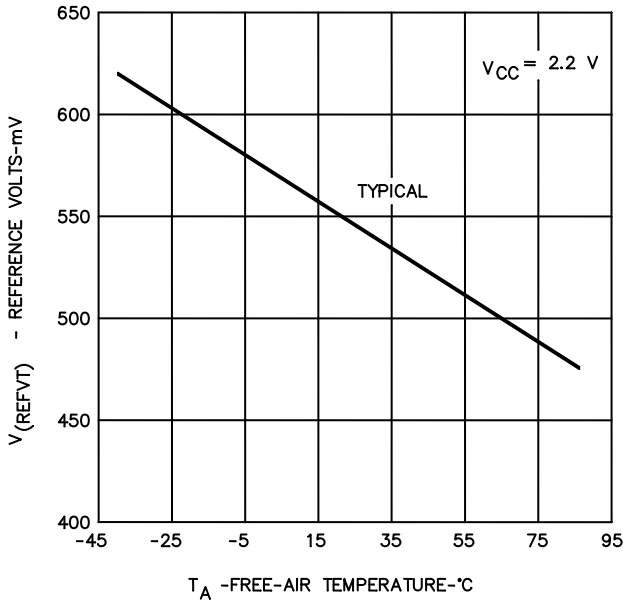


COMPARATOR_A+ SHORT RESISTANCE TEST CONDITIONS

FIGURE 16. Test circuits and timing waveforms

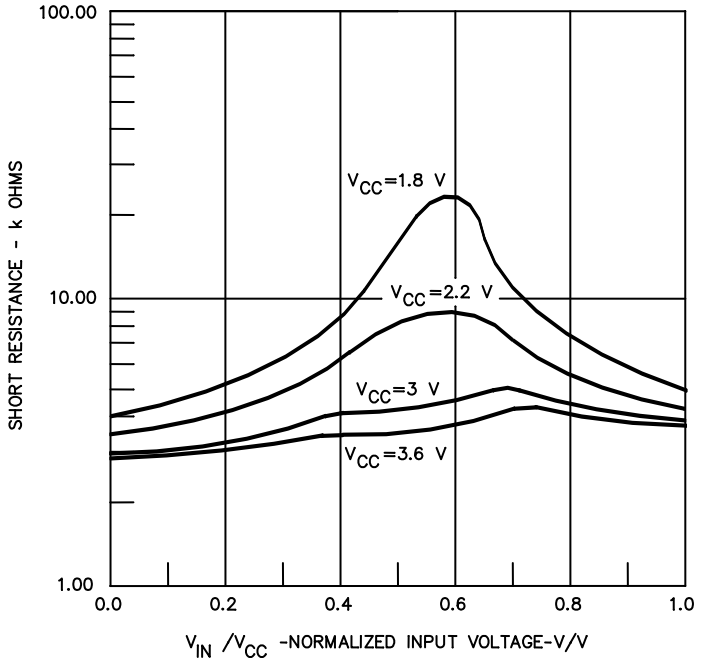


$V_{(REFVT)}$ vs TEMPERATURE, V_{CC} = 3 V



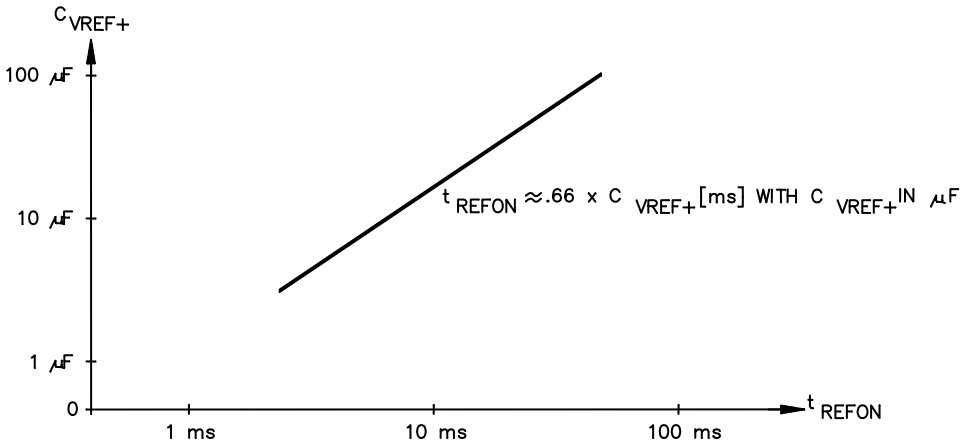
$V_{(REFVT)}$ vs TEMPERATURE, V_{CC} = 2.2 V

FIGURE 17. Test circuits and timing waveforms



SHORT RESISTANCE vs V_{IN}/V_{CC}

FIGURE 18. Test circuits and timing waveforms



TYPICAL SETTLING TIME OF INTERNAL REFERENCE t_{REFON} vs EXTERNAL CAPACITOR ON V_{REF+}

FIGURE 19. Test circuits and timing waveforms

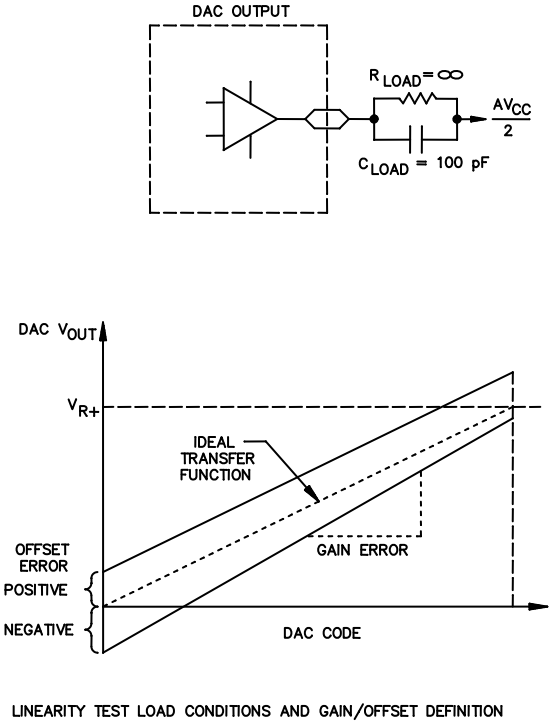


FIGURE 20. Test circuits and timing waveforms

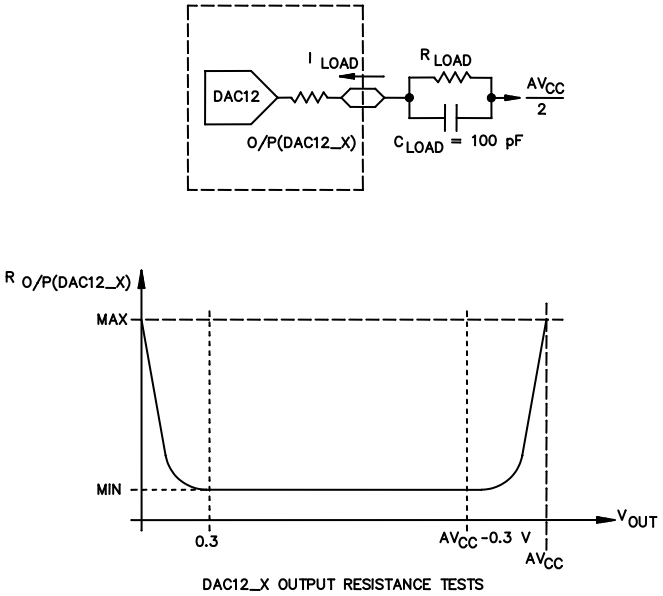


FIGURE 21. Test circuits and timing waveforms

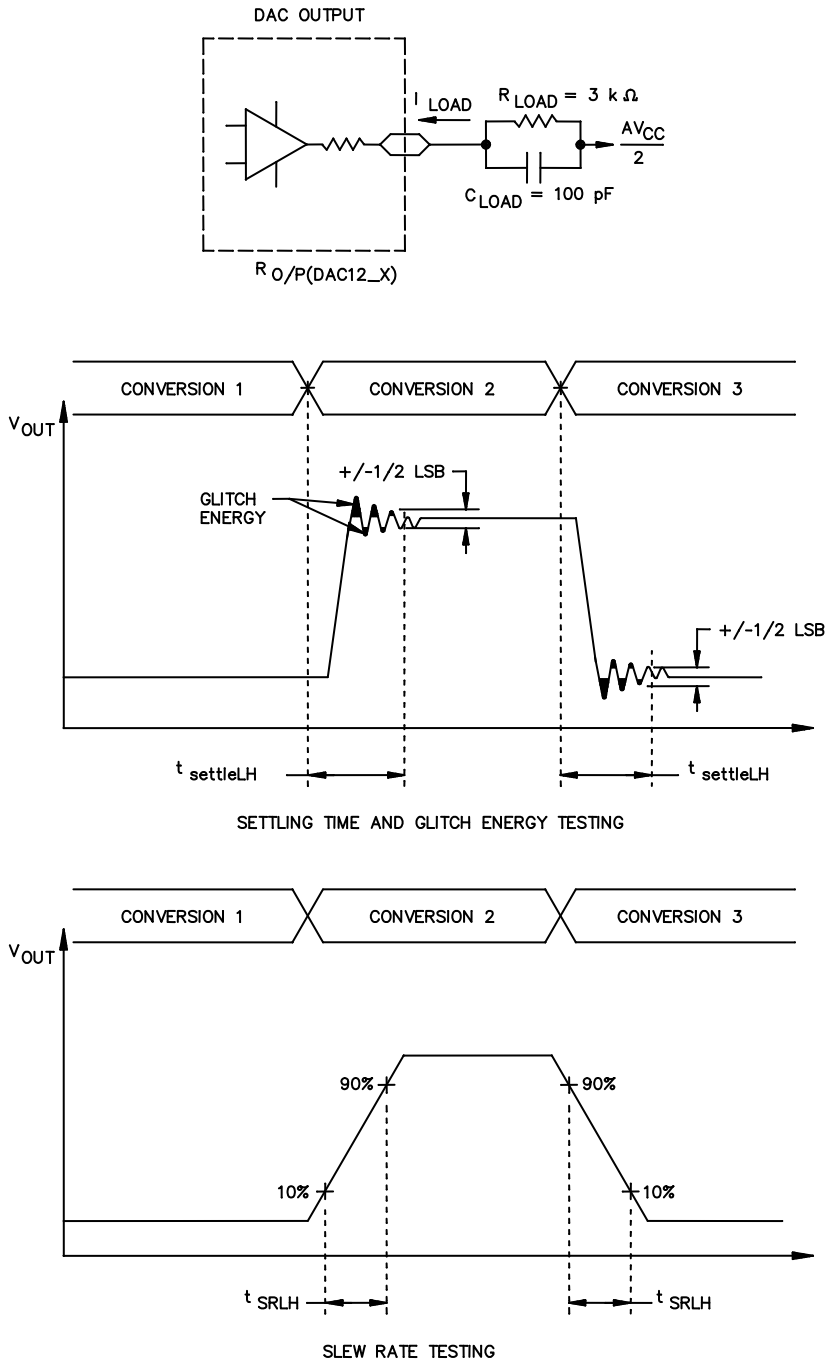
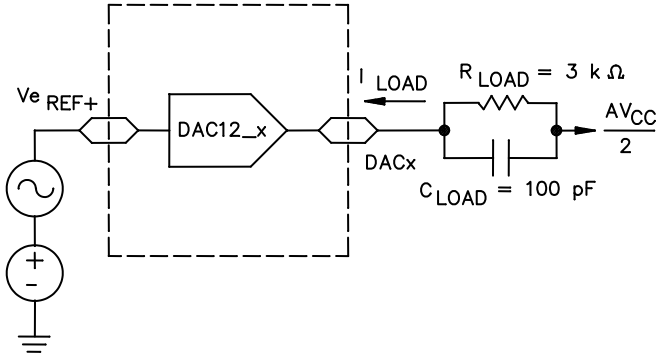
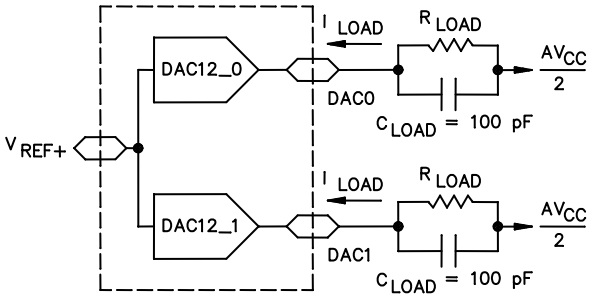


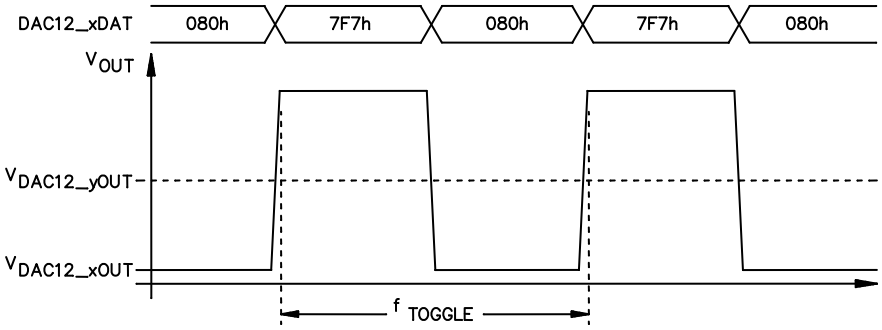
FIGURE 22. Test circuits and timing waveforms



TEST CONDITIONS FOR 3-dB BANDWIDTH SPECIFICATIONS

FIGURE 23. Test circuits and timing waveforms





CROSSTALK TEST CONDITIONS

FIGURE 24. Test circuits and timing waveforms

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/09620-01XE	01295	MSP430F2618TGQWTEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493