REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate paragraphs to current requirements. - PHN	17-06-29	Thomas M. Hess
B	Update boilerplate paragraphs to current VID description requirements. - PHN	23-07-25	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV																						
SHEET																						
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16						

PMIC N/A

Original date of drawing

YY MM DD

09-03-09

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COLUMBUS, OHIO 43218-3990
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TITLE
MICROCIRCUIT, DIGITAL, 4-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/09618
REV B		PAGE 1 OF 16

AMSC N/A

5962-V126-23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 4-bit dual-supply bus transceiver with configurable voltage translation and 3-state outputs microcircuit, with an operating temperature range of -55ºC to +125ºC.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/09618	-	01	X	E
Drawing number		Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74AVCH4T245-EP	4-bit dual-supply bus transceiver with configurable voltage translation and 3-state outputs

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	JEDEC MO-288	Plastic quad flatpack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range, ($V_{CCA,}$ V_{CCB})	-0.5 V to +4.6 V
Input voltage range, (V_I):	
I/O ports (A port)	-0.5 V to +4.6 V 2/
I/O ports (B port)	-0.5 V to +4.6 V 2/
Control inputs	-0.5 V to +4.6 V 2/
Voltage range applied to any output in the high impedance or power-off stage, (V_O):	
A port	-0.5 V to +4.6 V 2/
B port	-0.5 V to +4.6 V 2/
Voltage range applied to any output in the high or slow state, (V_O):	
A port	-0.5 V to V_{CCA} + 0.5 V 2/ 3/
B port	-0.5 V to V_{CCB} + 0.5 V 2/ 3/
Maximum input clamp current, (I_{IK}) (V_I < 0)	-50 mA
Maximum output clamp current, (I_{OK}) (V_O < 0)	-50 mA
Maximum continuous output current, (I_O)	±50 mA
Maximum continuous current through V_{CCA}, V_{CCB}, or GND	±100 mA
Maximum package thermal impedance (θ_{JA})	184 °C/W
Storage temperature range, (T_{STG})	-65°C to +150°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input voltage and output negative-voltage ratings may exceeded if the input and output current ratings are observed.
3/ The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

1.4 Recommended operating conditions. 4/ 5/ 6/ 7/

		V_{CCI}	V_{CCO}	Min	Max	Unit
Supply voltage, (V_{CCA})				1.2	3.6	V
Supply voltage, (V_{CCB})				1.2	3.6	V
High level input voltage, (V_{IH})	Data inputs 8/	1.2 V to 1.95 V		0.65 x V_{CCI}		V
		1.95 V to 2.7 V		1.6		V
		2.7 V to 3.6 V		2		V
Low level input voltage, (V_{IL})	Data inputs 8/	1.2 V to 1.95 V			0.35 x V_{CCI}	V
		1.95 V to 2.7 V			0.7	V
		2.7 V to 3.6 V			0.8	V
High level input voltage, (V_{IH})	DIR 9/ referenced to V_{CCA}	1.2 V to 1.95 V		0.65 x V_{CCA}		V
		1.95 V to 2.7 V		1.6		V
		2.7 V to 3.6 V		2		V
Low level input voltage, (V_{IL})	DIR 9/ referenced to V_{CCA}	1.2 V to 1.95 V			0.35 x V_{CCA}	V
		1.95 V to 2.7 V			0.7	V
		2.7 V to 3.6 V			0.8	V
Input voltage, (V_I)				0	3.6	V
Output voltage, ($V_{/O}$)	Active state			0	V_{CCO}	V
	3-state			0	3.6	V
High level output current, (I_{OH})			1.2 V		-3	mA
			1.4 V to 1.6 V		-6	mA
			1.65 V to 1.95 V		-8	mA
			2.3 V to 2.7 V		-9	mA
			3.0 V to 3.6 V		-12	mA
Low level output current, (I_{OL})			1.2 V		3	mA
			1.4 V to 1.6 V		6	mA
			1.65 V to 1.95 V		8	mA
			2.3 V to 2.7 V		9	mA
			3.0 V to 3.6 V		12	mA
Input transition rise or fall rate, ($\Delta t/\Delta v$)					5	ns/V
Operating free air temperature, (T_A)				-55	125	°C

4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
5/ V_{CCI} is the V_{CC} associated with the input port.
6/ V_{CCO} is the V_{CC} associated with the output port.
7/ All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to manufacturer for more information.
8/ For V_{CCI} values not specified, V_{IH} min = V_{CCI} x 0.7, V_{IL} max = V_{CCI} x 0.3 V.
9/ For V_{CCA} values not specified, V_{IH} min = V_{CCA} x 0.7, V_{IL} max = V_{CCA} x 0.3 V.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Function table. The function table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Load circuit and voltage waveforms. The load circuit and timing waveforms shall be as specified in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test		Symbol	Conditions 2/ 3/ $-55^{\circ}C \le T_A \le +125^{\circ}C$ unless otherwise specified	V_{CCA}	V_{CCB}	Limits		Unit
						Min	Max	
High level output voltage		V_{OH}	$V_I = V_{IH}$, I_{OH} = -100 µA	1.2 V to 3.6 V	1.2 V to 3.6 V	V_{CCO}– 0.2		V
			$V_I = V_{IH}$, I_{OH} = -3 mA, $T_A = 25^{\circ}C$	1.2 V	1.2 V	0.95	TYP	V
			$V_I = V_{IH}$, I_{OH} = -6 mA	1.4 V	1.4 V	1.05		V
			$V_I = V_{IH}$, I_{OH} = -8 mA	1.65 V	1.65 V	1.2		V
			$V_I = V_{IH}$, I_{OH} = -9 mA	2.3 V	2.3 V	1.75		V
			$V_I = V_{IH}$, I_{OH} = -12 mA	3.0 V	3.0 V	2.3		V
Low level output voltage		V_{OL}	$V_I = V_{IL}$, I_{OL} = 100 µA	1.2 V to 3.6 V	1.2 V to 3.6 V		0.2	V
			$V_I = V_{IL}$, I_{OL} = 3 mA, $T_A = 25^{\circ}C$	1.2 V	1.2 V	0.15	TYP	V
			$V_I = V_{IL}$, I_{OL} = 6 mA	1.4 V	1.4 V		0.35	V
			$V_I = V_{IL}$, I_{OL} = 8 mA	1.65 V	1.65 V		0.45	V
			$V_I = V_{IL}$, I_{OL} = 9 mA	2.3 V	2.3 V		0.55	V
			$V_I = V_{IL}$, I_{OL} = 12 mA	3.0 V	3.0 V		0.7	V
Input current	DIR input	I_I	$V_I = V_{CCA}$ or GND	1.2 V to 3.6 V	1.2 V to 3.6 V		±1	µA
			$V_I = V_{CCA}$ or GND, $T_A = 25^{\circ}C$	1.2 V to 3.6 V	1.2 V to 3.6 V		±0.25	µA
Bus-hold low level input current		I_{BHL} 4/	V_I = 0.42 V, $T_A = 25^{\circ}C$	1.2 V	1.2 V	25	TYP	µA
			V_I = 0.49 V	1.4 V	1.4 V	15		µA
			V_I = 0.58 V	1.65 V	1.65 V	25		µA
			V_I = 0.7 V	2.3 V	2.3 V	45		µA
			V_I = 0.8 V	3.3 V	3.3 V	100		µA
Bus-hold high level input current		I_{BHH} 5/	V_I = 0.78 V, $T_A = 25^{\circ}C$	1.2 V	1.2 V	-25	TYP	µA
			V_I = 0.91 V	1.4 V	1.4 V	-15		µA
			V_I = 1.07 V	1.65 V	1.65 V	-25		µA
			V_I = 1.6 V	2.3 V	2.3 V	-45		µA
			V_I = 2.0 V	3.3 V	3.3 V	-100		µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test		Symbol	Conditions 2/ 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	V_{CCA}	V_{CCB}	Limits		Unit
						Min	Max	
Bus-hold low level output current		I_{BHLO} 6/	V_I = 0 to V_{CCI}, T_A = 25°C	1.2 V	1.2 V	50	TYP	µA
			V_I = 0 to V_{CCI}	1.6 V	1.6 V	125		µA
				1.95 V	1.95 V	200		µA
				2.7 V	2.7 V	300		µA
				3.6 V	3.6 V	500		µA
Bus-hold high level output current		I_{BHHO} 7/	V_I = 0 to V_{CCI}, T_A = 25°C	1.2 V	1.2 V	-50	TYP	µA
			V_I = 0 to V_{CCI}	1.6 V	1.6 V	-125		µA
				1.95 V	1.95 V	-200		µA
				2.7 V	2.7 V	-300		µA
				3.6 V	3.6 V	-500		µA
Input/Output power off leakage current	A port	I_{off}	V_I or V_O = 0 to 3.6 V	0 V	0 V to 3.6 V		±13	µA
	B port			0 V to 3.6 V	0 V		±13	µA
	A port		V_I or V_O = 0 to 3.6 V,	0 V	0 V to 3.6 V		±1	µA
	B port		T_A = 25°C	0 V to 3.6 V	0 V		±1	µA
High impedance state output current	A or B port	I_{OZ} 8/	$\overline{OE}$ = V_{IH}, V_O = V_{CCO} or GND, V_I = V_{CCI} or GND	3.6 V	3.6 V		±5	µA
			$\overline{OE}$ = V_{IH}, V_O = V_{CCO} or GND, V_I = V_{CCI} or GND, T_A = 25°C	3.6 V	3.6 V		±2.5	µA
	B port		$\overline{OE}$ = don't care, V_O = V_{CCO} or GND,	0 V	3.6 V		±14	µA
	A port		V_I = V_{CCI} or GND	3.6 V	0 V		±5	µA
Quiescent supply currents		I_{CCA}	V_I = V_{CCI} or GND, I_O = 0	1.2 V to 3.6 V	1.2 V to 3.6 V		8	µA
				0 V	3.6 V		-2	µA
				3.6 V	0 V		8	µA
		I_{CCB}	V_I = V_{CCI} or GND, I_O = 0	1.2 V to 3.6 V	1.2 V to 3.6 V		8	µA
				0 V	3.6 V		8	µA
				3.6 V	0 V		-2	µA
		I_{CCA} + I_{CCB}	V_I = V_{CCI} or GND, I_O = 0	1.2 V to 3.6 V	1.2 V to 3.6 V		16	µA
Input capacitance	Control inputs	C_i	V_I = 3.3 V or GND	3.3 V	3.3 V		4.5	pF
			V_I = 3.3 V or GND, T_A = 25°C	3.3 V	3.3 V	3.5	TYP	pF
Input/Output capacitance	A or B port	C_{io}	V_O = 3.3 V or GND	3.3 V	3.3 V		7	pF
			V_O = 3.3 V or GND, T_A = 25°C	3.3 V	3.3 V	6	TYP	pF

See footnote at end of the table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbo l	Conditions T_A = +25ºC unless otherwise specified	V_{CCB} = 1.2 V TYP	V_{CCB} = 1.5 V ±0.1 V TYP	V_{CCB} = 1.8 V ±0.15 V TYP	V_{CCB} = 2.5 V ±0.2 V TYP	V_{CCB} = 3.3 V ±0.3 V TYP	Unit
Switching characteristics, V_{CCA} = 1.2 V								
Propagation delay time, from input A to output B	t_{PLH}	See figure 5.	3.4	2.9	2.7	2.6	2.8	ns
	t_{PHL}		3.4	2.9	2.7	2.6	2.8	ns
Propagation delay time, from input B to output A	t_{PLH}		3.6	3.1	2.8	2.6	2.6	ns
	t_{PHL}		3.6	3.1	2.8	2.6	2.6	ns
Enable time, from input $\overline{OE}$ to output A	t_{PZH}		5.6	4.7	4.3	3.9	3.7	ns
	t_{PZL}		5.6	4.7	4.3	3.9	3.7	ns
Enable time, from input $\overline{OE}$ to output B	t_{PZH}		5	4.3	3.9	3.6	3.6	ns
	t_{PZL}		5	4.3	3.9	3.6	3.6	ns
Disable time, from input $\overline{OE}$ to output A	t_{PHZ}		6.2	5.2	5.2	4.3	4.8	ns
	t_{PLZ}		6.2	5.2	5.2	4.3	4.8	ns
Disable time, from input $\overline{OE}$ to output B	t_{PHZ}		5.9	5.1	5	4.7	5.5	ns
	t_{PLZ}		5.9	5.1	5	4.7	5.5	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions -55°C ≤ T_A ≤ +125°C unless otherwise specified	V_{CCB} = 1.2 V TYP	V_{CCB} = 1.5 V ±0.1 V Min	 Max	V_{CCB} = 1.8 V ±0.15 V Min	 Max	V_{CCB} = 2.5 V ±0.2 V Min	 Max	V_{CCB} = 3.3 V ±0.3 V Min	 Max	Unit
Switching characteristics, V_{CCA} = 1.5 V ±0.1 V												
Propagation delay time, from input A to output B	t_{PLH}	See figure 5.	3.2	0.3	10.3	0.3	9.2	0.4	8.2	0.4	8.2	ns
	t_{PHL}		3.2	0.3	10.3	0.3	9.2	0.4	8.2	0.4	8.2	ns
Propagation delay time, from input B to output A	t_{PLH}		3.3	0.7	10.3	0.5	10	0.4	9.7	0.3	9.6	ns
	t_{PHL}		3.3	0.7	10.3	0.5	10	0.4	9.7	0.3	13.6	ns
Enable time, from input $\overline{OE}$ to output A	t_{PZH}		4.9	1.4	13.6	1.1	13.5	0.7	13.4	0.4	13.4	ns
	t_{PZL}		4.9	1.4	13.6	1.1	13.5	0.7	13.4	0.4	13.4	ns
Enable time, from input $\overline{OE}$ to output B	t_{PZH}		4.5	1.4	14.6	1.1	11.7	0.9	9.8	0.9	9.6	ns
	t_{PZL}		4.5	1.4	14.6	1.1	11.7	0.9	9.8	0.9	9.6	ns
Disable time, from input $\overline{OE}$ to output A	t_{PHZ}		5.6	1.8	14.2	1.5	14.2	1.3	14.2	1.6	14.2	ns
	t_{PLZ}		5.6	1.8	14.2	1.5	14.2	1.3	14.2	1.6	14.2	ns
Disable time, from input $\overline{OE}$ to output B	t_{PHZ}		5.2	1.9	14.3	1.9	13.1	1.4	11.4	1.2	11.6	ns
	t_{PLZ}		5.2	1.9	14.3	1.9	13.1	1.4	11.4	1.2	11.6	ns
Switching characteristics, V_{CCA} = 1.8 V ±0.15 V												
Propagation delay time, from input A to output B	t_{PLH}	See figure 5.	2.9	0.1	10	0.1	8.9	0.1	7.9	0.3	7.9	ns
	t_{PHL}		2.9	0.1	10	0.1	8.9	0.1	7.9	0.3	7.9	ns
Propagation delay time, from input B to output A	t_{PLH}		3	0.6	9.3	0.5	8.9	0.3	8.6	0.3	8.5	ns
	t_{PHL}		3	0.6	9.3	0.5	8.9	0.3	8.6	0.3	8.5	ns
Enable time, from input $\overline{OE}$ to output A	t_{PZH}		4.4	1	13.4	1	11.3	0.6	11.3	0.4	11.2	ns
	t_{PZL}		4.4	1	13.4	1	11.3	0.6	11.3	0.4	11.2	ns
Enable time, from input $\overline{OE}$ to output B	t_{PZH}		4.1	1.2	14.4	1	12.4	0.8	9.3	0.8	8.6	ns
	t_{PZL}		4.1	1.2	14.4	1	12.4	0.8	9.3	0.8	8.6	ns
Disable time, from input $\overline{OE}$ to output A	t_{PHZ}		5.4	1.6	12.6	1.8	12.7	1.3	12.7	1.6	12.7	ns
	t_{PLZ}		5.4	1.6	12.6	1.8	12.7	1.3	12.7	1.6	12.7	ns
Disable time, from input $\overline{OE}$ to output B	t_{PHZ}		5	1.7	13.9	1.6	12.7	1.2	10.9	1	10.9	ns
	t_{PLZ}		5	1.7	13.9	1.6	12.7	1.2	10.9	1	10.9	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ±0.1 V		V_{CCB} = 1.8 V ±0.15 V		V_{CCB} = 2.5 V ±0.2 V		V_{CCB} = 3.3 V ±0.3 V		Unit
			TYP	Min	Max	Min	Max	Min	Max	Min	Max	
Switching characteristics, V_{CCA} = 2.5 V ±0.1 V												
Propagation delay time, from input A to output B	t_{PLH}	See figure 5.	2.8	0.1	9.7	0.1	8.6	0.2	7.5	0.1	7.6	ns
	t_{PHL}		2.8	0.1	9.7	0.1	8.6	0.2	7.5	0.1	7.6	ns
Propagation delay time, from input B to output A	t_{PLH}		2.7	0.6	8.2	0.4	7.9	0.2	7.4	0.2	7.3	ns
	t_{PHL}		2.7	0.6	8.2	0.4	7.9	0.2	7.4	0.2	7.3	ns
Enable time, from input $\overline{OE}$ to output A	t_{PZH}		4	0.7	10.5	0.7	9.2	0.6	8.8	0.4	8.8	ns
	t_{PZL}		4	0.7	10.5	0.7	9.2	0.6	8.8	0.4	8.8	ns
Enable time, from input $\overline{OE}$ to output B	t_{PZH}		3.8	0.9	14.8	0.8	12	0.6	9.8	0.6	9	ns
	t_{PZL}		3.8	0.9	14.8	0.8	12	0.6	9.8	0.6	9	ns
Disable time, from input $\overline{OE}$ to output A	t_{PHZ}		4.7	1	12.4	1	12.4	1	10.2	1	10.6	ns
	t_{PLZ}		4.7	1	12.4	1	12.4	1	10.2	1	10.6	ns
Disable time, from input $\overline{OE}$ to output B	t_{PHZ}		4.5	1.5	13.4	1.3	12.2	1.1	10.2	0.9	9.2	ns
	t_{PLZ}		4.5	1.5	13.4	1.3	12.2	1.1	10.2	0.9	9.2	ns
Switching characteristics, V_{CCA} = 3.3 V ±0.3 V												
Propagation delay time, from input A to output B	t_{PLH}	See figure 5.	2.9	0.1	9.6	0.1	8.5	0.1	7.3	0.1	6.9	ns
	t_{PHL}		2.9	0.1	9.6	0.1	8.5	0.1	7.3	0.1	6.9	ns
Propagation delay time, from input B to output A	t_{PLH}		2.6	0.6	8.2	0.4	7.4	0.2	7	0.1	6.8	ns
	t_{PHL}		2.6	0.6	8.2	0.4	7.4	0.2	7	0.1	6.8	ns
Enable time, from input $\overline{OE}$ to output A	t_{PZH}		3.8	0.6	12.7	0.6	9.2	0.6	7.8	0.4	7.8	ns
	t_{PZL}		3.8	0.6	12.7	0.6	9.2	0.6	7.8	0.4	7.8	ns
Enable time, from input $\overline{OE}$ to output B	t_{PZH}		3.7	0.8	14.7	0.6	11.8	0.5	9.7	0.5	8.8	ns
	t_{PZL}		3.7	0.8	14.7	0.6	11.8	0.5	9.7	0.5	8.8	ns
Disable time, from input $\overline{OE}$ to output A	t_{PHZ}		4.8	0.7	13.3	0.7	12.3	0.7	9.6	0.7	10.6	ns
	t_{PLZ}		4.8	0.7	13.3	0.7	12.3	0.7	9.6	0.7	10.6	ns
Disable time, from input $\overline{OE}$ to output B	t_{PHZ}		5.3	1.4	13.3	1.2	12.1	1	10.4	0.8	10.2	ns
	t_{PLZ}		5.3	1.4	13.3	1.2	12.1	1	10.4	0.8	10.2	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test		Symbol	Conditions T_A = +25ºC unless otherwise specified	V_{CCB} = 1.2 V TYP	V_{CCB} = 1.5 V ±0.1 V TYP	V_{CCB} = 1.8 V ±0.15 V TYP	V_{CCB} = 2.5 V ±0.2 V TYP	V_{CCB} = 3.3 V ±0.3 V TYP	Unit
Operating characteristics									
Power dissipation capacitance, from A to B	Outputs enabled	C_{pdA} 9/	C_L = 0, f = 10 MHz, t_r, t_f = 1 ns	1	1	1	1.5	2	pF
	Outputs disabled			1	1	1	1	1	pF
Power dissipation capacitance, from B to A	Outputs enabled			12	12.5	13	14	15	pF
	Outputs disabled			1	1	1	1	1	pF
Power dissipation capacitance, from A to B	Outputs enabled	C_{pdB} 9/	C_L = 0, f = 10 MHz, t_r, t_f = 1 ns	12	12.5	13	14	15	pF
	Outputs disabled			1	1	1	1	1	pF
Power dissipation capacitance, from B to A	Outputs enabled			1	1	1	1	2	pF
	Outputs disabled			1	1	1	1	1	pF

1. Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2. V_{CCO} is the V_{CC} associated with the output port.
3. V_{CCI} is the V_{CC} associated with the input port.
4. The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.
5. The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.
6. An external driver must source at least I_{BHLO} to switch this node from low to high.
7. An external driver must sink at least I_{BHHO} to switch this node from high to low.
8. For I/O ports, the parameter I_{OZ} includes the input leakage current.
9. Power dissipation capacitance per transceiver.

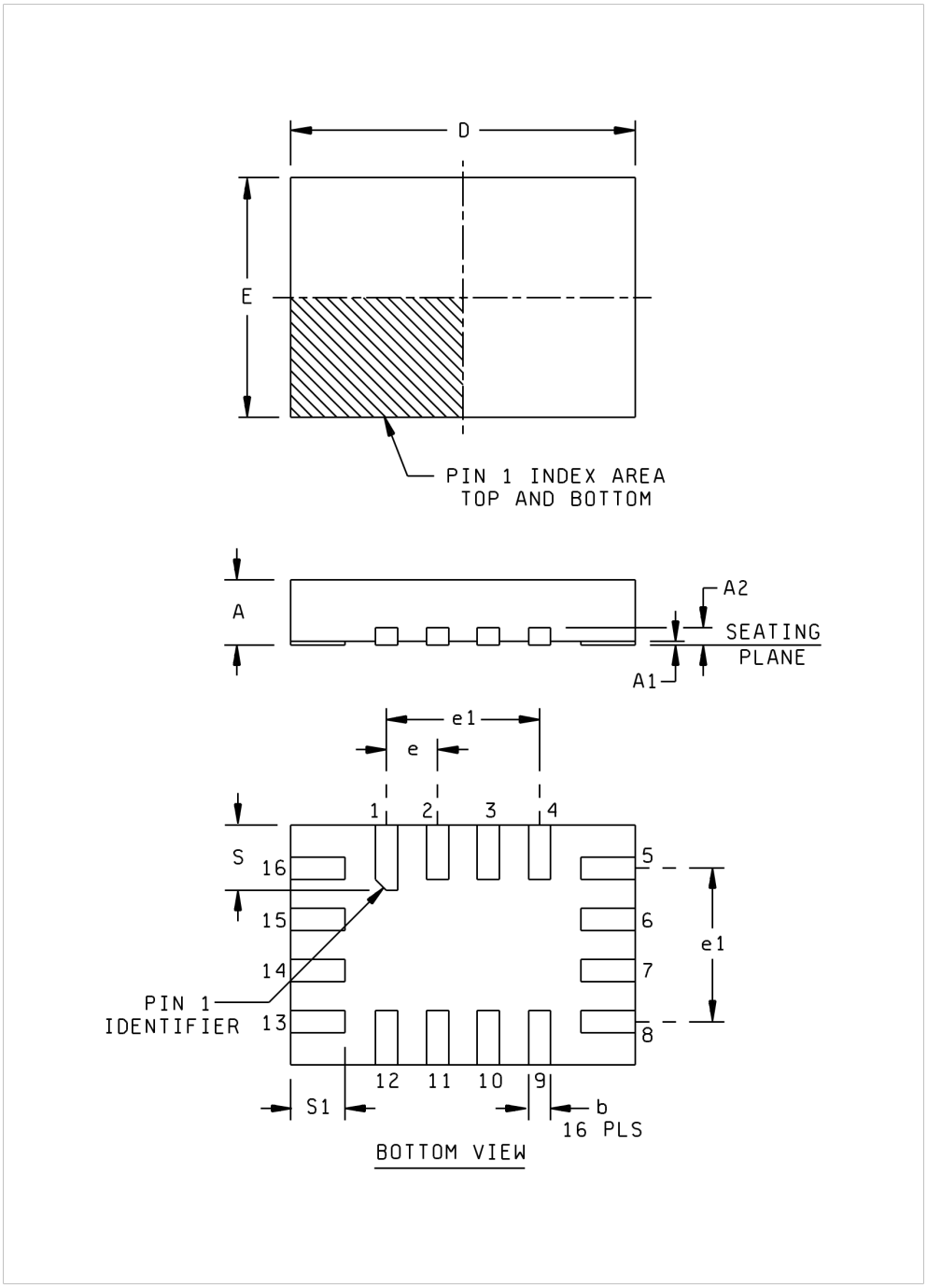


FIGURE 1. Case outlines.

Case X

Dimensions

Symbol	Min	Max	Symbol	Min	Max
A	0.45	0.55	E	1.75	1.85
A1	0.00	0.05	e	0.40 TYP	
A2	0.13 NOM		e1	1.20 TYP	
b	0.15	0.25	S	0.45	0.55
D	2.55	2.65	S1	0.35	0.45

Notes:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-288 variation UFHE, except minimum package thickness.

FIGURE 1. Case outlines - Continued.

(Each 2-bit section)

Control Inputs		Output circuits		Operation
$\overline{OE}$	DIR	A Port	B Port	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

Note: Input circuits of the data I/Os are always active.

FIGURE 2. Function Table

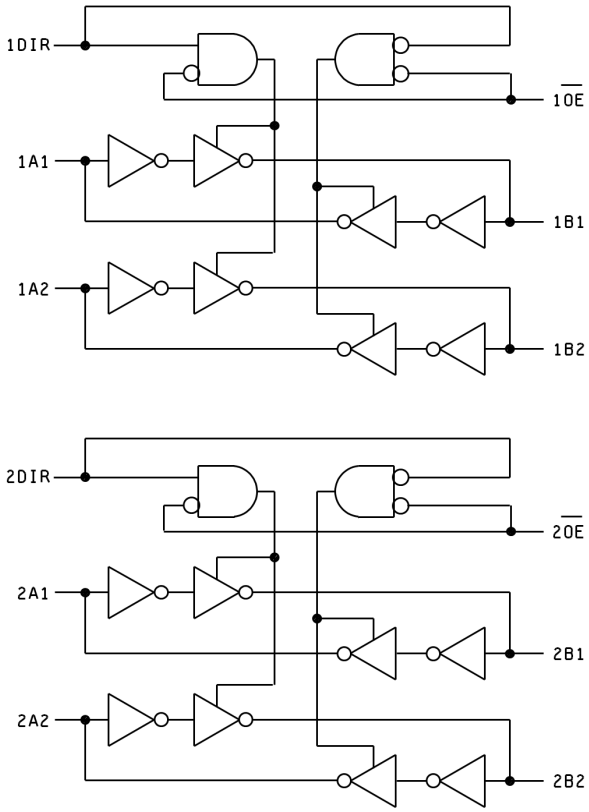
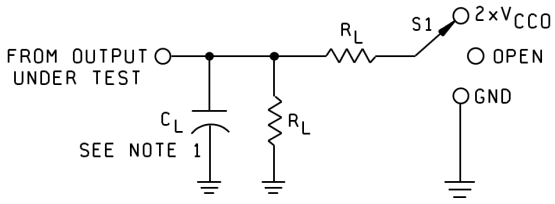


FIGURE 3. Logic diagram.

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{1OE}$	9	2A2
2	VCCB	10	GND
3	VCCA	11	GND
4	1DIR	12	2B2
5	2DIR	13	2B1
6	1A1	14	1B2
7	1A2	15	1B1
8	2A1	16	$\overline{2OE}$

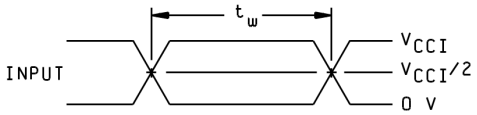
FIGURE 4. Terminal connections.



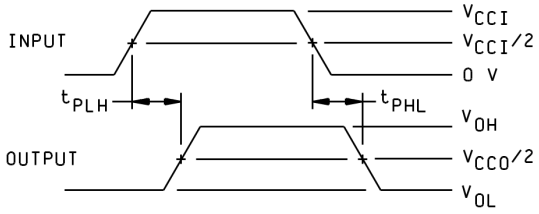
LOAD CIRCUIT

TEST	S1
t_{pd}	OPEN
t_{PLZ}/t_{PZL}	$2\times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

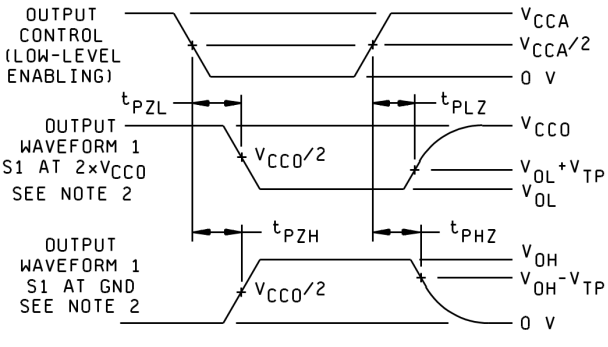
V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 kΩ	0.1 V
1.5 V ±0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ±0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ±0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ±0.3 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

Notes:
1. C_L includes probe and test fixture capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
4. The outputs are measured one at a time with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same t_{dis}.
6. t_{PZL} and t_{PZH} are the same t_{en}.
7. t_{PLH} and t_{PHL} are the same t_{pd}.
8. V_{CCI} is the V_{CC} associated with the input port.
9. V_{CCO} is the V_{CC} associated with the input port

FIGURE 5. Load circuit and voltage waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/09618-01XE	01295	CAVCH4T245MRSVREP	SODM

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243