REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 09-01-13	**CHECKED BY** RAJESH PITHADIA	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, 4:1 HIGH SPEED MULTIPLEXER, MONOLITHIC SILICON
	APPROVED BY ROBERT M. HEBER	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/09616**
	REV	**PAGE** 1 **OF** 14

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 4:1 high speed multiplexer microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/09616	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	OPA4872-EP	4:1 high speed multiplexer

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	14	MS-012-AB	Plastic surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Power supply voltage ..... ±6.5 V
Input voltage range ..... $\pm V_S$
Power dissipation (P_D) ..... 312.5 mW
Storage temperature range (T_{STG})..... -65°C to +125°C
Lead temperature (soldering, 10 seconds) ..... +260°C
Junction temperature (T_J) ..... +150°C
Junction temperature: continuous operation, long term reliability ..... +140°C
Thermal resistance, junction to ambient (θ_{JA}) ..... 80°C/W
Electrostatic discharge (ESD) rating:
  Human body model (HBM) ..... 1500 V
  Charged device model (CDM) ..... 1000 V
  Machine model (MM) ..... 200 V

1.4 Recommended operating conditions. 2/

Power supply voltage ..... ±5 V
Operating free-air temperature range (T_A) ..... -55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ 3/ 4/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC performance section							
Small signal bandwidth	SSBW	V_O = 500 mV_{PP}, R_L = 150 Ω	+25°C	01	500 typical		MHz
Bandwidth for 0.1 db flatness	BW	V_O = 500 mV_{PP}, R_L = 150 Ω	+25°C	01	120 typical		MHz
Large signal bandwidth	LSBW	V_O = 2 V_{PP}, R_L = 150 Ω	+25°C	01	500 typical		MHz
Slew rate	SR	4 V step	+25°C	01	2300 typical		V/μs
Rise time and fall time	t_r, t_f	4 V step	+25°C	01	1.25 typical		ns
Settling time	t_S	To 0.05 %, 2 V step	+25°C	01	15 typical		ns
		To 0.1 %, 2 V step			14 typical		
Channel switching time	t_{CS}		+25°C	01	10 typical		ns
Second harmonic distortion	HD2	G = +2 V/V, f = 10 MHz, V_O = 2 V_{PP}, R_L = 150 Ω	+25°C	01	-60 typical		dBc
Third harmonic distortion	HD3	G = +2 V/V, f = 10 MHz, V_O = 2 V_{PP}, R_L = 150 Ω	+25°C	01	-78 typical		dBc
Input voltage noise	N_{IV}	f > 100 kHz	+25°C	01	4.5 typical		nV / $\sqrt{Hz}$
Noninverting input current noise	N_{NIN}	f > 100 kHz	+25°C	01	4.0 typical		pA / $\sqrt{Hz}$
Inverting input current noise	N_{IN}	f > 100 kHz	+25°C	01	19 typical		pA / $\sqrt{Hz}$
Differential gain	GD	G = +2 V/V, PAL, V_O = 1.4 V_P	+25°C	01	0.035 typical		%
Differential phase	GP	G = +2 V/V, PAL, V_O = 1.4 V_P	+25°C	01	0.005 typical		°
All hostile crosstalk, input referred	CT	3 channels driven at 5 MHz, 1 V_{PP}	+25°C	01	-80 typical		dB
		3 channels driven at 30 MHz, 1 V_{PP}			-66 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/ 4/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
DC performance	section						
Open loop transimpedance	Z_{OL}	V_O = 0 V, R_L = 100 Ω	+25°C	01	92		kΩ
			-55°C to +125°C		60		
Input offset voltage	V_{IO}	V_{CM} = 0 V	+25°C	01		±5	mV
			-55°C to +125°C			±10.5	
Average input offset voltage drift	ΔVIO	V_{CM} = 0 V	-55°C to +125°C	01		±30	µV/°C
Input offset voltage matching	V_{IOM}	V_{CM} = 0 V	+25°C	01		±5	mV
			-55°C to +125°C			±10.5	
Noninverting input bias current	I_{NIB}	V_{CM} = 0 V	+25°C	01		±14	µA
			-55°C to +125°C			±20	
Average noninverting input bias current	ΔI_{NIB}	V_{CM} = 0 V	-55°C to +125°C	01		±48	nA/°C
Inverting bias current	I_{IB}	V_{CM} = 0 V	+25°C	01		±18	µA
			-55°C to +125°C			±35	
Average inverting input bias current	ΔI_{IB}	V_{CM} = 0 V	-55°C to +125°C	01		±125	nA/°C
Input section							
Common mode input range	CMIR	Each noninverting input	+25°C	01	±2.55		V
			-55°C to +125°C		±2.4		
Common mode rejection ratio	CMRR	V_{CM} = 0 V, input referred, noninverting input	+25°C	01	50		dB
			-55°C to +125°C		43		
Input resistance	R_{IN}	Noninverting, channel enabled	+25°C	01	2.5 typical		MΩ
		Inverting, open loop			70 typical		Ω
Input capacitance	C_{IN}	Noninverting, channel enabled	+25°C	01	0.9 typical		pF
		Channel deselected			0.9 typical		
		Chip disabled			0.9 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/ 4/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Output section							
Output voltage swing	V_{OUT}	$R_L \geq 1$ kΩ	+25°C	01	±3.9		V
			-55°C to +125°C		±3.55		
		$R_L = 150$ Ω	+25°C		±3.55		
			-55°C to +125°C		±3.35		
Output current	I_{OUT}	$V_O = 0$ V	+25°C	01	±48		mA
			-55°C to +125°C		±38		
Short circuit output current	I_{OS}	Output shorted to ground	+25°C	01	±100 typical		mA
Closed loop output impedance	Z_{CLO}	G = +2 V/V, f ≤ 100 kHz	+25°C	01	0.03 typical		Ω
ENABLE ($\overline{EN}$) section							
Power down supply current	I_{PD}	$V\overline{EN} = 0$ V	+25°C	01		3.6	mA
			-55°C to +125°C			4.3	
Disable time	t_D	$V_{IN} = \pm 0.25\ V_{DC}$	+25°C	01	25 typical		ns
Enable time	t_E	$V_{IN} = \pm 0.25\ V_{DC}$	+25°C	01	6 typical		ns
Off isolation	OI	G = +2 V/V, f = 10 MHz	+25°C	01	88 typical		dB
Output resistance in disable	R_{OD}		+25°C	01	14 typical		MΩ
Output capacitance in disable	C_{OD}		+25°C	01	2.5 typical		pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/ 4/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Digital inputs section							
Maximum logic 0	V_{L0}	A0, A1, $\overline{EN}$, SD	+25°C	01		0.8	V
			-55°C to +125°C			0.8	
Maximum logic 1	V_{L1}	A0, A1, $\overline{EN}$, SD	+25°C	01	2.0		V
			-55°C to +125°C		2.0		
Logic input current	I_{LI}	A0, A1, $\overline{EN}$, SD, input = 0 V each line	+25°C	01		40	µA
			-55°C to +125°C			55	
Output switching glitch	V_{OSG}	Channel selection, at matched load	+25°C	01	±20 typical		mV
		Channel disable, at matched load			±40 typical		
		Shutdown, at matched load			±40 typical		
Shutdown (SD) section							
Shutdown supply current	I_{SD}	V_{SD} = 0 V	+25°C	01		1.3	mA
			-55°C to +125°C			2.0	
Shutdown time	t_{SD}	V_{IN} = ±0.25 V_{DC}	+25°C	01	75 typical		ns
Enable time	$t_{\overline{EN}}$	V_{IN} = ±0.25 V_{DC}	+25°C	01	15 typical		ns
Off isolation	OI	G = +2 V/V, f = 10 MHz	+25°C	01	88 typical		dB
Output resistance in shutdown	R_{SD}		+25°C	01	14 typical		MΩ
Output capacitance in shutdown	C_{SD}		+25°C	01	2.5 typical		pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ 3/ 4/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power supply section							
Specified operating voltage	V_S		+25°C	01	±5 typical		V
Minimum operating voltage	$V_{S(min)}$		+25°C	01	±3.5		V
			-55°C to +125°C		±3.5		
Maximum operating voltage	$V_{S(max)}$		+25°C	01		±6.0	V
			-55°C to +125°C			±6.0	
Maximum quiescent current	$I_{Q(max)}$	V_S = ±5 V	+25°C	01		11	mA
			-55°C to +125°C			12.5	
Minimum quiescent current	$I_{Q(min)}$	V_S = ±5 V	+25°C	01	10		mA
			-55°C to +125°C		8.25		
Power supply rejection ratio	+PSRR	Input referred	+25°C	01	-50		dB
			-55°C to +125°C		-42		
	-PSRR		+25°C		-51		
			-55°C to +125°C		-43		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_S = ±5 V, gain (G) = +2 V/V, feedback resistance (R_F) = 523 Ω, and load resistance (R_L) = 150 Ω.

3/ Junction temperature = ambient for +25°C tested specifications.

4/ Junction temperature = ambient at low temperature limit; junction temperature = ambient +9°C at high temperature limit for over temperature specifications.

Case X

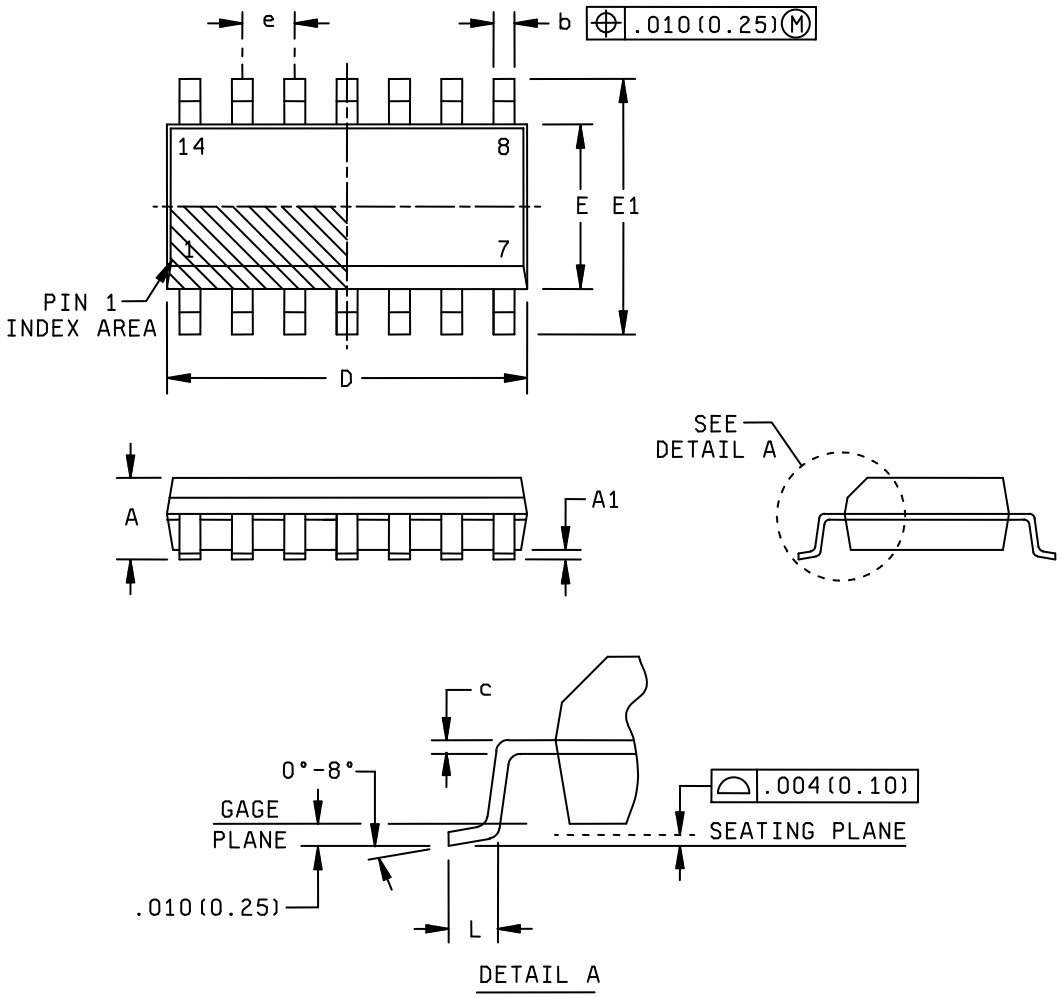

FIGURE 1. Case outline.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/09616
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Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.069	---	1.75
A1	.004	.010	0.10	0.25
b	.012	.020	0.31	0.51
c	.005	.010	0.13	0.25
D	.337	.344	8.55	8.75
e	.050 BSC		1.27 BSC	
E	.150	.157	3.80	4.00
E1	.228	.244	5.80	6.20
L	.016	.050	0.40	1.27
n	14 leads		14 leads	

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) per side.
4. Falls within JEDEC MS-012 variation AB.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	IN 0	Device input 0
2	GND	Ground
3	IN 1	Device input 1
4	GND	Ground
5	IN 2	Device input 2
6	$-V_S$	Negative supply voltage
7	IN 3	Device input 3
8	A0	Channel control pin 0
9	A1	Channel control pin 1
10	$\overline{EN}$	Chip enable
11	SD	Shutdown
12	FB	Feedback
13	OUT	Device output
14	$+V_S$	Positive supply voltage

FIGURE 2. Terminal connections.

A0	A1	$\overline{EN}$	SD	V_{OUT}
0	0	0	0	INPUT 0
1	0	0	0	INPUT 1
0	1	0	0	INPUT 2
1	1	0	0	INPUT 3
X	X	1	0	High Z, I_Q = 3.4 mA
X	X	X	1	High Z, I_Q = 1.1 mA

FIGURE 3. Truth table.

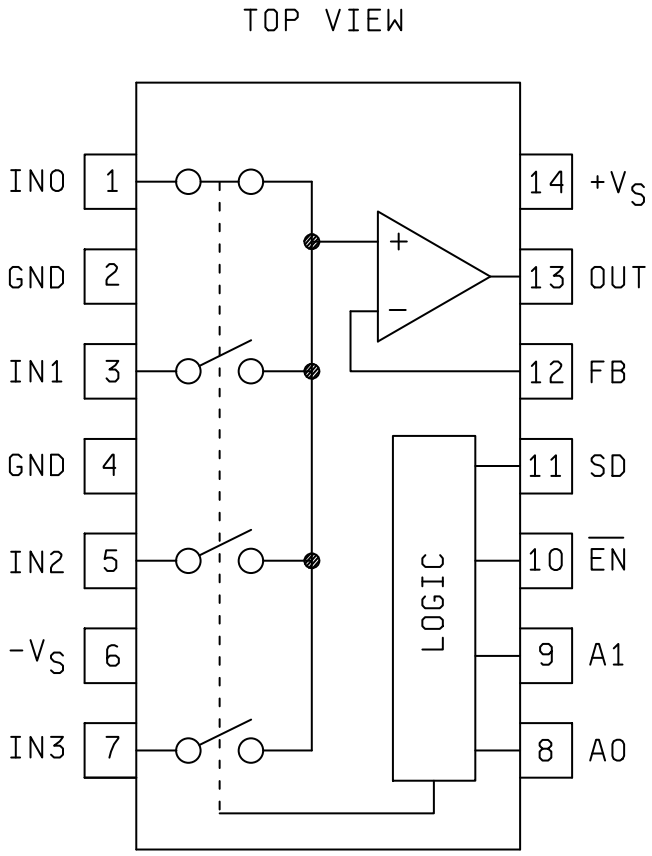

FIGURE 4. Logic diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number 1/ 2/	Device manufacturer CAGE code	Package marking 3/	Transport media, quantity	Vendor part number
V62/09616-01XE	01295	OPA4872M	Tape and reel, 2500	OPA4872MDREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet , or use website www.ti.com.

3/ Package drawings, standard packaging quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available at www.ti.com/sc/package.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493