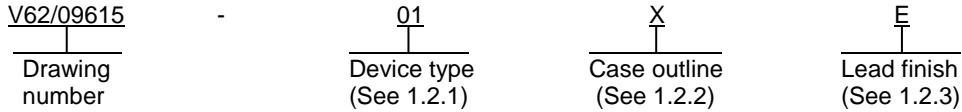


1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 8 bit dual supply bus transceiver with configurable voltage translation and 3-state outputs microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74LVC8T245-EP	8-bit dual supply bus transceiver with configurable voltage translation and 3-state outputs.

1.2.2 Case outline(s). The case outlines shall be as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	24	JEDEC MO-153	Plastic small outline package.
Y	24	JEDEC MS-013	Plastic small outline package.
Z	24	JEDEC MO-241	Quad Flat pack No-Lead (QFN) package.

1.2.3 Lead finishes. The lead finishes shall be as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range, (V _{CCA} , V _{CCB})	-0.5 V to +6.5 V
Input voltage range, (V _i):	
I/O ports (A port)	-0.5 V to +6.5 V 2/
I/O ports (B port)	-0.5 V to +6.5 V 2/
Control inputs	-0.5 V to +6.5 V 2/
Voltage range applied to any output in the high impedance or power-off stage, (V _o):	
A port	-0.5 V to +6.5 V 2/
B port	-0.5 V to +6.5 V 2/
Voltage range applied to any output in the high or slow state, (V _o):	
A port	-0.5 V to V _{CCA} + 0.5 2/ 3/
B port	-0.5 V to V _{CCB} + 0.5 2/ 3/
Maximum Input clamp current, (I _{IK}) (V _i < 0)	-50 mA
Maximum Output clamp current, (I _{OK}) (V _o < 0)	-50 mA
Maximum Continuous output current, (I _o)	±50 mA
Maximum Continuous current through V _{CC} or GND	±100 mA
Maximum Package thermal impedance (θ _{JA})	88°C/W 4/
Storage temperature range, (T _{STG})	-65°C to +150°C

1.4 ESD Ratings.

Electrostatic discharge:

Human Body model (HBM), per ANSI/ESDA/JEDEC JS-001	±4000 V 5/
Charged-device model (CDM), per JEDEC specification JESD22-C101	±1000 V 6/
Machine model.....	±200 V

-
- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ The input and output negative voltage ratings may exceeded if the input and output current ratings are observed.
- 3/ The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed..
- 4/ The package thermal impedance is calculated in accordance with JESD 51-7.
- 5/ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- 6/ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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1.5 Recommended operating conditions. 7/ 8/ 9/ 10/

		V _{CCI}	V _{CCO}	Min	Max	Unit
Supply voltage, (V _{CC})	V _{CCA}			1.65	5.5	V
	V _{CCB}			1.65	5.5	
High level input voltage, (V _{IH})	Data inputs 11/	1.65 V to 1.95 V		0.65 x V _{CCI}		
		2.3 V to 2.7 V		1.7		
		3.0 V to 3.6 V		2		
		4.5 V to 5.5 V		0.7 x V _{CCI}		
Low level input voltage, (V _{IL})	Data inputs 11/	1.65 V to 1.95 V			0.35 x V _{CCI}	
		2.3 V to 2.7 V			0.7	
		3.0 V to 3.6 V			0.8	
		4.5 V to 5.5 V			0.3 x V _{CCI}	
High level input voltage, (V _{IH})	Control inputs 12/ referenced to V _{CCA}	1.65 V to 1.95 V		0.65 x V _{CCA}		V
		2.3 V to 2.7 V		1.7		
		3.0 V to 3.6 V		2		
		4.5 V to 5.5 V		0.7 x V _{CCA}		
Low level input voltage, (V _{IL})	Control inputs 12/ referenced to V _{CCA}	1.65 V to 1.95 V			0.35 x V _{CCA}	
		2.3 V to 2.7 V			0.7	
		3.0 V to 3.6 V			0.8	
		4.5 V to 5.5 V			0.3 x V _{CCA}	
Input voltage, (V _I)	Control inputs			0	5.5	
Input/Output voltage, (V _{I/O})	Active state			0	V _{CCO}	
	3-state			0	5.5	
High level output current, (I _{OH})			1.65 V to 1.95 V		-4	mA
			2.3 V to 2.7 V		-8	
			3.0 V to 3.6 V		-24	
			4.5 V to 5.5 V		-32	
Low level output current, (I _{OL})			1.65 V to 1.95 V		4	
			2.3 V to 2.7 V		8	
			3.0 V to 3.6 V		24	
			4.5 V to 5.5 V		32	
Input transition rise or fall rate, Δt/Δv	Data inputs	1.65 V to 1.95 V			20	ns/V
		2.3 V to 2.7 V			20	
		3.0 V to 3.6 V			10	
		4.5 V to 5.5 V			5	
Operating free air temperature, T _A				-55	125	°C

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1.6 Thermal characteristics.

Thermal metric <u>13/</u>	Case outline X	Case outline Y	Case outline Z	Units
Junction to ambient thermal resistance, $R_{\theta JA}$	90.6	68.1	36.2	°C/W
Junction to case (top) thermal resistance, $R_{\theta JCtop}$	27.6	35.6	27.9	
Junction to board thermal resistance, $R_{\theta JB}$	45.3	37.8	13.15	
Junction to top characterization parameter, Ψ_{JT}	1.3	13	9.5	
Junction to board characterization parameter, Ψ_{JB}	44.8	37.5	13.4	
Junction to case (bottom) thermal resistance, $R_{\theta JCbot}$	N/A	N/A	3.6	

7/ V_{CCI} is the V_{CC} associated with the data input port.

8/ V_{CCO} is the V_{CC} associated with the output port.

9/ All unused or driven (floating) data inputs (I/Os) of the device must be held at logic HIGH or LOW (preferably V_{CCI} or GND) to ensure proper device operation and minimized power. Refer to manufacturer for more information.

10/ All unused control inputs must be held at V_{CCA} or GND to ensure proper device operation and minimize power consumption.

11/ For V_{CCI} values not specified in the data sheet, $V_{IH\ min} = V_{CCI} \times 0.7$, $V_{IL\ max} = V_{CCI} \times 0.3\ V$.

12/ For V_{CCA} values not specified in the data sheet, $V_{IH\ min} = V_{CCA} \times 0.7$, $V_{IL\ max} = V_{CCA} \times 0.3\ V$.

13/ For more information about traditional and new thermal metrics, see manufacturer data *IC Package Thermal Metrics* application report, SPRA953.

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2. APPLICABLE DOCUMENTS

- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices.
- JEDEC JS-001 – Joint JEDEC/ESDA standard for electrostatic discharge sensitivity test – Human Body Model (HBM)
- JESD22-C101 – Field-Induced Charged-Device Model (FIDCM) Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
- JEP155 – Recommended ESD target levels for HBM/MM qualification.
- JEP157 – Recommended ESD-CDM target levels.

(Applications for copies should be addressed to the Electronic Industry Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or at <http://www.jedec.org>)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Function table. The function table shall be as shown in figure 4.

3.5.5 Load circuit and voltage waveforms. The load circuit and timing waveforms shall be as specified in figure 5.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ 3/ 4/ unless otherwise specified	V _{CCA}	V _{CCB}	Limits		Unit	
					Min	Max		
High level output voltage	V _{OH}	V _I = V _{IH} , I _{OH} = -100 μA	1.65 V to 4.5 V	1.65 V to 4.5 V	V _{CCO} -0.1		V	
		V _I = V _{IH} , I _{OH} = -4 mA	1.65 V	1.65 V	1.2			
		V _I = V _{IH} , I _{OH} = -8 mA	2.3 V	2.3 V	1.9			
		V _I = V _{IH} , I _{OH} = -24 mA	3 V	3 V	2.4			
		V _I = V _{IH} , I _{OH} = -32 mA	4.5 V	4.5 V	3.8			
Low level output voltage	V _{OL}	V _I = V _{IL} , I _{OL} = 100 μA	1.65 V to 4.5 V			0.1	V	
		V _I = V _{IL} , I _{OL} = 4 mA	1.65 V			0.45		
		V _I = V _{IL} , I _{OL} = 8 mA	2.3 V			0.3		
		V _I = V _{IL} , I _{OL} = 24 mA	3 V			0.55		
		V _I = V _{IL} , I _{OL} = 32 mA	4.5 V			0.55		
Input current	DIR	I _I	V _I = V _{CCA} or GND	1.65 V to 5.5 V	1.65 V to 5.5 V	-2	2	μA
		V _I = V _{CCA} or GND, T _A = 25°C	1.65 V to 5.5 V	1.65 V to 5.5 V	-1	1		
Input/Output power off leakage current	A or B port	I _{off}	V _I or V _O = 0 to 5.5 V	0 V	0 to 5.5 V	-11	11	μA
				0 to 5.5 V	0 V	-11	11	
		V _I or V _O = 0 to 5.5 V, T _A = 25°C	0 V	0 to 5.5 V	-1	1		
			0 to 5.5 V	0 V	-1	1		
High impedance state output current	A or B port	I _{oz}	V _O = V _{CCO} or GND, $\overline{OE} = V_{IH}$	1.65 V to 5.5 V	1.65 V to 5.5 V	-6	6	μA
			V _O = V _{CCO} or GND, $\overline{OE} = V_{IH}$, T _A = 25°C	1.65 V to 5.5 V	1.65 V to 5.5 V	-1	1	
Quiescent supply current	I _{CCA}	V _I = V _{CCI} or GND, I _O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V		20	μA	
			5 V	0 V		20		
			0 V	5 V		-10		
	I _{CCB}	V _I = V _{CCI} or GND, I _O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V		20	μA	
			5 V	0 V		-10		
			0 V	5 V		20		
I _{CCA} + I _{CCB}	V _I = V _{CCI} or GND, I _O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V		40	μA		
Quiescent supply current delta	A port	ΔI _{CCA}	One A port at V _{CCA} - 0.6 V DIR at V _{CCA} , B port = open	3 V to 5.5 V	3 V to 5.5 V		50	μA
	DIR		DIR at V _{CCA} - 0.6 V, B port = open, A port at V _{CCA} or GND	3 V to 5.5 V	3 V to 5.5 V		50	
	B port	ΔI _{CCB}	One B port at V _{CCB} - 0.6 V, DIR at GND, A port = open	3 V to 5.5 V	3 V to 5.5 V		50	μA
Input capacitance	Control inputs	C _i	V _I = V _{CCA} or GND	3.3 V	3.3 V		5	pF
			V _I = V _{CCA} or GND, T _A = 25°C	3.3 V	3.3 V	4 TYP		
Input/Output capacitance	A or B port	C _{io}	V _O = V _{CCA/B} or GND	3.3 V	3.3 V		10	
			V _O = V _{CCA/B} or GND, T _A = 25°C	3.3 V	3.3 V	8.5 TYP		

See footnote at end of the table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 2/ unless otherwise specified	V _{CCB} = 1.8 V ±0.15 V		V _{CCB} = 2.5 V ±0.2 V		V _{CCB} = 3.3 V ±0.3 V		V _{CCB} = 5 V ±0.5 V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Switching characteristics, V_{CCA} = 1.8 V ±0.15 V											
Propagation delay time, from input A to output B	t _{PLH}		1.7	25.9	1.3	13.2	1	11.4	0.8	11.1	ns
	t _{PHL}										
Propagation delay time, from input B to output A	t _{PLH}		0.9	28.8	0.8	27.6	0.7	27.4	0.7	27.4	
	t _{PHL}										
Disable time, from input \overline{OE} to output A	t _{PHZ}		1.5	33.6	1.5	33.4	1.5	33.3	1.4	33.2	
	t _{PLZ}										
Disable time, from input \overline{OE} to output B	t _{PHZ}		2.4	36.2	1.9	17.1	1.7	16	1.3	14.3	
	t _{PLZ}										
Enable time, from input \overline{OE} to output A	t _{PZH}		0.4	28	0.4	27.8	0.4	27.7	0.4	27.7	
	t _{PZL}										
Enable time, from input \overline{OE} to output B	t _{PZH}		1.8	40	1.5	20	1.2	16.6	0.9	14.8	
	t _{PZL}										
Switching characteristics, V_{CCA} = 2.5 V ±0.2 V											
Propagation delay time, from input A to output B	t _{PLH}		1.5	25.4	1.2	13	0.8	10.2	0.6	8.8	ns
	t _{PHL}										
Propagation delay time, from input B to output A	t _{PLH}		1.2	13.3	1	13.1	1	12.9	0.9	12.8	
	t _{PHL}										
Disable time, from input \overline{OE} to output A	t _{PHZ}		1.4	13	1.4	13	1.4	13	1.4	13	
	t _{PLZ}										
Disable time, from input \overline{OE} to output B	t _{PHZ}		2.3	33.6	1.8	15	1.7	14.3	0.9	10.9	
	t _{PLZ}										
Enable time, from input \overline{OE} to output A	t _{PZH}		1	17.2	1	17.3	1	17.2	1	17.3	
	t _{PZL}										
Enable time, from input \overline{OE} to output B	t _{PZH}		1.7	32.2	1.5	18.1	1.2	14.1	1	11.2	
	t _{PZL}										

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 2/ unless otherwise specified	V _{CCB} = 1.8 V ±0.15 V		V _{CCB} = 2.5 V ±0.2 V		V _{CCB} = 3.3 V ±0.3 V		V _{CCB} = 5 V ±0.5 V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Switching characteristics, V_{CCA} = 3.3 V ±0.3 V											
Propagation delay time, from input A to output B	t _{PLH}		1.5	25.2	1.1	12.8	0.8	10.3	0.5	10.4	ns
	t _{PHL}										
Propagation delay time, from input B to output A	t _{PLH}		0.8	11.2	0.8	10.2	0.7	10.1	0.6	10	
	t _{PHL}										
Disable time, from input OE to output A	t _{PHZ}		1.6	12.2	1.6	12.2	1.6	12.2	1.6	12.2	
	t _{PLZ}										
Disable time, from input OE to output B	t _{PHZ}		2.1	33	1.7	14.3	1.5	12.6	0.8	10.3	
	t _{PLZ}										
Enable time, from input OE to output A	t _{PZH}		0.8	14.1	0.8	13.6	0.8	13.2	0.8	13.6	
	t _{PZL}										
Enable time, from input OE to output B	t _{PZH}	1.8	31.7	1.4	18.4	1.1	12.9	0.9	10.9		
	t _{PZL}										
Switching characteristics, V_{CCA} = 5 V ±0.5 V											
Propagation delay time, from input A to output B	t _{PLH}		1.5	25.4	1	12.8	0.7	10	0.4	8.2	ns
	t _{PHL}										
Propagation delay time, from input B to output A	t _{PLH}		0.7	11	0.4	8.8	0.3	8.5	0.3	8.3	
	t _{PHL}										
Disable time, from input OE to output A	t _{PHZ}		0.3	9.4	0.3	9.4	0.3	9.4	0.3	9.4	
	t _{PLZ}										
Disable time, from input OE to output B	t _{PHZ}		2	32.7	1.6	13.7	1.4	12	0.7	9.7	
	t _{PLZ}										
Enable time, from input OE to output A	t _{PZH}		0.7	10.9	0.7	10.9	0.7	10.9	0.7	10.9	
	t _{PZL}										
Enable time, from input OE to output B	t _{PZH}	1.5	31.6	1.3	18.4	1	13.7	0.9	10.7		
	t _{PZL}										

Test	Symbol	Conditions T _A = 25°C unless otherwise specified	V _{CCA} = V _{CCB} = 1.8 V	V _{CCA} = V _{CCB} = 2.5 V	V _{CCA} = V _{CCB} = 3.3 V	V _{CCA} = V _{CCB} = 5 V	Unit
			TYP	TYP	TYP	TYP	
Operating Characteristics							
A port input, B port output	C _{pdA} 5/		2	2	2	3	pF
B port input, A port output			12	13	13	16	
A port input, B port output	C _{pdB} 5/		13	13	14	16	
B port input, A port output			2	2	2	3	

See footnote at end of table.

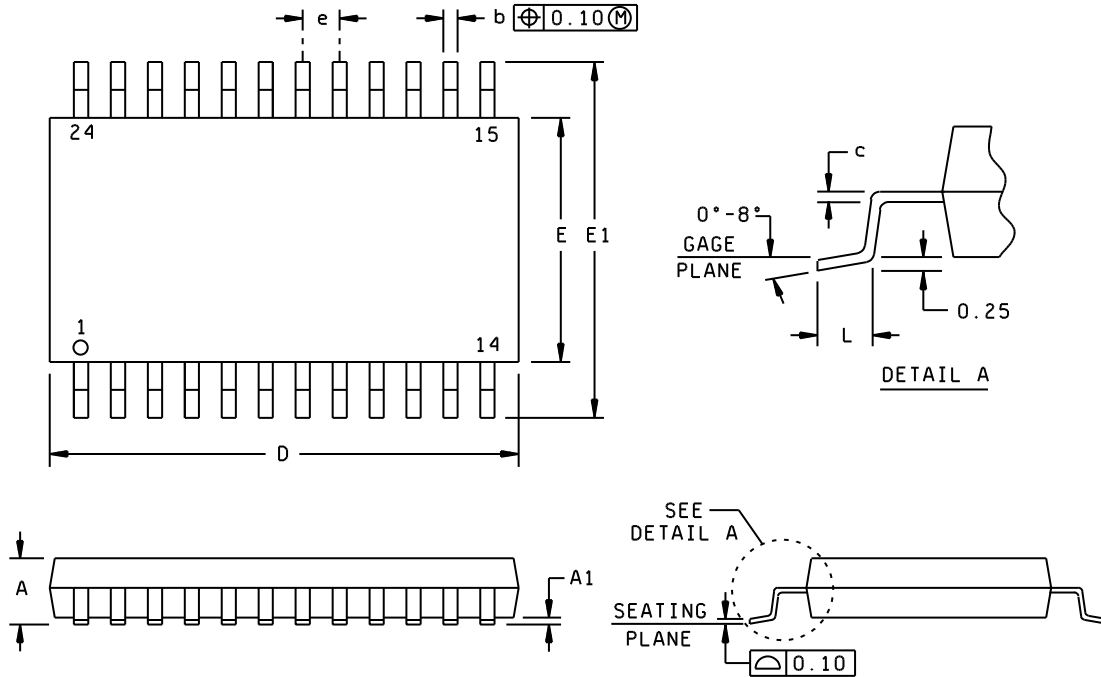
DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/09615
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TABLE I. Electrical performance characteristics - Continued.

1. Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2. Over recommended operating free air temperature range, $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$.
3. V_{CCO} is the V_{CC} associated with the output port.
4. V_{CCI} is the V_{CC} associated with the input port.
5. Power dissipation capacitance per transceiver.

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Case X



Dimensions					
Symbol	Min	Max	Symbol	Min	Max
A		1.20	e	0.65 BSC	
A1	0.05	0.15	E	4.30	4.50
b	0.19	0.30	E1	6.20	6.60
c	0.15 NOM		L	0.50	0.75
D	7.70	7.90			

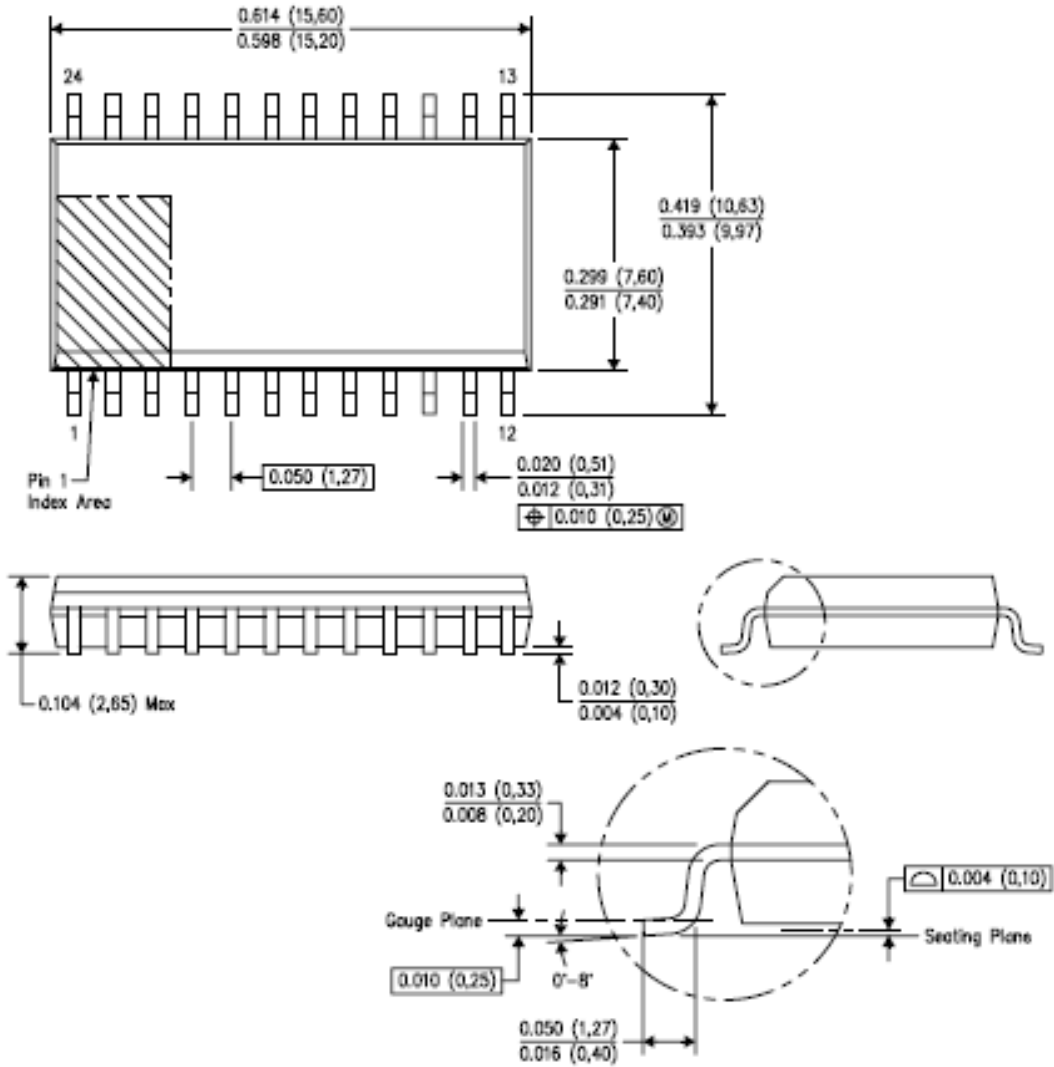
Notes:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion not to exceed 0.15.
4. Fall within JEDEC MO-153.

FIGURE 1. Case outlines.

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Case outline Y



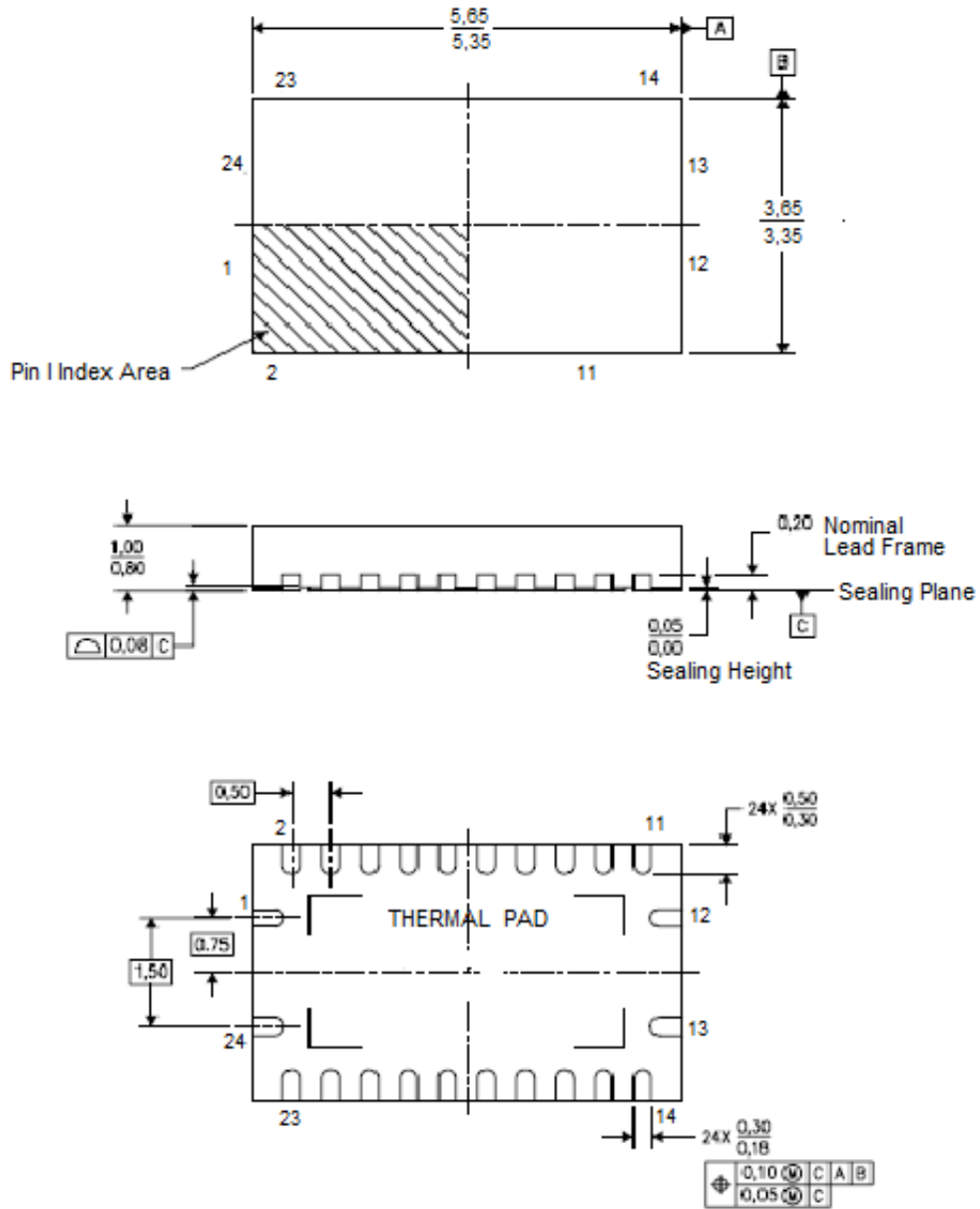
Notes:

1. All linear dimensions are in inches (millimeters).
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
4. Fall within JEDEC MS-013 variation AD.

FIGURE 1. Case outlines - Continued.

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Case outline Z



Notes:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the board for thermal and mechanical performance..
4. Fall within JEDEC MO-241.

FIGURE 1. Case outlines- Continued.

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Pin No.	Signal name	Pin No.	Signal name
1	V _{CCA}	13	GND
2	DIR	14	B8
3	A1	15	B7
4	A2	16	B6
5	A3	17	B5
6	A4	18	B4
7	A5	19	B3
8	A6	20	B2
9	A7	21	B1
10	A8	22	\overline{OE}
11	GND	23	V _{CCB}
12	GND	24	V _{CCB}

FIGURE 2. Terminal connections.

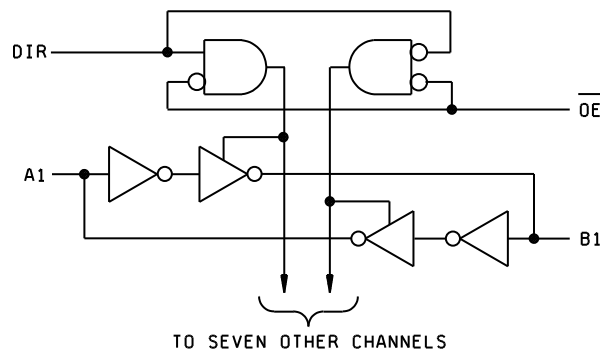
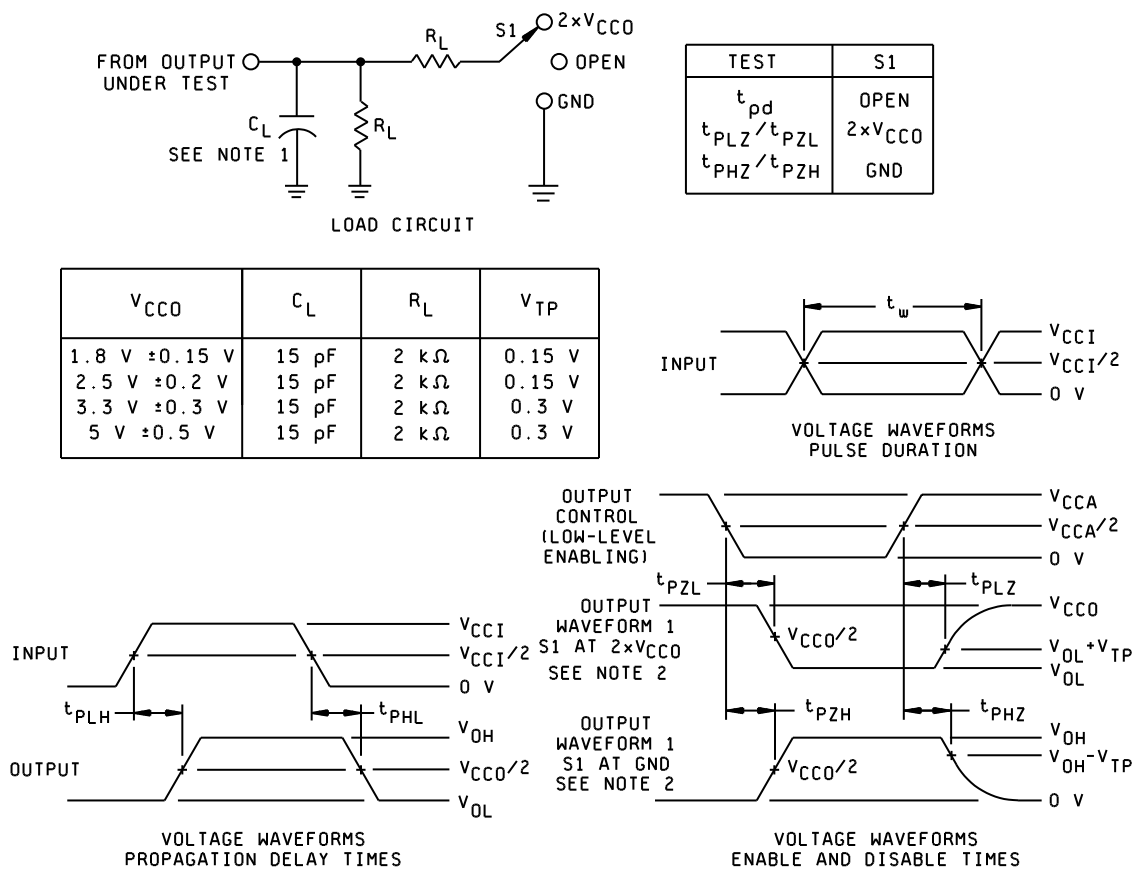


FIGURE 3. Logic diagram.

Control Inputs		Output circuits		Operation
\overline{OE}	DIR	A Port	B Port	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

FIGURE 4. Function Table

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Notes:

1. C_L includes probe and test fixture capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having following characteristics: $PRR \leq 10$ MHz, $Z_o = 50 \Omega$, $dv/dt \geq 1$ V/ns.
4. The outputs are measured one at a time with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same t_{dis} .
6. t_{PZL} and t_{PZH} are the same t_{en} .
7. t_{PLH} and t_{PHL} are the same t_{pd} .
8. V_{CCI} is the V_{CC} associated with the input port.
9. V_{CC0} is the V_{CC} associated with the input port
10. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and voltage waveforms.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/09615-01XE	01295	SN74LVC8T245MPWREP	NH245MEP
V62/09615-01YE	01295	SN74LVC8T245MDWREP	LVC8T245M
V62/09615-01ZE	01295	CLVC8T245MRHLTEP	P8T245M

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest Lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

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