REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add conditions to the Power supply quiescent current test under Table I. Update document paragraphs to current requirements. - ro	17-04-25	C. SAFFLE
B	Make correction to note 4 as specified under Figure 1. Add quantity information to paragraph 6.3. Update document paragraphs to current requirements. - ro	22-05-11	J. ESCHMEYER

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	B	B	B	B	B	B	B	B	B	B	B	B										
SHEET	1	2	3	4	5	6	7	8	9	10	11	12										

PMIC N/A

Original date of drawing
YY-MM-DD
09-01-27

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COLUMBUS, OHIO 43218-3990
https://www.dla.mil/landandmaritime

TITLE
MICROCIRCUIT, LINEAR, DIFFERENTIAL AMPLIFIER, MONOLITHIC SILICON

SIZE	CAGE CODE
A	16236

DWG NO. V62/09613

REV B

PAGE 1 OF 12

AMSC N/A

5962-V061-22

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance differential amplifier microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/09613	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	INA159-EP	Differential amplifier

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	M0-187-AA	Plastic surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{CC})	+5.5 V
Signal input terminals (-IN and +IN), voltage	±30 V
Reference (REF 1 and REF 2) and series pins:	
Current	±10 mA
Voltage	$-V_{CC}$ – 0.5 to $+V_{CC}$ + 0.5 V
Output short circuit (I_{OS})	Continuous
Storage temperature range (T_{STG})	-65°C to +150°C
Junction temperature range (T_J)	+150°C
Power dissipation (P_D)	833.33 mW
Thermal resistance, junction to ambient (θ_{JA})	150°C/W
Thermal resistance, junction to case (θ_{JC})	78.495°C/W
Electrostatic discharge (ESD) rating:	
Human body model (HBM)	4000 V
Charged device model (CDM)	1000 V

1.4 Recommended operating conditions. 2/

Operating free-air temperature range (T_A)	-55°C to +125°C

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1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Test circuit for reference divider accuracy. The test circuit for reference divider accuracy shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Initial offset voltage 3/	V_{OS}	V_S = ±2.5 V, reference and input pin grounded	+25°C	01		±500	µV
			-55°C to +125°C			±1450	
Power supply rejection ratio	PSRR	V_S = ±0.9 V to ±2.75 V	+25°C	01		±100	µV/V
			-55°C to +125°C			±200	
Reference divider 4/ accuracy			+25°C	01		±0.024	%
			-55°C to +125°C			±0.050	
Differential input 5/ impedance	Z_{DIN}		+25°C	01	240 typical		kΩ
Common mode 5/ input impedance	Z_{CM}		+25°C	01	60 typical		kΩ
Common mode voltage range	+V_{CM}		+25°C	01	17.5 typical		V
	-V_{CM}				-12.5 typical		
Common mode rejection ratio	CMRR	V_{CM} = -10 V to +10 V, R_S = 0 Ω	+25°C	01	80		dB
			-55°C to +125°C		74		
Output voltage 6/ noise		f = 0.1 Hz to 10 Hz	-55°C to +125°C	01	10 typical		µVPP
		f = 10 kHz			30 typical		nV / $\sqrt{Hz}$
Initial gain	Gi	V_{REF2} = 4.096 V, R_L connected to GND, +V_{IN} – (-V_{IN}) = -10 V to +10 V, V_{CM} = 0 V	+25°C	01	0.2 typical		V/V
Gain error	Ge	V_{REF2} = 4.096 V, R_L connected to GND, +V_{IN} – (-V_{IN}) = -10 V to +10 V, V_{CM} = 0 V	+25°C	01		±0.024	%
			-55°C to +125°C			±0.035	
Nonlinearity gain	Gn	V_{REF2} = 4.096 V, V_{CM} = 0 V, R_L connected to GND, +V_{IN} – (-V_{IN}) = -10 V to +10 V	+25°C	01	±0.0002 typical		% of FS

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Positive output voltage	$+V_{OUT}$	V_{REF2} = 4.096 V,	+25°C	01	+V – 0.1		V
		R_L connected to GND	-55°C to +125°C		+V - 0.2		
Negative output voltage	$-V_{OUT}$	V_{REF2} = 4.096 V,	+25°C	01	-V + 0.048		V
		R_L connected to GND	-55°C to +125°C		-V + 0.070		
Current limit, continuous to common			+25°C	01	±60 typical		mA
Capacitive load	C_L	See figure 4		01			pF
Open loop output impedance	R_O	f = 1 MHz, I_O = 0	+25°C	01	110 typical		Ω
Small signal bandwidth	SSBW	-3 dB	+25°C	01	1.5 typical		MHz
Slew rate	SR		+25°C	01	15 typical		V/μs
Settling time, 0.01 %	t_S	4 V output step, C_L = 100 pF	+25°C	01	1 typical		μs
Overload recovery time		50% overdrive	+25°C	01	250 typical		ns
Power supply specified voltage range	V_S		-55°C to +125°C	01		+5	V
Power supply operating voltage range			-55°C to +125°C	01	+1.8	+5.5	V
Power supply quiescent current	I_Q	I_O = 0 mA, V_S = ±2.5 V, reference and input pins grounded	+25°C	01		1.5	mA
			-55°C to +125°C			2.0	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, at T_A = +25°C, R_L = 10 kΩ connected to V_S/2, REF 1 pin connected to ground, and REF 2 pin connected to V_{REF} = 5 V.

3/ Includes effects of amplifier input bias and offset currents.

4/ Reference divider accuracy specifies the match between the reference divider resistor using figure 3.

5/ Internal resistors are ratio matched but have 20% absolute value.

6/ Includes effect of amplifier input current noise and terminal noise contribution of resistor network.

Case X

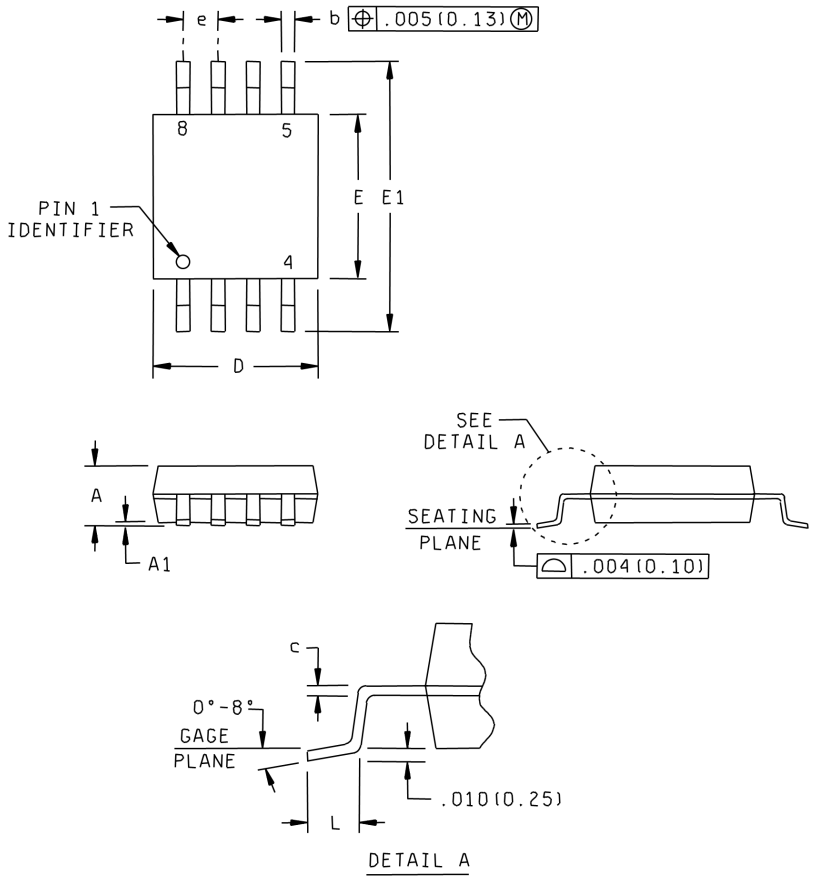


FIGURE 1. Case outline.

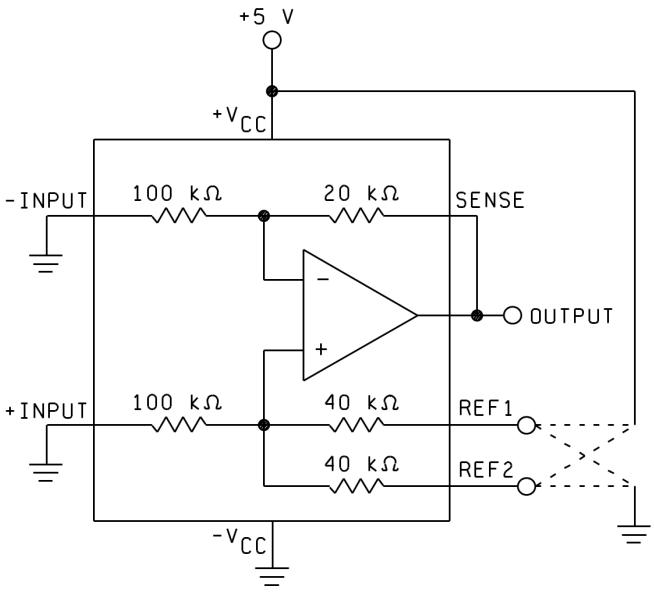
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.043	---	1.10
A1	0.001	0.006	0.05	0.15
b	0.010	0.014	0.25	0.38
c	0.005	0.009	0.13	0.23
D	0.114	0.122	2.90	3.10
E	0.114	0.122	2.90	3.10
E1	0.187	0.199	4.75	5.05
e	0.026 BSC		0.65 BSC	
L	0.015	0.027	0.40	0.70

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Reference dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.15 mm (0.006 inch) per end.
3. Reference dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.50 mm (0.019 inch) per side.
4. Falls with JEDEC MO-187-AA, except interlead flash.

FIGURE 1. Case outline - Continued.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	REF 1
2	-INPUT
3	+INPUT
4	$-V_{CC}$
5	SENSE
6	OUTPUT
7	$+V_{CC}$
8	REF 2

FIGURE 2. Terminal connections.



NOTE: The test is performed by measuring the output with the reference applied to alternate reference resistors, and calculating a result such that the amplifier offset is cancelled in the final measurement.

FIGURE 3. Test circuit for reference divider accuracy.

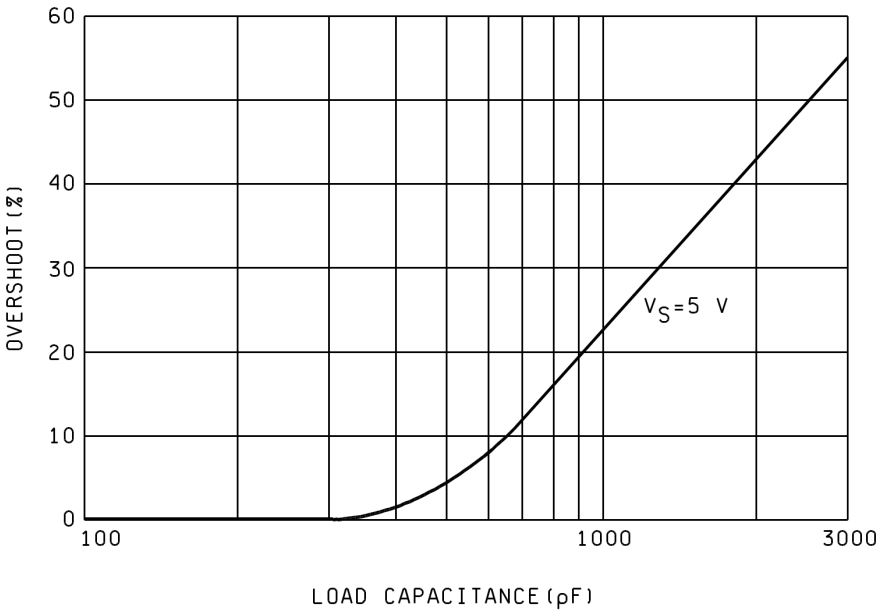


Figure 4. Small signal overshoot versus load capacitance.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/ 2/	Device manufacturer CAGE code	Mode of transportation and quantity 3/	Package designator	Top side marking	Vendor part number
V62/09613-01XE	01295	Tape and reel, 250 units	DGK	OAA	INA159AMDGKTEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet, or contact the manufacturer.

3/ Package drawings, standard packaging quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available from the manufacturer.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243