REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add JEDEC references under section 2. Update document paragraphs to current requirements. - ro	15-10-20	C. SAFFLE
B	Update document paragraphs to current requirements. - ro	20-09-23	J. ESCHMEYER

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV	B	B	B	B	B	B															
PAGE	18	19	20	21	22	23															

REV STATUS OF PAGES	**REV**	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 09-01-13	**CHECKED BY** RAJESH PITHADIA	**TITLE** MICROCIRCUIT, DIGITAL, CONTROLLER AREA NETWORK (CAN) TRANSCEIVER, MONOLITHIC SILICON
	APPROVED BY ROBERT M. HEBER	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/09611**
	REV **B**	**PAGE** 1 **OF** 23

AMSC N/A

5962-V072-20

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a controller area network (CAN) transceiver microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/09611	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN65HVD233-EP	Controller area network (CAN) transceiver

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MS-012-AA	Plastic surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC})	-0.3 V to 7.0 V
Voltage range at any bus terminal (CANH or CANL)	-36 V to +36 V
Voltage input range, transient pulse, CANH and CANL, through 100 Ω (see figure 5)	-100 V to +100 V
Input voltage range (V_I) (D, R, R_S, LBK)	-0.5 V to 7.0 V
Receiver output current (I_O)	-10 mA to 10 mA
Electrostatic discharge (ESD):	
Human body model (HBM): 3/	
CANH, CANL and GND	16 kV
All pins	3 kV
Charged device model (CDM): 4/	
All pins	1 kV
Continuous total power dissipation	See 1.5, dissipation rating table
Operating junction temperature (T_J)	+150°C
Storage temperature range (T_{STG})	-65°C to 150°C
Lead temperature 1.6 mm from case for 10 seconds	+260°C
Thermal resistance, junction to ambient (θ_{JA}): 5/	
Low – K, no air flow	185°C/W 6/
High – K, no air flow	101°C/W 7/
Thermal resistance, junction to board (θ_{JB}):	
High – K, no air flow	82.8°C/W 7/
Thermal resistance, junction to case (θ_{JC})	26.5°C/W
Average power dissipation (P_{AVG}) :	
With R_L = 60 Ω, R_S at 0 V, input to D a 1 MHz 50% duty cycle square wave,	
V_{CC} at 3.3 V and T_A = +25°C	36.4 mW
Thermal shutdown junction temperature (T_{SD})	170°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
3/ Tested in accordance with JEDEC Standard 22, test method A114-A.
4/ Tested in accordance with JEDEC Standard 22, test method C101
5/ See manufacturer’s literature number SZZA003 for an explanation of this parameter.
6/ JESD51-3 low effective thermal conductivity test board for leaded surface mount packages.
7/ JESD51-7 high effective thermal conductivity test board for leaded surface mount packages.

1.4 Recommended operating conditions. 8/

Supply voltage range (V_{CC}): ..... 3.0 V to 3.6 V
Voltage at any bus terminal (separately or common mode) ..... -7.0 to 12.0 V
High level input voltage, (V_{IH}) D, LBK pins ..... 2.0 V to 5.5 V
Low level input voltage (V_{IL}), D, LBK pins ..... 0 V to 0.8 V
Differential input voltage, (V_{ID}) ..... -6.0 V to 6.0 V
Resistance from R_S to ground ..... 0.0 kΩ to 100 kΩ
Input voltage at R_S for standby ..... 0.75 V_{CC} to 5.5 V
High level output current, (I_{OH}):
Driver ..... -50 mA minimum
Receiver ..... -10 mA minimum
Low level output current, (I_{OL}):
Driver ..... 50 mA maximum
Receiver ..... 10 mA maximum
Operating junction temperature (T_J) ..... +150°C
Operating free-air temperature range (T_A) ..... -55°C to +125°C 9/

1.5. Dissipation rating table.

Case outline	Circuit board	$T_A \leq 25°C$ power rating	Derating factor 10/ above $T_A = 25°C$	$T_A = 85°C$ power rating	$T_A = 125°C$ power rating
X	Low K	596.6 mW	5.7 mW/°C	255.7 mW	28.4 mW
	High K	1076.9 mW	10.3 mW/°C	461.5 mW	51.3 mW

———

8/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
9/ Maximum free air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.
10/ This is the inverse of the junction to ambient thermal resistance when board mounted and with no air flow.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JESD 22-C101	-	Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronics Components
JESD 22-A114	-	Electrostatic Discharge Sensitivity Testing Human Body Model (HBM)
EIA/JEDEC 51-3	-	Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
EIA/JEDEC 51-7	-	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JEDEC PUB 95	-	Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional tables. The functional tables shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figures 5 through 14.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver electrical characteristics.							
Bus output voltage (Dominant)	$V_{O(D)}$	CANH pin, D = 0 V, R_S = 0 V, see figures 6 and 7	-55°C to +125°C	01	2.45	V_{CC}	V
		CANL pin, D = 0 V, R_S = 0 V, see figures 6 and 7			0.5	1.25	
Bus output voltage (Recessive)	V_O	CANH pin, D = 3 V, R_S = 0 V, see figures 6 and 7	+25°C	01	2.3 typical		V
		CANL pin, D = 3 V, R_S = 0 V, see figures 6 and 7			2.3 typical		
Differential output voltage (Dominant)	$V_{OD(D)}$	D = 0 V, R_S = 0 V, see figures 6 and 7	-55°C to +125°C	01	1.5	3	V
		D = 0 V, R_S = 0 V, see figures 7 and 8			1.2	3	
Differential output voltage (Recessive)	V_{OD}	D = 3 V, R_S = 0 V, see figures 6 and 7	-55°C to +125°C	01	-120	12	mV
		D = 3 V, R_S = 0 V, no load			-0.5	0.05	V
Peak to peak common mode output voltage	$V_{OC(PP)}$	V_{CC} = 3.3 V, see figure 9	+25°C	01	1 typical		V
High level input current	I_{IH}	D, LBK pins, D = 2 V	-55°C to +125°C	01	-30	30	µA
Low level input current	I_{IL}	D, LBK pins, D = 0.8 V	-55°C to +125°C	01	-30	30	µA
Short circuit output current	I_{OS}	V_{CANH} = -7 V, CANL open, see figure 10	-55°C to +125°C	01	-250		mA
		V_{CANH} = 12 V, CANL open, see figure 10				1	
		V_{CANL} = -7 V, CANH open, see figure 10			-1		
		V_{CANL} = 12 V, CANH open, see figure 10				250	
Output capacitance	C_O	See receiver input capacitance					

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver electrical characteristics – continued.							
R_S input current for standby	$I_{IRS(S)}$	R_S = 0.75 V_{CC}	-55°C to +125°C	01	-10		µA
Supply current	I_{CC}	Standby, R_S = V_{CC}, D = V_{CC}, LBK = 0 V	-55°C to +125°C	01		600	µA
		Dominant, no load, D = 0 V, LBK = 0 V, R_S = 0 V				6	mA
		Recessive, no load, D = V_{CC}, LBK = 0 V, R_S = 0 V				6	mA
Driver switching characteristics.							
Propagation delay time, low to high level output	t_{PLH}	R_S = 0 V, see figure 11	-55°C to +125°C	01		95	ns
		R_S with 10 kΩ to ground, see figure 11				125	
		R_S with 100 kΩ to ground, see figure 11				870	
Propagation delay time, high to low level output	t_{PHL}	R_S = 0 V, see figure 11	-55°C to +125°C	01		120	ns
		R_S with 10 kΩ to ground, see figure 11				180	
		R_S with 100 kΩ to ground, see figure 11				1200	
Pulse skew 3/ (| t_{PHL} – t_{PLH} |)	$t_{sk(p)}$	R_S = 0 V, see figure 11	-55°C to +125°C	01	35 typical		ns
		R_S with 10 kΩ to ground, see figure 11			60 typical		
		R_S with 100 kΩ to ground, see figure 11			370 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Driver switching characteristics – continued.							
Differential output signal rise time	t_r	R_S = 0 V, see figure 11	-55°C to +125°C	01	20	70	ns
Differential output signal fall time	t_f	R_S = 0 V, see figure 11	-55°C to +125°C	01	20	70	ns
Differential output signal rise time	t_r	R_S with 10 kΩ to ground, see figure 11	-55°C to +125°C	01	30	135	ns
Differential output signal fall time	t_f	R_S with 10 kΩ to ground, see figure 11	-55°C to +125°C	01	30	135	ns
Differential output signal rise time	t_r	R_S with 100 kΩ to ground, see figure 11	-55°C to +125°C	01	300	1400	ns
Differential output signal fall time	t_f	R_S with 100 kΩ to ground, see figure 11	-55°C to +125°C	01	300	1400	ns
Enable time from standby to dominant	$t_{en(s)}$	See figure 12	-55°C to +125°C	01		1.5	µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Receiver electrical characteristics.							
Positive going input threshold voltage 4/	V_{IT+}	LBK = 0 V, see table II	-55°C to +125°C	01		900	mV
Negative going input threshold voltage 4/	V_{IT-}	LBK = 0 V, see table II	-55°C to +125°C	01	500		mV
Hysteresis voltage (V_{IT+} - V_{IT-})	V_{hys}	LBK = 0 V, see table II	+25°C	01	100 typical		mV
High level output voltage	V_{OH}	I_O = -4 mA, see figure 13	-55°C to +125°C	01	2.4		V
Low level output voltage	V_{OL}	I_O = 4 mA, see figure 13	-55°C to +125°C	01		0.4	V
Bus input current	I_I	CANH or CANL = 12 V, Other bus pin = 0, D = 3, LBK = 0 V, R_S = 0 V	-55°C to +125°C	01	150	500	µA
		CANH or CANL = 12 V, Other bus pin = 0, D = 3, LBK = 0 V, R_S = 0 V, V_{CC} = 0 V			200	600	
		CANH or CANL = -7 V, Other bus pin = 0, D = 3, LBK = 0 V, R_S = 0 V			-610	-150	
		CANH or CANL = -7 V, Other bus pin = 0, D = 3, LBK = 0 V, R_S = 0 V, V_{CC} = 0 V			-450	-130	
Input capacitance (CANH or CANL)	C_{IN}	Pin to ground, D = 3 V, LBK = 0 V, V_I = 0.4 sin (4E6πt) + 0.5 V	+25°C	01	40 typical		pF
Differential input capacitance	C_{ID}	Pin to pin, D = 3 V, LBK = 0 V, V_I = 0.4 sin (4E6πt) + 0.5 V	+25°C	01	20 typical		pF
Differential input resistance	R_{ID}	D = 3 V, LBK = 0 V	-55°C to +125°C	01	40	100	kΩ
Input resistance (CANH or CANL)	R_{IN}	D = 3 V, LBK = 0 V	-55°C to +125°C	01	20	50	kΩ

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Receiver electrical characteristics – continued.							
Supply current	I_{CC}	Sleep, D = V_{CC}, R_S = 0 V or V_{CC}	-55°C to +125°C	01		2	µA
		Standby, D = V_{CC}, R_S = V_{CC}, LBK = 0 V				600	
		Dominant, D = 0 V, no load, R_S = 0 V, LBK = 0 V				6	mA
		Recessive, D = V_{CC}, no load, R_S = 0 V, LBK = 0 V				6	
Receiver switching characteristics.							
Propagation delay time, low to high level output	t_{PLH}	See figure 13	-55°C to +125°C	01		60	ns
Propagation delay time, high to low level output	t_{PHL}	See figure 13	-55°C to +125°C	01		60	ns
Pulse skew 3/ ($\lvert t_{PHL} - t_{PLH} \rvert$)	$t_{sk(p)}$	See figure 13	+25°C	01	7 typical		ns
Output signal rise time	t_r	See figure 13	-55°C to +125°C	01		6.5	ns
Output signal fall time	t_f	See figure 13	-55°C to +125°C	01		6.5	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Device switching characteristics.							
Loopback delay, driver input to receiver output	$t_{(LBK)}$	See figure 14	-55°C to +125°C	01		13	ns
Total loop delay, driver input to receiver output, recessive to dominant	$t_{(loop1)}$	R_S = 0 V, see figure 15	-55°C to +125°C	01		135	ns
		R_S with 10 kΩ to ground, see figure 15				190	
		R_S with 100 kΩ to ground, see figure 15				1000	
Total loop delay, driver input to receiver output, dominant to recessive	$t_{(loop2)}$	R_S = 0 V, see figure 15	-55°C to +125°C	01		135	ns
		R_S with 10 kΩ to ground, see figure 15				190	
		R_S with 100 kΩ to ground, see figure 15				1100	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ All typical values are 25°C and with a 3.3 V supply.
3/ Timing parameters are characterized but not production tested.
4/ Characterized but not production tested.

Case X

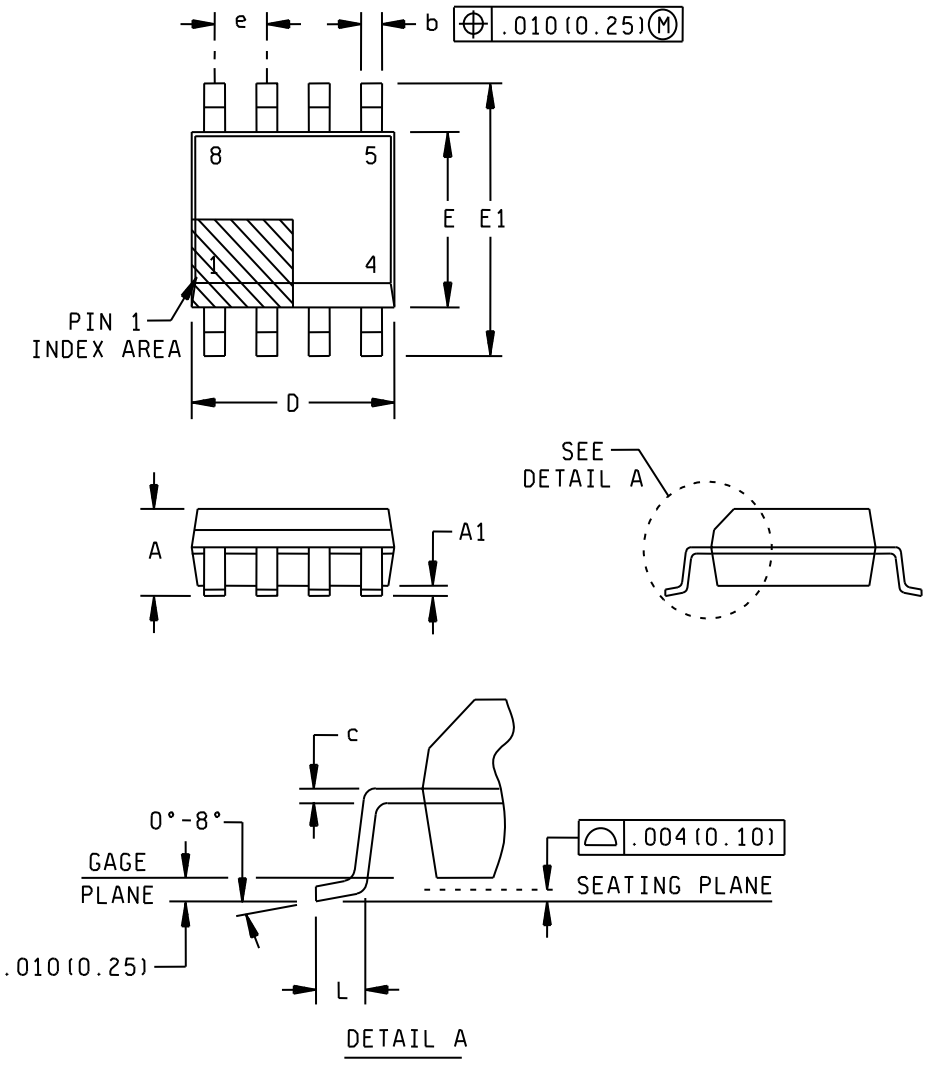


FIGURE 1. Case outline.

Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.069	---	1.75
A1	0.004	0.010	0.10	0.25
b	0.012	0.020	0.31	0.51
c	0.005	0.010	0.13	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
E1	0.228	0.244	5.80	6.20
e	0.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27
n	8		8	

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. For dimension E, body width does not include interlead flash.
4. Falls within JEDEC MS-012 variation AA.

FIGURE 1. Case outline – Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	D	Driver input
2	GND	Ground
3	V_{CC}	Supply voltage
4	R	Receiver output
5	LBK	Loopback
6	CANL	Low bus output
7	CANH	High bus output
8	R_S	Standby / slope control

FIGURE 2. Terminal connections.

DRIVER					
INPUTS			OUTPUS		
D	LBK / AB	R_S	CANH	CANL	BUS STATE
X	X	$> 0.75\ V_{CC}$	Z	Z	Recessive
L	L or open	$\leq 0.33\ V_{CC}$	H	L	Dominant
H or open	X	$\leq 0.33\ V_{CC}$	Z	Z	Recessive
X	H	$\leq 0.33\ V_{CC}$	Z	Z	Recessive

RECEIVER				
INPUTS				OUTPUTS
BUS STATE	$V_{ID} = V_{(CANH)} - V_{(CANL)}$	LBK	D	R
Dominant	$V_{ID} \geq 0.9\ V$	L or open	X	L
Recessive	$V_{ID} \leq 0.5\ V$ or open	L or open	H or open	H
?	$0.5\ V < V_{ID} < 0.9\ V$	L or open	H or open	?
X	X	H	L	L
X	X	H	H	H

H = High level
L = Low level
Z = high impedance
X = Irrelevant
? = Indeterminate

FIGURE 3. Function table.

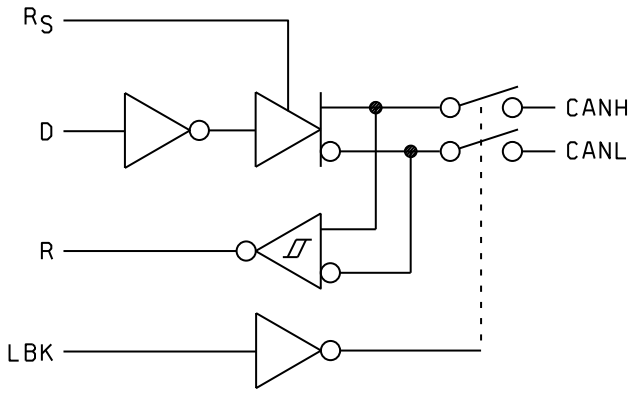
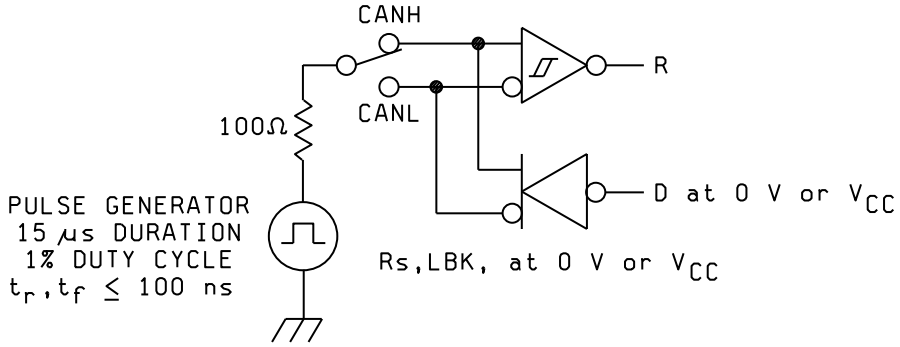


FIGURE 4. Functional block diagram.



NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

FIGURE 5. Transient over voltage test circuit.

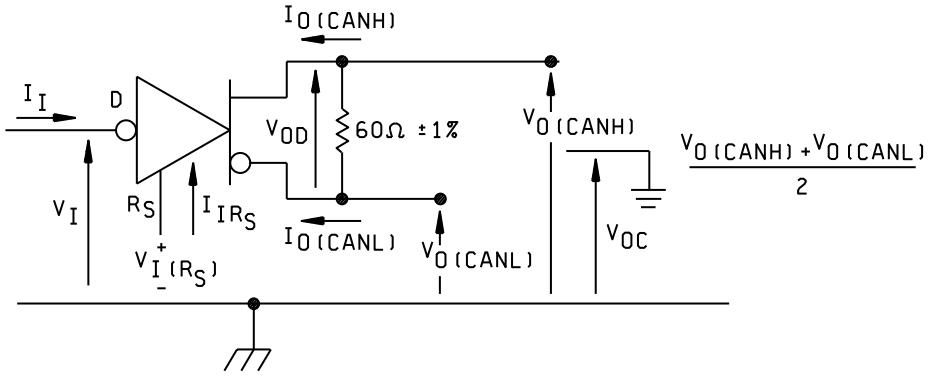


Figure 6. Driver voltage, current, and test definition.

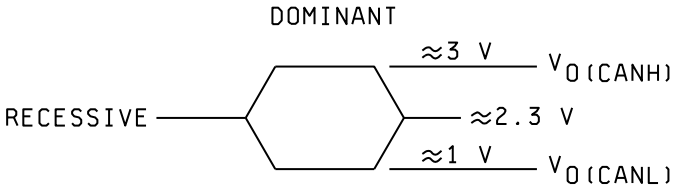


Figure 7. Bus logic state voltage definitions.

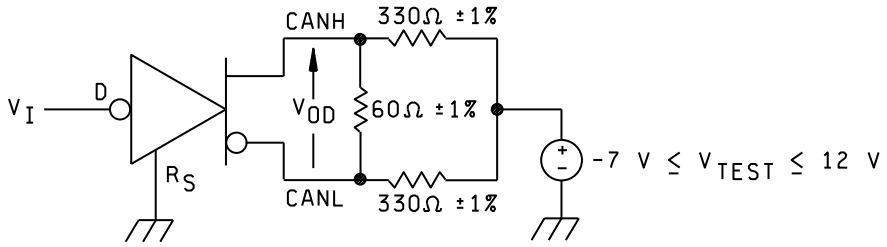
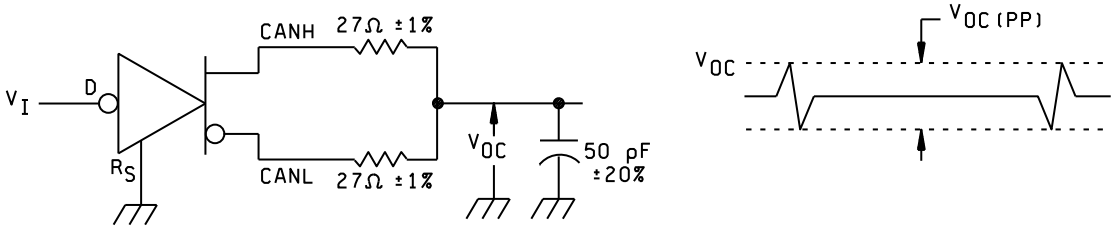


Figure 8. Driver V_{OD}.



NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 9. $V_{OC(pp)}$ test circuit and voltage waveforms.

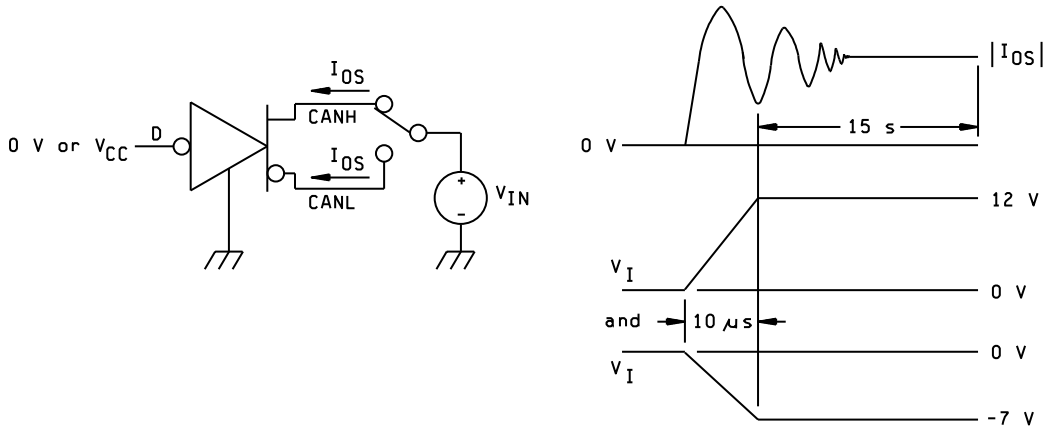
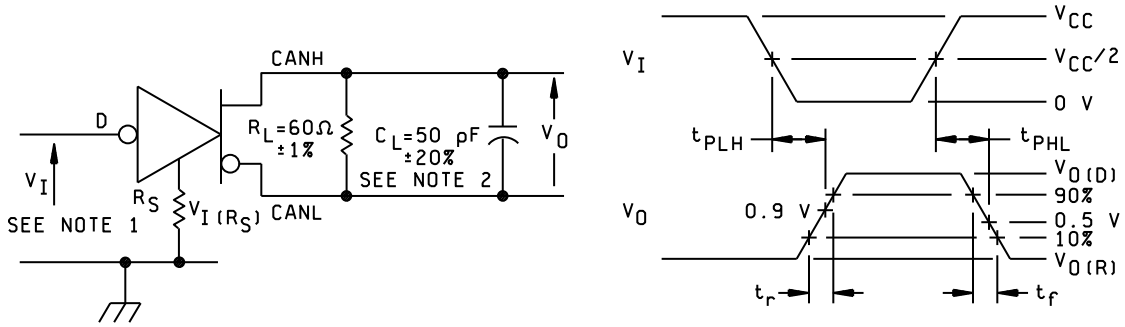


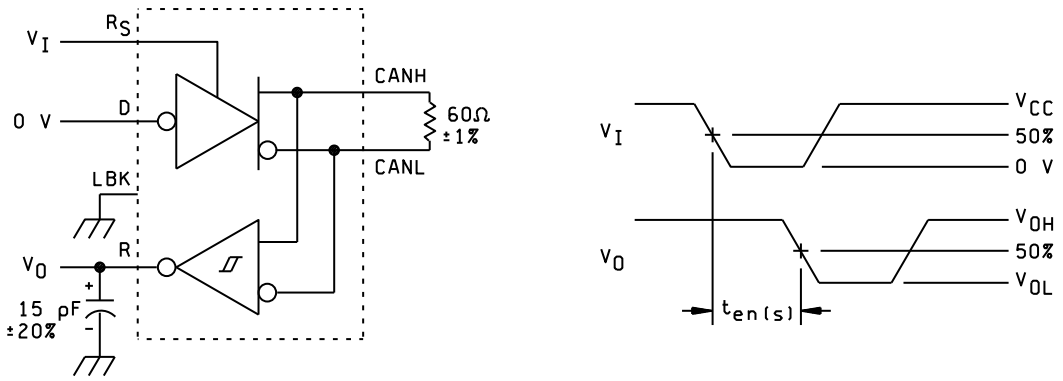
Figure 10. I_{OS} test circuit and waveforms.



NOTES:

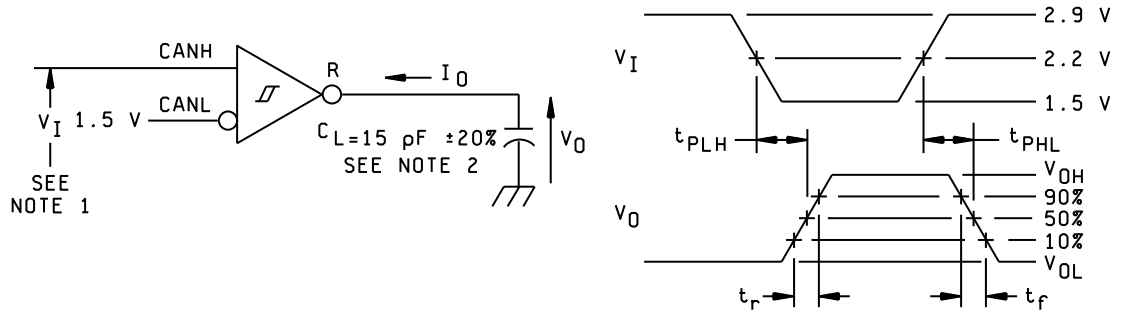
1. The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
2. C_L includes fixture and instrumentation capacitance.

Figure 11. Driver test circuit and voltage waveforms.



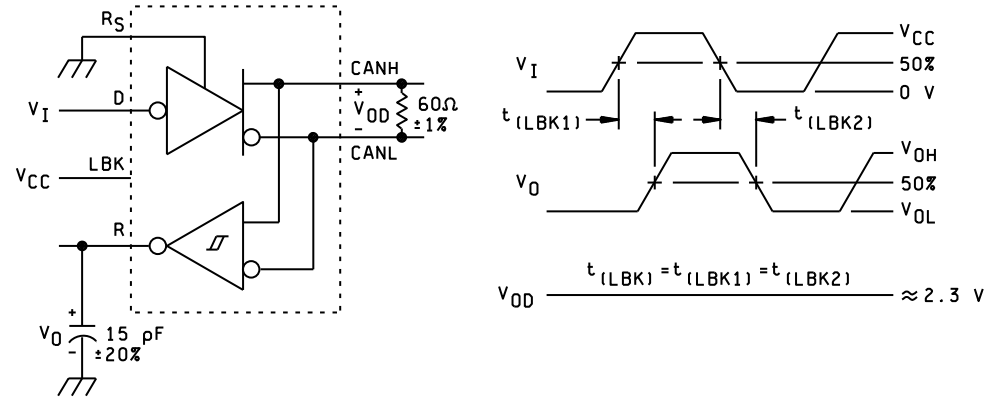
NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 12. $t_{en(s)}$ test circuit and voltage waveforms.



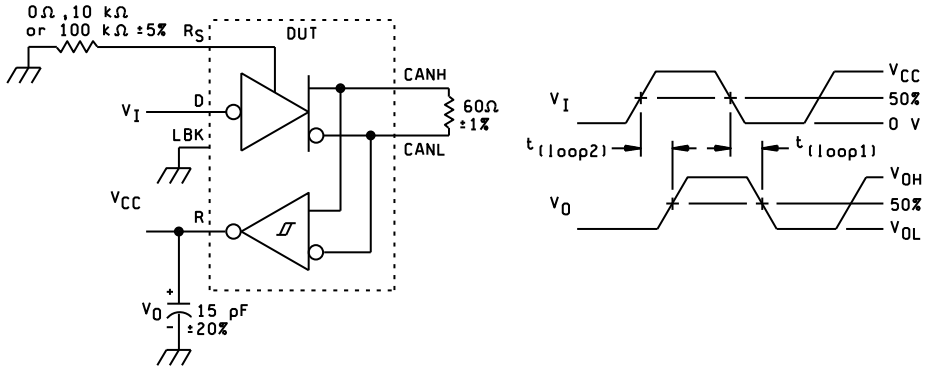
NOTES:
1. The input pulse is supplied by a generator having the following characteristics: Pulse repetition rate (PRR) ≤ 125 kHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50\ \Omega$.
2. C_L includes fixture and instrumentation capacitance.

Figure 13. Receiver test circuit and voltage waveforms.



NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 14. $t_{(LBK)}$ test circuit and voltage waveforms.



NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 15. $t_{(loop)}$ test circuit and voltage waveforms.

TABLE II. Differential input voltage threshold test.

INPUT		OUTPUT		MEASURED
V_{CANH}	V_{CANL}	R		$\lvert V_{ID} \rvert$
-6.1 V	-7 V	L	V_{OL}	900 mV
12 V	11.1 V	L		900 mV
-1 V	-7 V	L		6 V
12 V	6 V	L		6 V
-6.5 V	-7 V	H	V_{OH}	500 mV
12 V	11.5 V	H		500 mV
-7 V	-1 V	H		6 V
6 V	12 V	H		6 V
Open	Open	H		X

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/ 2/	Device manufacturer CAGE code	Package 3/	Top side marking	Vendor part number
V62/09611-01XE	01295	Reel of 2500	H233EP	SN65HVD233MDREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet.
3/ Package drawings, standard packaging quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available from the manufacturer.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243