REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update document paragraphs to current requirements. - ro	15-10-20	C. SAFFLE

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**		A	A	A	A	A	A	A	A	A	A	A								
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PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 08-12-03	**CHECKED BY** RAJESH PITHADIA	**TITLE** MICROCIRCUIT, DIGITAL, TRIPLE BUFFER / DRIVER WITH OPEN DRAIN OUTPUTS, MONOLITHIC SILICON
	APPROVED BY ROBERT M. HEBER	
	SIZE **A** **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/09610**
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a triple buffer / driver with open drain outputs microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/09610	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74LVC3G07-EP	Triple buffer / driver with open drain outputs

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MO-187-CA	Plastic surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to 6.5 V
Input voltage range (V_I)	-0.5 V to 6.5 V
Voltage range applied to any output in the high impedance or power off state (V_O)	-0.5 V to 6.5 V 2/
Voltage range applied to any output in the high or low state (V_O)	-0.5 V to 6.5 V 2/ 3/
Input clamp current (I_{IK}) with $V_I < 0$	-50 mA maximum
Output clamp current (I_{OK}) with $V_O < 0$	-50 mA maximum
Continuous output current	±50 mA maximum
Continuous current through V_{CC} or GND	±100 mA maximum
Package thermal impedance (θ_{JA})	227°C/W 4/
Storage temperature range (T_{STG})	-65°C to +150°C

1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ The input and output negative voltage ratings may be exceeded if the input and output current ratings are observed.

3/ The value of V_{CC} is provided in the recommended operating conditions table.

4/ The package thermal impedance is calculated in accordance with JESD 51-7.

1.4 Recommended operating conditions. 5/ 6/

Supply voltage (V_{CC}):	
Operating	1.65 V to 5.5 V
Data retention only	1.5 V minimum
High level input voltage (V_{IH}):	
V_{CC} = 1.65 V to 1.95 V	0.65 V x V_{CC} minimum
V_{CC} = 2.3 V to 2.7 V	1.7 V minimum
V_{CC} = 3 V to 3.6 V	2 V minimum
V_{CC} = 4.5 V to 5.5 V	0.7 V x V_{CC} minimum
Low level input voltage (V_{IL}):	
V_{CC} = 1.65 V to 1.95 V	0.35 V x V_{CC} maximum
V_{CC} = 2.3 V to 2.7 V	0.7 V maximum
V_{CC} = 3 V to 3.6 V	0.8 V maximum
V_{CC} = 4.5 V to 5.5 V	0.3 V x V_{CC} maximum
Input voltage range (V_I)	0 V to 5.5 V
Output voltage range (V_O)	0 V to 5.5 V
Low level output current (I_{OL}) :	
V_{CC} = 1.65 V	4 mA maximum
V_{CC} = 2.3 V	8 mA maximum
V_{CC} = 3 V	16 mA maximum 24 mA maximum
V_{CC} = 4.5 V	32 mA maximum
Input transition rise or fall rate ($\Delta t / \Delta V$):	
V_{CC} = 1.8 V ±0.15 V, 2.5 V ±0.2 V	20 ns / V
V_{CC} = 3.3 V ±0.3 V	10 ns / V
V_{CC} = 5 V ±0.5 V	5 ns / V
Operating free-air temperature range (T_A)	-55°C to +125°C

5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

EIA/JEDEC 51-7 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JEDEC PUB 95 - Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Low level output voltage	V_{OL}	I_{OL} = 100 μA, V_{CC} = 1.65 V to 5.5 V	-55°C to +125°C	01		0.1	V
		I_{OL} = 4 mA, V_{CC} = 1.65 V				0.45	
		I_{OL} = 8 mA, V_{CC} = 2.3 V				0.3	
		I_{OL} = 16 mA, V_{CC} = 3 V				0.4	
		I_{OL} = 24 mA, V_{CC} = 3 V				0.55	
		I_{OL} = 32 mA, V_{CC} = 4.5 V				0.55	
Input current, A inputs	I_I	V_I = 5.5 V or GND, V_{CC} = 0 to 5.5 V	-55°C to +125°C	01		±5	μA
Off current 2/	I_{off}	V_I or V_O = 5.5 V, V_{CC} = 0	-55°C to +125°C	01		±10	μA
Supply current	I_{CC}	V_I = 5.5 V or GND, I_O = 0 , V_{CC} = 1.65 V to 5.5 V	-55°C to +125°C	01		10	μA
Delta supply current	ΔI_{CC}	One input at V_{CC} – 0.6 V, other inputs at V_{CC} or GND, V_{CC} = 3 V to 5.5 V	-55°C to +125°C	01		500	μA
Input capacitance	C_I	V_I = V_{CC} or GND, V_{CC} = 3.3 V	+25°C	01	3.5 typical		pF
Propagation delay time	t_{PD}	From input A to output Y, V_{CC} = 2.5 V ±0.2 V, see figure 5	-55°C to +125°C	01	0.5	7.3	ns
		From input A to output Y, V_{CC} = 3.3 V ±0.3 V, see figure 5			1.1	6.7	
		From input A to output Y, V_{CC} = 5 V ±0.5 V, see figure 5			0.25	5.9	
Power dissipation capacitance	C_{pd}	V_{CC} = 1.8 V, f = 10 MHz	+25°C	01	3 typical		pF
		V_{CC} = 2.5 V, f = 10 MHz			3 typical		
		V_{CC} = 3.3 V, f = 10 MHz			4 typical		
		V_{CC} = 5 V, f = 10 MHz			5 typical		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ This device is fully specified for partial power down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Case X

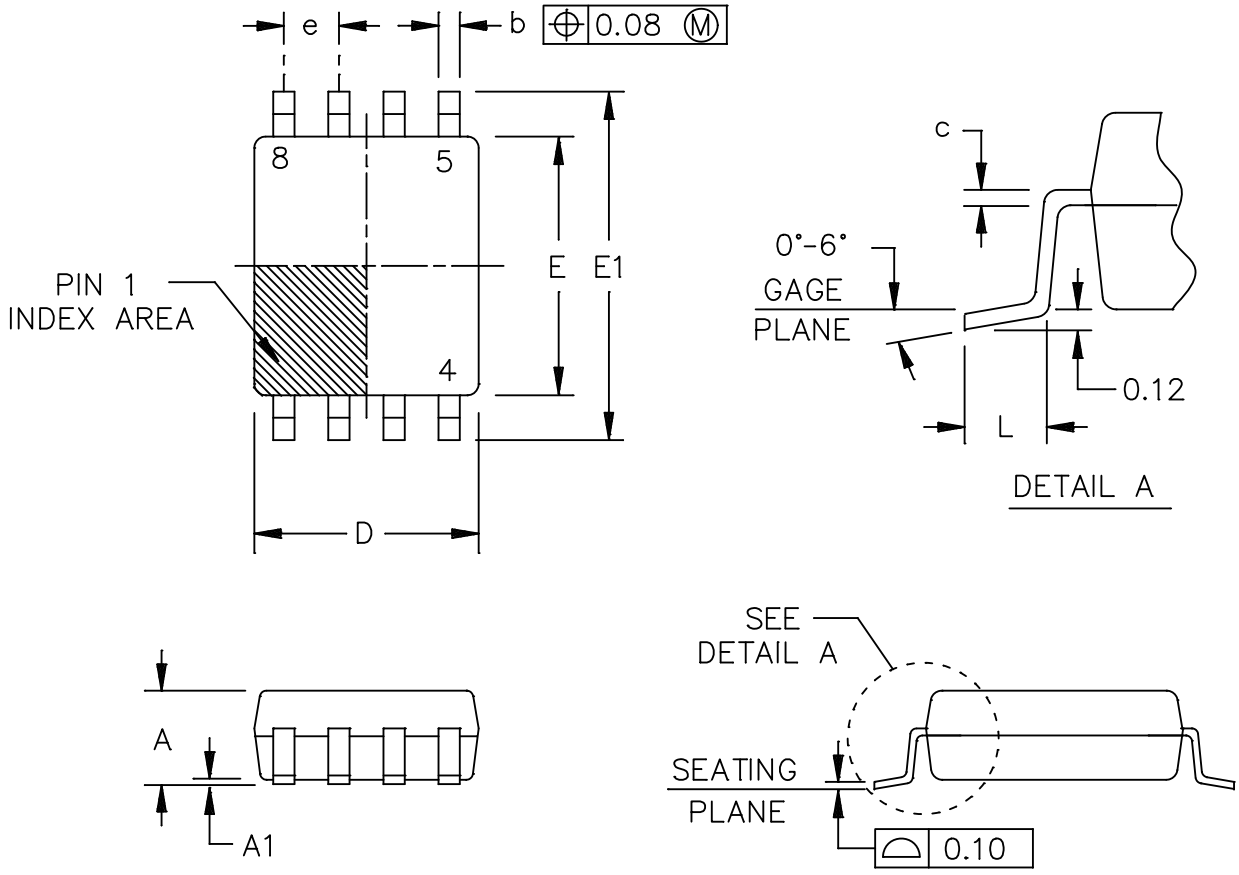

FIGURE 1. Case outline.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/09610
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Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.023	.035	0.60	0.90
A1	.000	.003	0.00	0.10
b	.006	.009	0.17	0.25
c	.005 NOM		0.13 NOM	
D	.074	.082	1.90	2.10
E	.086	.094	2.20	2.40
E1	.118	.125	3.00	3.20
e	.019 BSC		0.50 BSC	
L	.007	.013	0.20	0.35

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 mm (0.006 inch) per end.
3. Falls within reference to JEDEC MO-187-CA.

FIGURE 1. Case outline - Continued.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	INPUT 1A
2	OUTPUT 3Y
3	INPUT 2A
4	GND
5	OUTPUT 2Y
6	INPUT 3A
7	OUTPUT 1Y
8	V_{CC}

FIGURE 2. Terminal connections.

INPUT A	OUTPUT Y
H	H
L	L

FIGURE 3. Truth table.

Positive logic

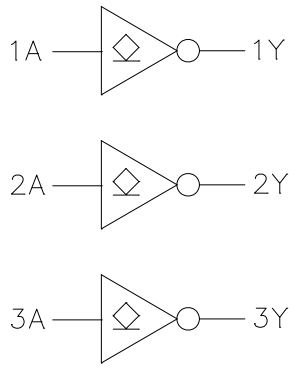
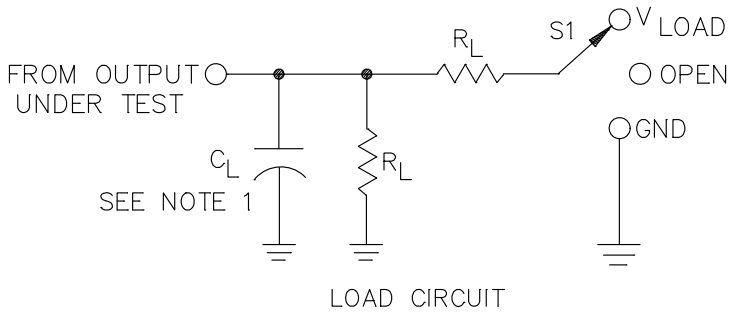


FIGURE 4. Logic diagram.

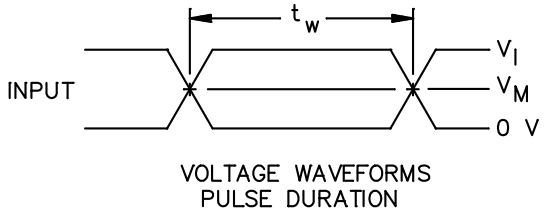


LOAD CIRCUIT

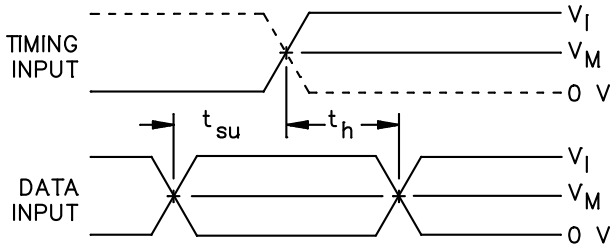
Test	S1
t_{PZL} (see notes 2 and 3)	V_{LOAD}
t_{PLZ} (see notes 2 and 4)	V_{LOAD}
t_{PHZ} / t_{PZH}	V_{LOAD}

V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r / t_f					
1.8 V ±0.15 V	V_{CC}	≤ 2 ns	V_{CC} / 2	2 x V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ±0.20 V	V_{CC}	≤ 2 ns	V_{CC} / 2	2 x V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ±0.30 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5.0 V ±0.50V	V_{CC}	≤ 2.5 ns	V_{CC} / 2	2 x V_{CC}	50 pF	500 Ω	0.3 V

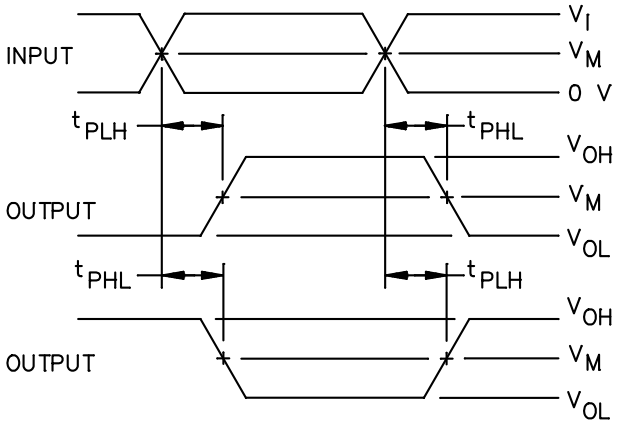
FIGURE 5. Timing waveforms and test circuit.



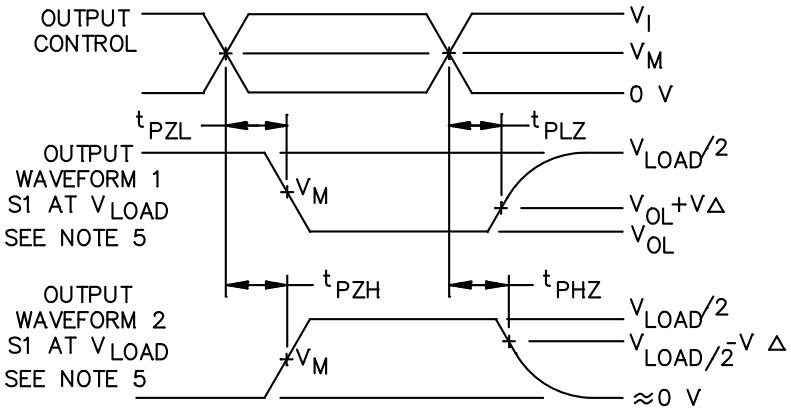
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW AND HIGH-LEVEL ENABLING

Notes:

1. C_L includes probe and jig capacitance.
2. Since this device has open drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd}.
3. t_{PZL} is measured at V_M.
4. t_{PLZ} is measured at $V_{OL} + V_\Delta$.
5. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
6. All input pulses are supplied by generators having following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
7. The outputs are measured one at a time with one transaction per measurement.
8. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Timing waveforms and test circuit – Continued.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/ 2/	Device manufacturer CAGE code	Package 3/	Top side marking 4/	Vendor part number
V62/09610-01XE	01295	Reel of 3000	SOCM	SN74LVC3G07MDCUREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet or contact the manufacturer.
3/ Package drawings, thermal data, and symbolization are available from the manufacturer.
4/ The actual top side marking has one additional character that designates the wafer fab/assembly site.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243