REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Correct terminal connections in figure 2. - PHN	13-01-16	Thomas M. Hess
B	Update boilerplate paragraphs to current VID description requirements. - PHN	22-02-22	Muhammad A. Akbar

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	B	B	B	B	B	B	B	B														
SHEET	1	2	3	4	5	6	7	8														

PMIC N/A

Original date of drawing

YY MM DD

09-02-04

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TITLE
MICROCIRCUIT, DIGITAL, CMOS HEX VOLTAGE LEVEL SHIFTER FOR TTL TO CMOS OR CMOS TO CMOS OPERATION, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/09606
REV B		PAGE 1 OF 8

AMSC N/A

5962-V021-22

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance CMOS hex voltage level shifter for TTL to CMOS or CMOS to CMOS operation microcircuit, with an operating temperature range of -55ºC to +125ºC.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/09606	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	CD4504B-EP	CMOS hex voltage level shifter for TTL to CMOS or CMOS to CMOS operation

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	JEDEC MO-153	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings.

DC supply voltage range, Voltage referenced to VSS terminal (V_{DD}) ..... -0.5 V to +20.0 V
Input voltage range, all inputs ..... -05 V to V_{CC} + 0.5 V
Maximum DC input current, any one input ..... ±10 mA
Maximum power dissipation per package, (PD):
T_A = -55°C to +100°C ..... 500 mW
T_A = +100°C to +125°C 1/
Maximum device dissipation per output transistor, for T_A = full package temperature range (all package types) ..... 100 mW
Operating temperature range, (T_A) ..... -55°C to +125°C
Maximum package thermal impedance (θ_{JA}) ..... 91.1°C/W 2/
Storage temperature range, (T_{STG}) ..... -85°C to +150°C
Maximum lead temperature (during soldering) , at distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max ..... +265°C

1/ Derate linearly at 12 mW/°C to 200 nW.
2/ The package thermal impedance is calculated in accordance with JESD 51-7.

1.4. Recommended operating conditions. 3/ 4/

Supply voltage range, (for T_A = full package temperature range) (V_{DD}) ..... +5.0 V to +18.0 V

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at https://www.jedec.org).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

3/ For maximum reliability, nominal operating conditions should be selected so that operation is always within the recommended range.
4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

TABLE I. Electrical performance characteristics. 1/

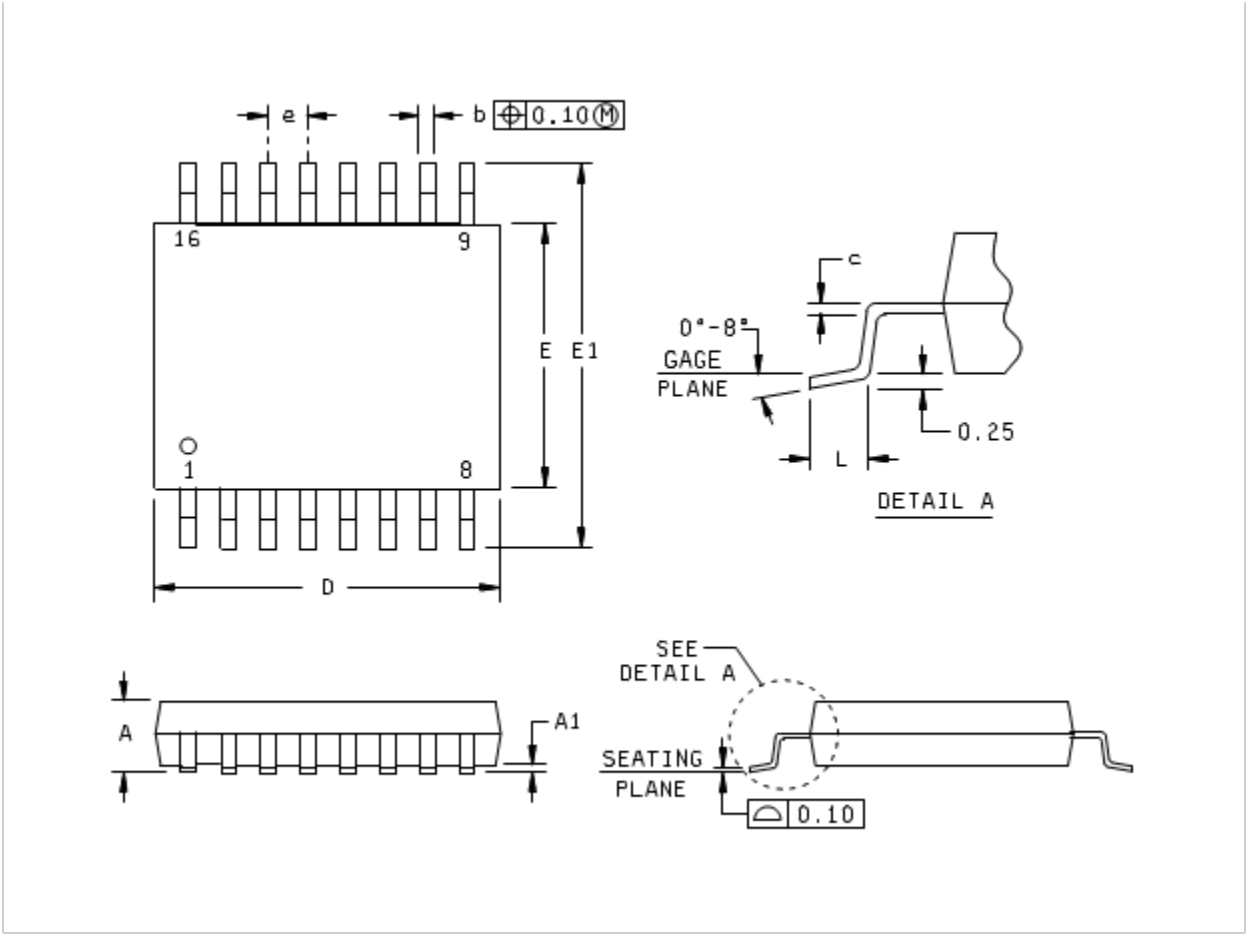
Test		Symbol	Conditions 2/				Limits at indicated temperatures (°C)						Unit
			V_O (V)	V_{IN} (V)	V_{CC} (V)	V_{CC} (V)	-55	-40	+85	+125	+ 25 Min	+ 25 Max	
Quiescent device current, I_{DD} max and I_{CC} in CMOS-CMOS mode				0, 5	5	5	1.5	1.5	1.5	1.5		1.5	mA
				0, 10	5	10	2	2	2	2		2	
				0, 15	5	15	4	4	120	120		4	µA
				0, 20	5	20	20	20	600	600		20	
Quiescent device current, I_{CC} max TTL-CMOS mode				0, 5	5	5	5	5	6	6		5	mA
				0, 10	5	10	5	5	6	6		5	
				0, 15	5	15	5	5	6	6		5	
Output low (sink) current, I_{OL} min			0.4	0, 5		5	0.64	0.61	0.42	0.36	0.51		mA
			0.5	0, 10		10	1.6	1.5	1.1	0.9	1.3		
			1.5	0, 15		15	4.2	4	2.8	2.4	3.4		
Output low (source) current, I_{OH} min			4.6	0, 5		5	-0.64	-0.61	-0.42	-0.36	-0.51		
			2.5	0, 5		5	-2	-1.8	-1.3	-1.15	-1.6		
			9.5	0, 10		10	-1.6	-1.5	-1.1	-0.9	-1.3		
			13.5	0, 15		15	-4.2	-4	-2.8	-2.4	-3.4		
Output voltage: low level, V_{OL} max				0, 5		5	0.05					0.05	V
				0, 10		10	0.05					0.05	
				0, 15		15	0.05					0.05	
Output voltage: high level, V_{OH} min				0, 5		5	4.95				4.95		
				0, 10		10	9.95				9.95		
				0, 15		15	14.95				14.95		
Input low voltage V_{IL} max 3/	TTL-CMOS		1		5	10	0.8					0.8	
	TTL-CMOS		1		5	15	0.8					0.8	
	CMOS-CMOS		1		5	10	1.5					1.5	
	CMOS-CMOS		1.5		5	15	1.5					1.5	
	CMOS-CMOS		1.5		10	15	3					3	
Input high Voltage, V_{IH} min 3/	TTL-CMOS		9		5	10	2				2		
	TTL-CMOS		13.5		5	15	2				2		
	CMOS-CMOS		9		5	10	3.5				3.5		
	CMOS-CMOS		13.5		5	15	3.5				3.5		
	CMOS-CMOS		13.5		10	15	7				7		
Input current, I_{IN} max				0, 18		18	±0.1	±0.1	±1	±1		±0.1	µA

See footnote at end of the table.

TABLE I. Electrical performance characteristics. 1/

Test		Symbol	Conditions 4/	V_{CC} (V)	V_{DD} (V)	Limits Min	Limits Max	Unit
Propagation delay: high to low	From TTL to CMOS	t_{PHL}	$V_{DD} > V_{CC}$	5	10		280	ns
				5	15		280	
	From CMOS to CMOS		$V_{DD} > V_{CC}$	5	10		240	
				5	15		240	
				10	15		140	
	From CMOS to CMOS		$V_{CC} > V_{DD}$	10	5		550	
				15	5		550	
				15	10		140	
Propagation delay: high to low	From TTL to CMOS	t_{PLH}	$V_{DD} > V_{CC}$	5	10		280	ns
				5	15		280	
	From CMOS to CMOS		$V_{DD} > V_{CC}$	5	10		240	
				5	15		240	
				10	15		140	
	From CMOS to CMOS		$V_{CC} > V_{DD}$	10	5		400	
				15	5		400	
				15	10		120	
Transition time		t_{THL}, t_{TLH}	All modes		5		200	ns
					10		100	
					15		80	
Input capacitance		C_{IN}	Any input				7.5	pF

1. Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2. Over recommended operating free air temperature range (unless otherwise noted).
3. Applies to the six input signals. For mode control (P13), only the CMOS-CMOS ratings apply..
4. $T_A = 25°C$, Input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200\ \Omega$.



Dimensions					
Symbol	Min	Max	Symbol	Min	Max
A		1.20	e	0.65 BSC	
A1	0.05	0.15	E	4.30	4.50
b	0.19	0.30	E1	6.20	6.60
c	0.15 NOM		L	0.50	0.75
D	4.90	5.10			

Notes:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion not to exceed 0.15.
4. Fall within JEDEC MO-153.

FIGURE 1. Case outlines.

Pin No.	Signal name	Pin No.	Signal name
1	V_{CC}	16	V_{DD}
2	A_{OUT}	15	F_{OUT}
3	A_{IN}	14	F_{IN}
4	B_{OUT}	13	SELECT
5	B_{IN}	12	E_{OUT}
6	C_{OUT}	11	E_{IN}
7	C_{IN}	10	D_{OUT}
8	V_{SS}	9	D_{IN}

FIGURE 2. Terminal connections.

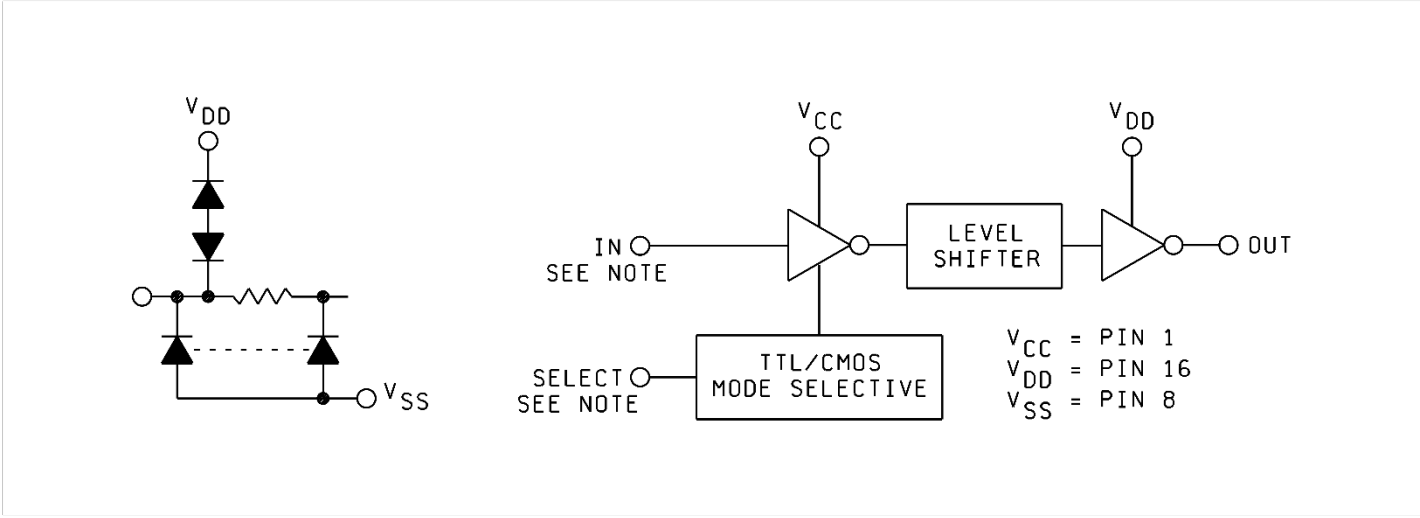


FIGURE 3. Block diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/09606-01XE	01295	CD4504BMPWREP	4504BEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243