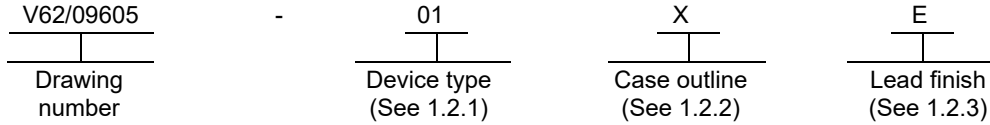




1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance CMOS hex voltage level shifter for TTL to CMOS or CMOS to CMOS operation microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74LVC16T245-EP	16-bit dual supply bus transceiver with configurable voltage translation and 3-state outputs.

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	48	JEDEC MO-153	Plastic small outline package
Y	48	JEDEC MO-153	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range, ( $V_{CCA}, V_{CCB}$ ) .....	-0.5 V to +6.5 V
Input voltage range, ( $V_i$ ):	
I/O ports (A port) .....	-0.5 V to +6.5 V 2/
I/O ports (B port) .....	-0.5 V to +6.5 V 2/
Control inputs .....	-0.5 V to +6.5 V 2/
Voltage range applied to any output in the high impedance or power-off stage, ( $V_o$ ):	
A port .....	-0.5 V to +6.5 V 2/
B port .....	-0.5 V to +6.5 V 2/
Voltage range applied to any output in the high or slow state, ( $V_o$ ):	
A port .....	-0.5 V to $V_{CCA} + 0.5$ V 2/ 3/
B port .....	-0.5 V to $V_{CCB} + 0.5$ V 2/ 3/
Input clamp current, ( $I_{IK}$ ) ( $V_i < 0$ ) .....	-50 mA
Output clamp current, ( $I_{OK}$ ) ( $V_o < 0$ ) .....	-50 mA
Continuous output current, ( $I_o$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 100$ mA
Package thermal impedance ( $\theta_{JA}$ ) .....	58°C/W 4/
Storage temperature range, ( $T_{STG}$ ).....	-65°C to +150°C

1.4 Recommended operating conditions. 5/ 6/ 7/ 8/

		$V_{CCI}$	$V_{CCO}$	Min	Max	Unit
Supply voltage, ( $V_{CC}$ )	$V_{CCA}$			1.65	5.5	V
	$V_{CCB}$			1.65	5.5	
		1.65 V to 1.95 V		$0.65 \times V_{CCI}$		
High level input voltage, ( $V_{IH}$ )	Data inputs 9/	2.3 V to 2.7 V		1.7		
		3.0 V to 3.6 V		2		
		4.5 V to 5.5 V		$0.7 \times V_{CCI}$		
		1.65 V to 1.95 V			$0.35 \times V_{CCI}$	
Low level input voltage, ( $V_{IL}$ )	Data inputs 9/	2.3 V to 2.7 V			0.7	
		3.0 V to 3.6 V			0.8	
		4.5 V to 5.5 V			$0.3 \times V_{CCI}$	

- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ The input and output negative voltage ratings may exceeded if the input and output current ratings are observed.
- 3/ The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed..
- 4/ The package thermal impedance is calculated in accordance with JESD 51-7.
- 5/  $V_{CCI}$  is the  $V_{CC}$  associated with the data input port.
- 6/  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.
- 7/ All unused or driven (floating) data inputs (I/Os) of the device must be held at logic HIGH or LOW (preferably  $V_{CCI}$  or GND) to ensure proper device operation and minimized power. Refer to manufacturer for more information.
- 8/ All unused control inputs must be held at  $V_{CCA}$  or GND to ensure proper device operation and minimize power consumption.
- 9/ For  $V_{CCI}$  values not specified in the data sheet,  $V_{IH} \text{ min} = V_{CCI} \times 0.7$ ,  $V_{IL} \text{ max} = V_{CCI} \times 0.3$  V.

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1.4 Recommended operating conditions - Continued.

		V <sub>CCI</sub>	V <sub>CCO</sub>	Min	Max	Unit
		1.65 V to 1.95 V		0.65 x V <sub>CCA</sub>		V
High level input voltage, (V <sub>IH</sub> )	Control inputs <u>10/</u> referenced to V <sub>CCA</sub>	2.3 V to 2.7 V		1.7		
		3.0 V to 3.6 V		2		
		4.5 V to 5.5 V		0.7 x V <sub>CCA</sub>		
		1.65 V to 1.95 V			0.35 x V <sub>CCA</sub>	
Low level input voltage, (V <sub>IL</sub> )	Control inputs <u>10/</u> referenced to V <sub>CCA</sub>	2.3 V to 2.7 V			0.7	
		3.0 V to 3.6 V			0.8	
		4.5 V to 5.5 V			0.3 x V <sub>CCA</sub>	
Input voltage, (V <sub>I</sub> )	Control inputs			0	5.5	
Input/Output voltage, (V <sub>I/O</sub> )	Active state			0	V <sub>CCO</sub>	
	3-state			0	5.5	
			1.65 V to 1.95 V		-4	mA
High level output current, (I <sub>OH</sub> )			2.3 V to 2.7 V		-8	
			3.0 V to 3.6 V		-24	
			4.5 V to 5.5 V		-32	
			1.65 V to 1.95 V		4	
Low level output current, (I <sub>OL</sub> )			2.3 V to 2.7 V		8	
			3.0 V to 3.6 V		24	
			4.5 V to 5.5 V		32	
		1.65 V to 1.95 V			20	ns/V
Input transition rise or fall rate, Δt/Δv	Data inputs	2.3 V to 2.7 V			20	
		3.0 V to 3.6 V			10	
		4.5 V to 5.5 V			5	
Operating free air temperature, T <sub>A</sub>				-55	125	°C

10/ For V<sub>CCA</sub> values not specified in the data sheet, V<sub>IH</sub> min = V<sub>CCA</sub> x 0.7, V<sub>IL</sub> max = V<sub>CCA</sub> x 0.3 V.

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2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JEP95 – Registered and Standard Outlines for Semiconductor Devices
- JESD51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Function table. The function table shall be as shown in figure 4.

3.5.5 Load circuit and voltage waveforms. The load circuit and timing waveforms shall be as specified in figure 5.

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TABLE I. Electrical performance characteristics. 1/

Test		Symbol	Conditions 2/ 3/ 4/ unless otherwise specified	V <sub>CCA</sub>	V <sub>CCB</sub>	Limits		Unit
						Min	Max	
High level output voltage		V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> , I <sub>OH</sub> = -100 μA	1.65 V to 4.5 V	1.65 V to 4.5 V	V <sub>CCO</sub> -0.1		V
			V <sub>I</sub> = V <sub>IH</sub> , I <sub>OH</sub> = -4 mA	1.65 V	1.65 V	1.2		
			V <sub>I</sub> = V <sub>IH</sub> , I <sub>OH</sub> = -8 mA	2.3 V	2.3 V	1.9		
			V <sub>I</sub> = V <sub>IH</sub> , I <sub>OH</sub> = -24 mA	3 V	3 V	2.4		
			V <sub>I</sub> = V <sub>IH</sub> , I <sub>OH</sub> = -32 mA	4.5 V	4.5 V	3.8		
Low level output voltage		V <sub>OL</sub>	V <sub>I</sub> = V <sub>IL</sub> , I <sub>OL</sub> = 100 μA	1.65 V to 4.5 V			0.1	V
			V <sub>I</sub> = V <sub>IL</sub> , I <sub>OL</sub> = 4 mA	1.65 V			0.45	
			V <sub>I</sub> = V <sub>IL</sub> , I <sub>OL</sub> = 8 mA	2.3 V			0.3	
			V <sub>I</sub> = V <sub>IL</sub> , I <sub>OL</sub> = 24 mA	3 V			0.55	
			V <sub>I</sub> = V <sub>IL</sub> , I <sub>OL</sub> = 32 mA	4.5 V			0.55	
Input current	Control inputs	I <sub>I</sub>	V <sub>I</sub> = V <sub>CCA</sub> or GND	1.65 V to 5.5 V	1.65 V to 5.5 V		±3	μA
			V <sub>I</sub> = V <sub>CCB</sub> or GND, T <sub>A</sub> = 25°C	1.65 V to 5.5 V	1.65 V to 5.5 V		±1	
5/		I <sub>BHL</sub>	V <sub>I</sub> = 0.58 V	1.65 V	1.65 V	15		μA
			V <sub>I</sub> = 0.7 V	2.3 V	2.3 V	45		
			V <sub>I</sub> = 0.8 V	3 V	3 V	75		
			V <sub>I</sub> = 1.35 V	4.5 V	4.5 V	100		
6/		I <sub>BHH</sub>	V <sub>I</sub> = 107 V	1.65 V	1.65 V	-15		μA
			V <sub>I</sub> = 1.7 V	2.3 V	2.3 V	-45		
			V <sub>I</sub> = 2 V	3 V	3 V	-75		
			V <sub>I</sub> = 3.15 V	4.5 V	4.5 V	-100		
7/		I <sub>BHLO</sub>	V <sub>I</sub> = 0 to V <sub>CC</sub>	1.95 V	1.95 V	200		μA
				2.7 V	2.7 V	300		
				3.6 V	3.6 V	500		
				5.5 V	5.5 V	900		
8/		I <sub>BHHO</sub>	V <sub>I</sub> = 0 to V <sub>CC</sub>	1.95 V	1.95 V	-200		μA
				2.7 V	2.7 V	-300		
				3.6 V	3.6 V	-500		
				5.5 V	5.5 V	-900		
			V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0 V	0 to 5.5 V		±20	μA
Input/Output power	A or B	I <sub>off</sub>		0 to 5.5 V	0 V	±20		
off leakage current	port		V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V,	0 V	0 to 5.5 V		±1.5	
			T <sub>A</sub> = 25°C	0 to 5.5 V	0 V		±1.5	

See footnote at end of the table.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ 3/ 4/ unless otherwise specified		V <sub>CCA</sub>	V <sub>CCB</sub>	Limits		Unit		
						Min	Max			
High impedance state output current	A or B port	I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CCO</sub> or GND, V <sub>I</sub> = V <sub>CCI</sub> or GND	$\overline{OE} = V_{IH}$	1.65 V to 5.5 V	1.65 V to 5.5 V		±4	μA	
	B port			$\overline{OE} =$ don't care	0 V	5.5 V		±4		
	A port				5.5 V	0 V		±4		
	A or B port	V <sub>O</sub> = V <sub>CCO</sub> or GND, V <sub>I</sub> = V <sub>CCI</sub> or GND T <sub>A</sub> = 25°C	$\overline{OE} = V_{IH}$	1.65 V to 5.5 V	1.65 V to 5.5 V		±1			
	B port		$\overline{OE} =$ don't care	0 V	5.5 V		±1			
	A port			5.5 V	0 V		±1			
Quiescent supply current	I <sub>CCA</sub>	V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0		1.65 V to 5.5 V	1.65 V to 5.5 V		20	μA		
				5 V	0 V		20			
				0 V	5 V		-4			
	I <sub>CCB</sub>	V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0		1.65 V to 5.5 V	1.65 V to 5.5 V		20	μA		
				5 V	0 V		-4			
				0 V	5 V		20			
	I <sub>CCA</sub> + I <sub>CCB</sub>	V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0		1.65 V to 5.5 V	1.65 V to 5.5 V		30	μA		
	Quiescent supply current delta	DIR	ΔI <sub>CCA</sub>	DIR at V <sub>CCA</sub> - 0.6 V, B port = open A port at V <sub>CCA</sub> or GND		3 V to 5.5 V	3 V to 5.5 V		50	μA
	Input capacitance	Control inputs	C <sub>i</sub>	V <sub>I</sub> = V <sub>CCA</sub> or GND, T <sub>A</sub> = 25°C		3.3 V	3.3 V		5	pF
Input/Output capacitance	A or B port	C <sub>io</sub>	V <sub>I</sub> = V <sub>CCA</sub> or GND, T <sub>A</sub> = 25°C		3.3 V	3.3 V	4	TYP		
			V <sub>I</sub> = V <sub>CCA</sub> or GND, T <sub>A</sub> = 25°C		3.3 V	3.3 V		10		
			V <sub>I</sub> = V <sub>CCA</sub> or GND, T <sub>A</sub> = 25°C		3.3 V	3.3 V	8.5	TYP		

See footnote at end of the table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 2/ unless otherwise specified	V <sub>CCB</sub> = 1.8 V ±0.15 V		V <sub>CCB</sub> = 2.5 V ±0.2 V		V <sub>CCB</sub> = 3.3 V ±0.3 V		V <sub>CCB</sub> = 5 V ±0.5 V		Unit	
			Min	Max	Min	Max	Min	Max	Min	Max		
<b>Switching characteristic</b> V <sub>CCA</sub> = 1.8 V ±0.15 V												
Propagation delay time, from input A to output B	t <sub>PLH</sub>		1.7	25.9	1.3	13.2	1	11.4	0.4	11.1	ns	
Propagation delay time, from input B to output A	t <sub>PHL</sub>		0.9	27.8	0.8	27.8	0.7	27.4	0.7	27.4		
Disable time, from input OE to output A	t <sub>PHZ</sub>		1.5	33.6	1.5	33.4	1.5	33.3	1.4	33.2		
Disable time, from input OE to output B	t <sub>PLZ</sub>		2.4	36.2	1.9	17.1	1.7	16	1.3	14.3		
Enable time, from input OE to output A	t <sub>PZH</sub>		0.4	28	0.4	27.8	0.4	27.7	0.4	27.7		
Enable time, from input OE to output B	t <sub>PZL</sub>		1.8	36	1.5	22	1.2	16.6	0.9	14.8		
<b>Switching characteristics,</b> V <sub>CCA</sub> = 2.5 V ±0.2 V												
Propagation delay time, from input A to output B	t <sub>PLH</sub>		1.5	25.4	1.2	13	0.8	10.2	0.6	8.8		ns
Propagation delay time, from input B to output A	t <sub>PHL</sub>		1.2	13.3	1	13.1	1	12.9	0.9	12.8		
Disable time, from input OE to output A	t <sub>PHZ</sub>		1.4	13	1.4	13	1.4	13	1.4	13		
Disable time, from input OE to output B	t <sub>PLZ</sub>		2.3	33.6	1.8	14	1.7	14.3	0.9	10.9		
Enable time, from input OE to output A	t <sub>PZH</sub>		1	14.9	1	14.9	1	14.9	1	14.9		
Enable time, from input OE to output B	t <sub>PZL</sub>		1.7	32.2	1.5	16.9	1.2	13.4	1	10.9		

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 2/	V <sub>CCB</sub> = 1.8 V ±0.15 V		V <sub>CCB</sub> = 2.5 V ±0.2 V		V <sub>CCB</sub> = 3.3 V ±0.3 V		V <sub>CCB</sub> = 5 V ±0.5 V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
		unless otherwise specified									
<b>Switching characteristic V<sub>CCA</sub> = 3.3 V ±0.3 V</b>											
Propagation delay time, from input A to output B	t <sub>PLH</sub>		1.6	25.2	1.1	12.8	0.8	10.2	0.6	8.4	ns
Propagation delay time, from input B to output A	t <sub>PHL</sub>										
Propagation delay time, from input B to output A	t <sub>PLH</sub>		0.8	11.2	0.8	10.2	0.7	10.1	0.6	10	
Propagation delay time, from input B to output A	t <sub>PHL</sub>										
Disable time, from input OE to output A	t <sub>PHZ</sub>		1.6	12.2	1.6	12.2	1.6	12.2	1.6	12.2	
Disable time, from input OE to output A	t <sub>PLZ</sub>										
Disable time, from input OE to output B	t <sub>PHZ</sub>		2.1	33	1.7	14.3	1.5	12.8	0.8	10.3	
Disable time, from input OE to output B	t <sub>PLZ</sub>										
Enable time, from input OE to output A	t <sub>PZH</sub>		0.8	11.8	0.8	12.1	0.8	12.1	0.8	12.1	
Enable time, from input OE to output A	t <sub>PZL</sub>										
Enable time, from input OE to output B	t <sub>PZH</sub>		1.8	3.7	1.4	16.4	1.1	12.5	0.9	10.4	
Enable time, from input OE to output B	t <sub>PZL</sub>										
<b>Switching characteristics, V<sub>CCA</sub> = 5 V ±0.5 V</b>											
Propagation delay time, from input A to output B	t <sub>PLH</sub>		1.5	25.4	1	12.8	0.7	10	0.4	8.2	ns
Propagation delay time, from input A to output B	t <sub>PHL</sub>										
Propagation delay time, from input B to output A	t <sub>PLH</sub>		0.7	11	0.4	8.8	0.3	8.5	0.3	8.3	
Propagation delay time, from input B to output A	t <sub>PHL</sub>										
Disable time, from input OE to output A	t <sub>PHZ</sub>		0.3	9.4	0.3	9.4	0.3	9.4	0.3	9.4	
Disable time, from input OE to output A	t <sub>PLZ</sub>										
Disable time, from input OE to output B	t <sub>PHZ</sub>		2	32.7	1.8	13.7	1.4	12	0.7	9.7	
Disable time, from input OE to output B	t <sub>PLZ</sub>										
Enable time, from input OE to output A	t <sub>PZH</sub>		0.7	10.4	0.7	10.4	0.7	10.4	0.7	10.4	
Enable time, from input OE to output A	t <sub>PZL</sub>										
Enable time, from input OE to output B	t <sub>PZH</sub>		1.5	31.6	1.3	15.4	1	12.1	0.9	10	
Enable time, from input OE to output B	t <sub>PZL</sub>										

See footnote at end of table.

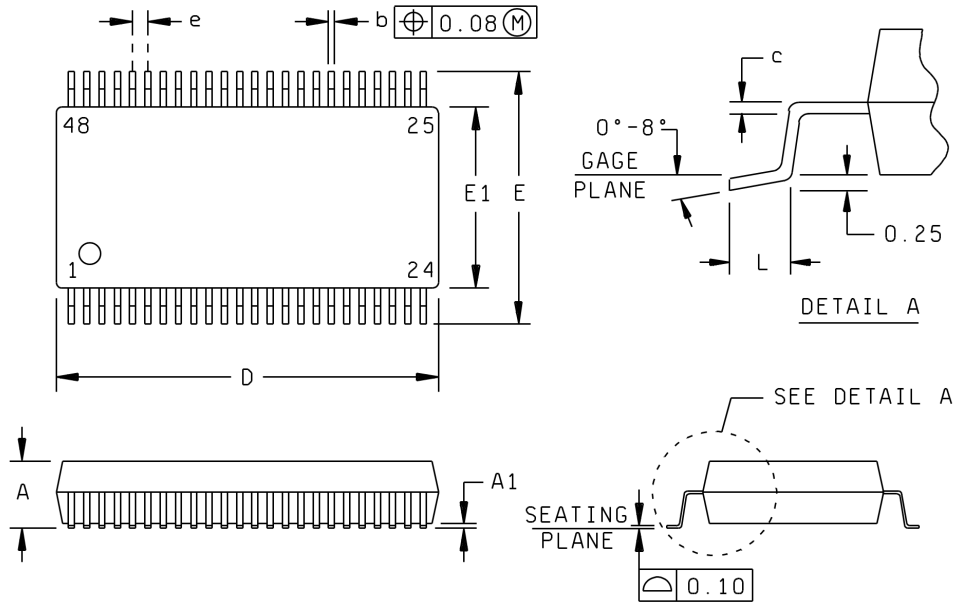
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Test	Symbol	Conditions 2/ unless otherwise specified	V <sub>CCA</sub> = V <sub>CCB</sub> = 1.8 V	V <sub>CCA</sub> = V <sub>CCB</sub> = 2.5 V	V <sub>CCA</sub> = V <sub>CCB</sub> = 3.3 V	V <sub>CCA</sub> = V <sub>CCB</sub> = 5 V	Unit
			TYP	TYP	TYP	TYP	
<b>Operating Characteristics</b>							
A port input, B port output	C <sub>pdA</sub> 9/	C <sub>L</sub> = 0,	2	2	2	3	pF
B port input, A port output		f = 10 MHz,	18	19	19	22	
A port input, B port output	C <sub>pdB</sub> 9/	t <sub>r</sub> = t <sub>f</sub> = 1 ns	18	19	20	22	
B port input, A port output			2	2	2	2	

1. Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2. Over recommended operating free air temperature range.
3. V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.
4. V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.
5. The bus hold circuit can sink at least the minimum low sustaining current at V<sub>IL</sub> max. I<sub>BHL</sub> should be measured after lowering V<sub>IN</sub> to GND and then raising it to V<sub>IL</sub> max.
6. The bus hold circuit can source at least the minimum high sustaining current at V<sub>IH</sub> min. I<sub>BHH</sub> should be measured after raising V<sub>IN</sub> to V<sub>CC</sub> and then lowering it to V<sub>IH</sub> min.
7. An external driver must source at least I<sub>BHLO</sub> to switch this node from low to high.
8. An external driver must sink at least I<sub>BHHO</sub> to switch this node from high to low.
9. Power dissipation capacitance per transceiver.

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Case X



Dimensions					
Symbol	Min	Max	Symbol	Min	Max
A		1.20	e	0.50 BSC	
A1	0.05	0.15	E	6.00	6.20
b	0.17	0.27	E1	7.90	8.30
c	0.15 NOM		L	0.50	0.75
D	12.40	12.60			

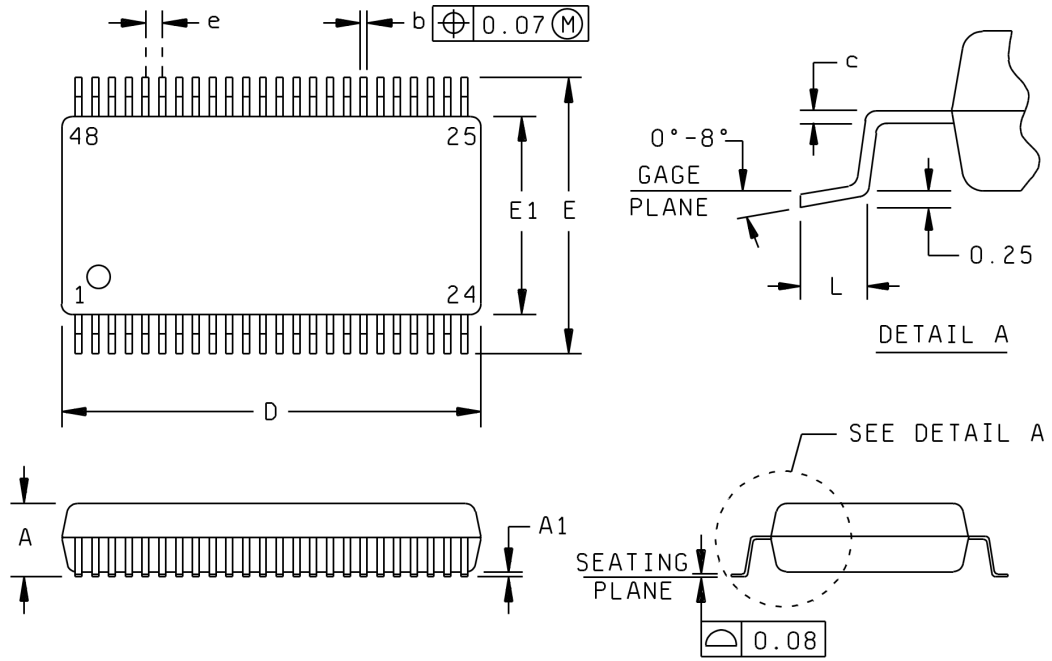
Notes:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion not to exceed 0.15.
4. Fall within JEDEC MO-153.

FIGURE 1. Case outlines.

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Case Y



Dimensions					
Symbol	Min	Max	Symbol	Min	Max
A		1.20	e	0.40 BSC	
A1	0.05	0.15	E	4.30	4.50
b	0.13	0.23	E1	6.20	6.60
c	0.16 NOM		L	0.50	0.75
D	9.60	9.80			

Notes:

5. All linear dimensions are in millimeters.
6. This drawing is subject to change without notice.
7. Body dimensions do not include mold flash or protrusion not to exceed 0.15.
8. Fall within JEDEC MO-153.

FIGURE 1. Case outlines - Continued.

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Pin No.	Signal name	Pin No.	Signal name
1	1DIR	25	2 $\overline{\text{OE}}$
2	1B1	26	2A8
3	1B2	27	2A7
4	GND	28	GND
5	1B3	29	2A6
6	1B4	30	2A5
7	VCCB	31	VCCA
8	1B5	32	2A4
9	1B6	33	2A3
10	GND	34	GND
11	1B7	35	2A2
12	1B8	36	2A1
13	2B1	37	1A8
14	2B2	38	1A7
15	GND	39	GND
16	2B3	40	1A6
17	2B4	41	1A5
18	VCCB	42	VCCA
19	2B5	43	1A4
20	2B6	44	1A3
21	GND	45	GND
22	2B7	46	1A2
23	2B8	47	1A1
24	2DIR	48	1 $\overline{\text{OE}}$

FIGURE 2. Terminal connections.

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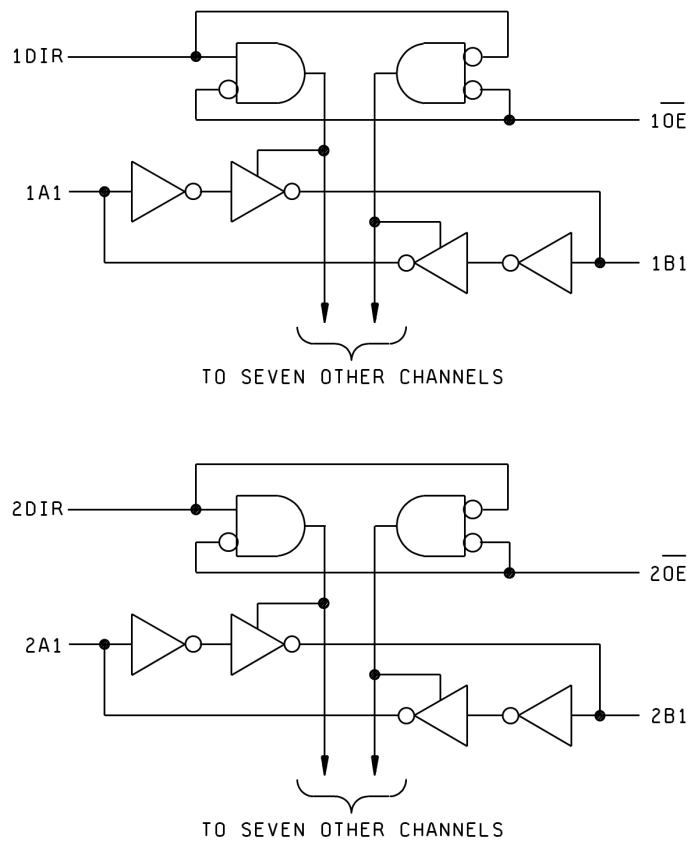
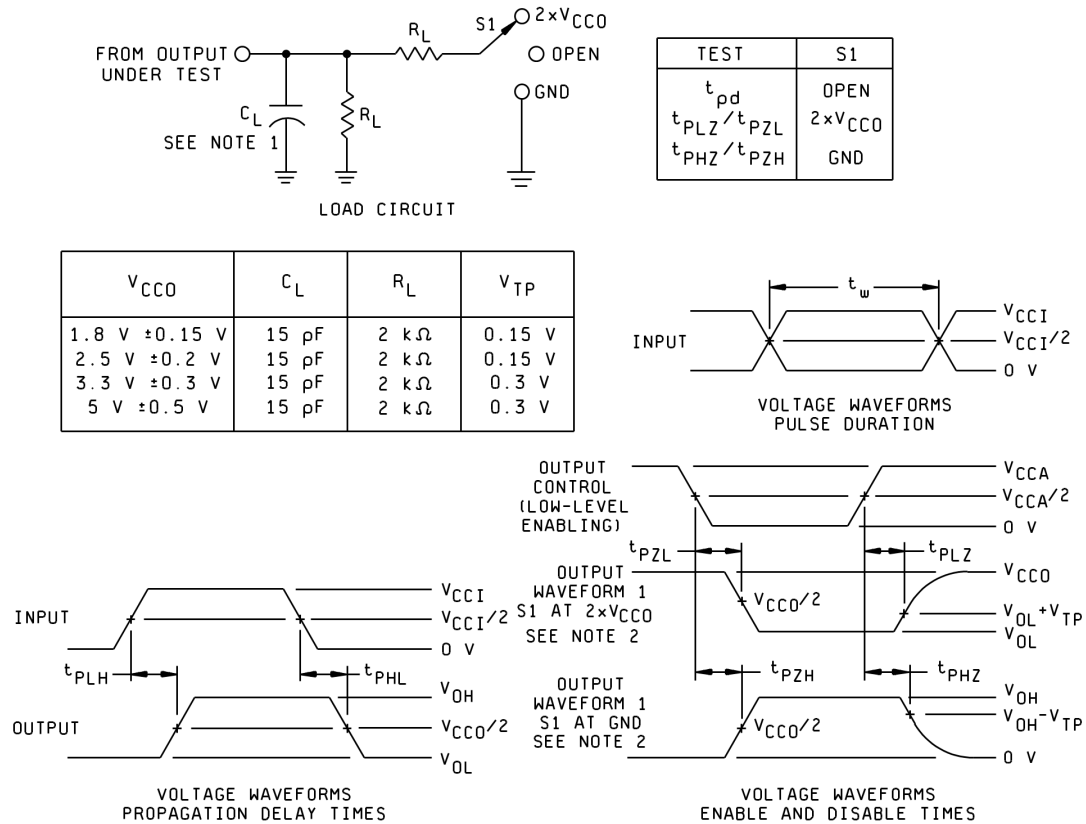


FIGURE 3. Logic diagram.

Control	Inputs	Output	circuits	Operation
$\overline{OE}$	DIR	A Port	B Port	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

FIGURE 4. Function Table

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Notes:

- $C_L$  includes probe and test fixture capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_o = 50 \Omega$ ,  $dv/dt \geq 1 \text{ V/ns}$ .
- The outputs are measured one at a time with one transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same  $t_{en}$ .
- $t_{PLH}$  and  $t_{PHL}$  are the same  $t_{pd}$ .
- $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
- $V_{CC0}$  is the  $V_{CC}$  associated with the input port
- All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and voltage waveforms.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/09605-01XE	01295	CLVCH16T245MDGGREP	8UT245MEP
V62/09605-01YE	01295	CLVCH16T245MDGVREP	LDHT245MEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
Semiconductor Group  
8505 Forest Lane  
P.O. Box 660199  
Dallas, TX 75243

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