REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Correct the maximum operating temperature range in section 1.1, 1.3 and 1.4. - phn	09-08-18	Thomas M. Hess
B	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	17-01-24	Thomas M. Hess

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**		B	B	B	B	B	B	B	B	B	B	B								
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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 08-12-10	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, DIGITAL, LOW VOLTAGE HIGH SPEED QUADRUPLE DIFFERENTIAL LINE DRIVER WITH ±15 kV ESD PROTECTION, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/09603**
	REV B	**PAGE** 1 **OF** 11

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low voltage high speed quadruple differential line driver with ±15 kV ESD protection microcircuit, with an operating temperature range of -55°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/09603	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AM26LV31E-EP	Low voltage high speed quadruple differential line driver with ±15 kV ESD protection

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	MS-012	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to +6.0 V 2/
Input voltage range (V_I)	-0.5 V to + 6.0 V
Output voltage range (V_O)	-0.5 V to +6.0 V
Input clamp current (I_{IK}) ($V_I < 0$)	-20 mA
Output clamp current (I_{OK}) ($V_O < 0$)	-20 mA
Continuous output current (I_O)	±150 mA
Continuous current through VCC or GND	±200 mA
Package thermal impedance (θ_{JA})	73°C/W 3/ 4/
Operating virtual junction temperature range (T_J)	+150°C
Storage temperature range	-65°C to +150°C
Operating free-air temperature range (T_A)	-55°C to +105°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	3.0 V to 3.6 V
Input voltage (V_I)	0 V to 5.5 V
Minimum high level input voltage (V_{IH})	2.0 V
Maximum low level input voltage (V_{IL})	0.8 V
Maximum high level output current (I_{OH})	-30 mA
Maximum low level output current (I_{OL})	+30 mA
Operating free-air temperature range (T_A)	-55°C to +105°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ All voltage values, except differential input voltage are with respect to network GND.

3/ Maximum power dissipation is a function of T_J (max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A) / \theta_{JA}$. Selecting the maximum of +150°C can affect reliability.

4/ The package thermal impedance is calculated in accordance with JESD 51-7.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
TIA/EIA-422-B	–	Electrical Characteristics of Balanced Voltage Digital Interface Circuits.

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

INTERNATIONAL ELECTROTECHNICAL COMMISSION (IEC)

IEC 61000-4-2 – Testing and measurement techniques –Electrostatic discharge immunity test

(Copies of these documents are available online at http:/www.iec.ch or IEC Regional Center for America (IEC-ReCNA) , 446 Main St., 16th Floor, Worcester, MA 01608).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function table. The function table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Test circuits. The test circuits shall be as shown in figures 5.

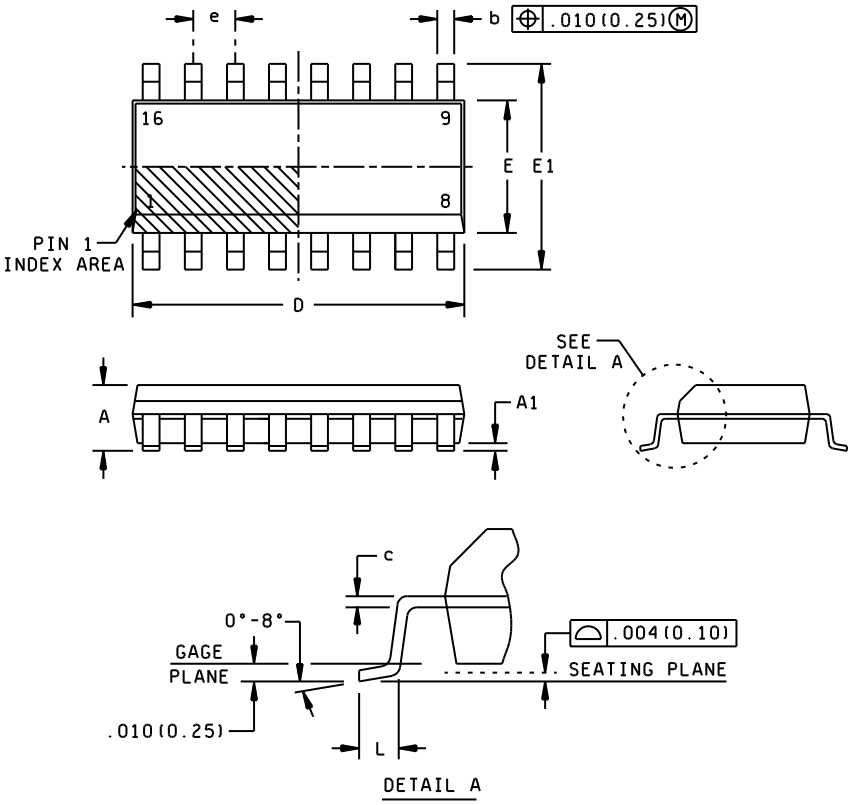
3.5.6 Timing waveforms. The timing waveforms shall be as shown in figures 6-8.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Limits		Unit
			Min	Max	
High level output voltage	V_{OH}	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = -20 mA	2.4		V
Low level output voltage	V_{OL}	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA		0.4	
Differential output voltage	$\|V_{OD1}\|$	I_O = 0 mA	2	4	
Differential output voltage	$\|V_{OD2}\|$	R_L = 100 Ω, See figure 5 3/	2		
Change in magnitude of differential output voltage	$\Delta\|V_{OD}\|$	R_L = 100 Ω, See figure 5 3/		±0.4	
Common mode output voltage	V_{OC}	R_L = 100 Ω, See figure 5 3/	1.5	2	
Change in magnitude of common mode output voltage	$\Delta\|V_{OC}\|$	R_L = 100 Ω, See figure 5 3/		±0.4	
Output current with power off	$I_{O(OFF)}$	V_{CC} = 0, V_O = -0.25 V or 5.5 V		±127	µA
High impedance state output current	I_{OZ}	V_O = -0.25 V or 5.5 V, G = 0.8 V or $\overline{G}$ = 2 V		±127	
Input current	II	V_{CC} = 0 or 3.6 V, V_I =0 or 5.5 V		±10	
Short circuit output current	I_{OS}	V_O = V_{CC} or GND 4/	-30	-150	mA
Supply current (total package)	I_{CC}	V_I = V_{CC} or GND, No load, enable		100	µA
Power dissipation capacitance	C_{pd}	No load, V_{CC} = 3.3 V, T_A = 25°C 5/	160 TYP		pF
Switching characteristics					
Propagation delay time, high to low level output	t_{PHL}	See figure 6	4	12	ns
Propagation delay time, low to high level output	t_{PLH}		3.5	12	
Transition time (tr or tf)	t_t	See figure 6		10	
Output enable time to high level	t_{PZH}	See figure 7		20	
Output enable time to low level	t_{PZL}	See figure 8		20	
Output disable time from high level	t_{PHZ}	See figure 7		20	
Output disable time from low level	t_{PLZ}	See figure 8		20	
Pulse skew	$t_{sk(p)}$	See figure 6 6/ 7/		3	
Skew limit (pin to pin)	$t_{sk(o)}$			1.5	
Skew limit (device to device)	$t_{sk(lim)}$			3	
Maximum operating frequency	f_{max}	See figure 6	32 TYP		MHz
ESD protection					
Driver output		HBM	±15		kV
		IEC6100-4-2, Air gap discharge	±15		
		IEC6100-4-2, Constant discharge	±8		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ Over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted).
3/ Refer to TIA-EIA-422 for exact conditions.
4/ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
5/ C_{pd} determined the no load dynamic current consumption: $I_S = C_{pd} \times V_{CC} \times f + I_{CC}$
6/ Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
7/ Skew limit (device to device) is the maximum difference in propagation delay times between any two channels of any two devices.

Case X



Symbols	Inches		Millimeters		Symbols	Inches		Millimeters	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	0.069	---	1.75	E	0.150	0.157	3.80	4.00
A1	0.004	0.010	0.10	0.25	E1	0.228	0.244	5.80	6.20
b	0.012	0.020	0.31	0.51	e	0.050 BSC		1.27 BSC	
c	0.007	0.010	0.17	0.25	L	0.016	0.050	0.40	1.27
D	0.386	0.394	9.80	10.00					

NOTES:
1. All linear dimensions are in inches (millimeters).
2. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch (0.15 mm) per end.
3. Body width does not include interlead flash. Interlead flash shall not exceed .017 inch (0.43 mm) per side.
4. Falls within JEDEC MS-012 variation AC.

FIGURE 1. Case outlines - Continued.

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	1A	9	3A
2	1Y	10	3Y
3	1Z	11	3Z
4	G	12	$\overline{G}$
5	2Z	13	4Z
6	2Y	14	4Y
7	2A	15	4A
8	GND	16	V_{CC}

FIGURE 2. Terminal connections.

Input	Enables		Outputs	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

FIGURE 3. Function table.

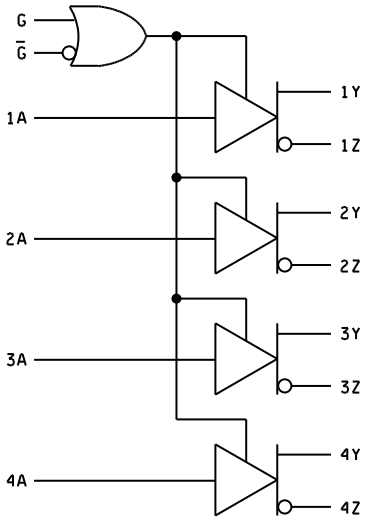


FIGURE 4. Logic diagram.

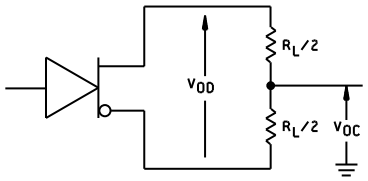
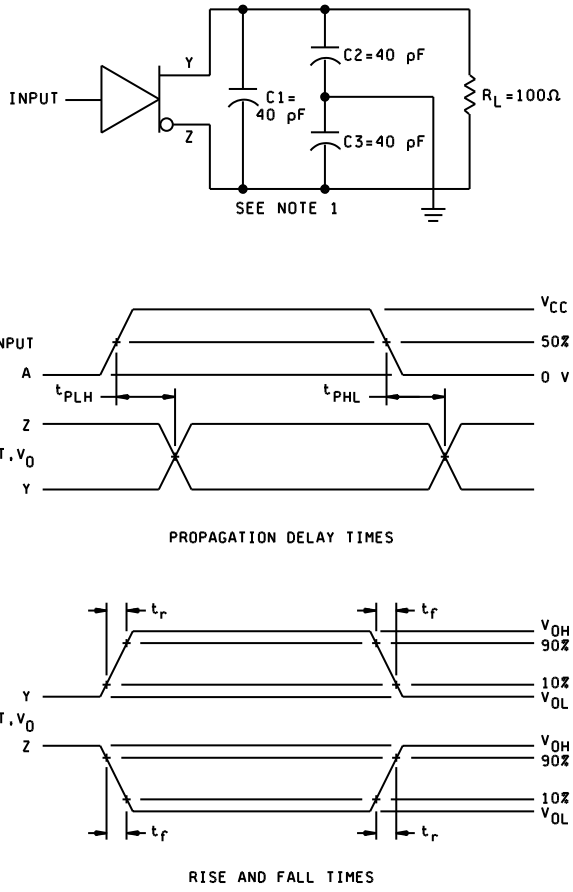


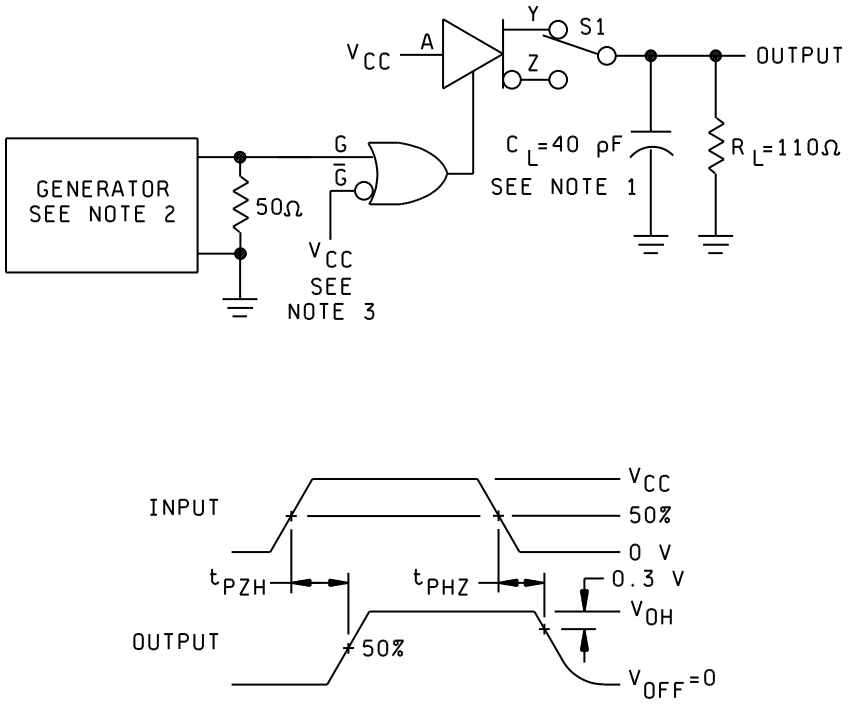
FIGURE 5. Test circuit, V_{OD} and V_{OC}.



NOTES:

1. C_L include probe and jig capacitance.
2. The input pulse is supplied by generators having the following characteristics: PRR ≤ 32 MHz, 50 % duty cycle, tr and tf ≤ 2 ns.

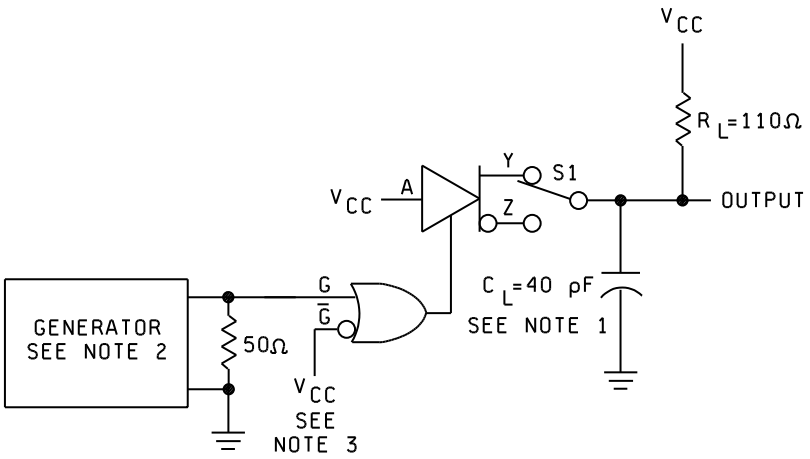
FIGURE 6. Timing waveforms, t_{PHL} and t_{PLH}.

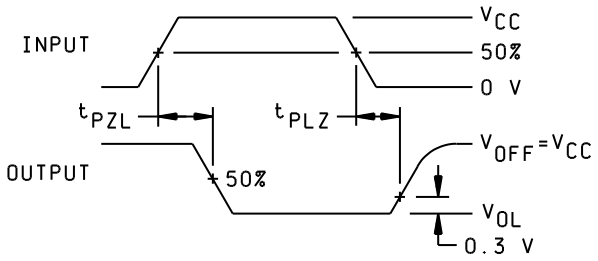


NOTES:

1. C_L include probe and jig capacitance.
2. The input pulse is supplied by generators having the following characteristics: PRR = 10 MHz, 50 % duty cycle, $t_r = t_f \leq 2$ ns.
3. To test the active low enable $\overline{G}$, ground G and apply an inverted waveform $\overline{G}$.

FIGURE 7. Timing waveforms, t_{PZH} and t_{PHZ}.





NOTES:

1. C_L include probe and jig capacitance.
2. The input pulse is supplied by generators having the following characteristics: PRR = 10 MHz, 50 % duty cycle, $t_r = t_f \leq 2$ ns.
3. To test the active low enable $\overline{G}$, ground G and apply an inverted waveform $\overline{G}$.

FIGURE 8. Timing waveforms, t_{PZL} and t_{PLZ}.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/09603-01XE	01295	AM26LV31ESDREP	A26LV31ESP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's datasheet, or at website www.ti.com.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493