REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate paragraphs to current VID description requirements. - DRH	22-09-26	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A					
SHEET	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40					
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

PMIC N/A

Original date of drawing

09-04-07

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TITLE
MICROCIRCUIT, DIGITAL, MIXED SIGNAL MICROCONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/09601
REV A		PAGE 1 OF 40

AMSC N/A

5962-V100-22

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance mixed signal microcontroller microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/09601	-	01	X	A
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	MSP430F249-EP	Mixed signal microcontroller

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	64	JEDEC MO-220	Plastic quad flatpack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Voltage applied at V_{CC} to V_{SS} ..... -0.3 V to 4.1 V
Voltage applied to any pin ..... -0.3 V to V_{CC} + 0.3 V 2/
Diode current at any device terminal ..... ±2 mA
Storage temperature range, T_{STG} (unprogrammed device) ..... -55°C to 150°C 3/
Storage temperature range, T_{STG} (programmed device) ..... -55°C to 125°C 3/

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

2/ All voltages referenced to V_{SS}. The JTAG fuse blow voltage, VFB, is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.

3/ Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

1.4 Recommended operating conditions. 4/

Supply voltage during program execution (V_{CC}) (AV_{CC} = DV_{CC} = V_{CC}) ..... 1.8 V to 3.6 V 5/
Supply voltage during flash memory programming (V_{CC}) (AV_{CC} = DV_{CC} = V_{CC}) ..... 2.2 V to 3.6 V 5/
Supply voltage (V_{SS}) (AV_{SS} = DV_{SS} = V_{SS})..... 0 V
Processor frequency f_{SYSTEM} (Maximum MCLK frequency): 6/ 7/ 8/
V_{CC} = 1.8 V, Duty Cycle 50% ±10% ..... 4.15 MHz
V_{CC} = 2.7 V, Duty Cycle 50% ±10% ..... 12 MHz
V_{CC} ≥ 3.3 V, Duty Cycle 50% ±10% ..... 16 MHz
Flash temperature range:
Read ..... -55°C to 125°C
Write ..... -55°C to 125°C
Operating free air temperature range, T_A ..... -55°C to 125°C

2. APPLICABLE DOCUMENTS

SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC JEP95 – Registered and Standard Outlines for Semiconductor Devices.
JEDEC J-STD-020 – Joint IPC/JEDEC standard for moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices.

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
5/ It is recommended to power AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AVCC and DVCC can be tolerated during power up.
6/ The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
7/ Modules might have a different maximum input clock specification. Refer to the data sheet from manufacturer.
8/ See figure 4.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Operating area. The operating area shall be as shown in figure 4.

3.5.5 Active mode supply current. The active mode supply current shall be as shown in figure 5.

3.5.6 POR/Brownout reset. The POR/Brownout reset shall be as shown in figure 6-8.

3.5.7 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as shown in figure 9-15.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	T_A	V_{CC}	Device type	Limits		Unit
						Min	Max	
Active mode supply current (into DV_{CC} + AV_{CC}) Excluding External current 3/ 4/								
Active mode (AM) current (1 MHz)	$I_{AM, 1MHz}$	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 32,768 Hz, Program executes from flash, BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1 MHz CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	-55°C to 105°C	2.2 V	01	275 TYP		µA
			125°C				318	
			-55°C to 105°C	3 V		386 TYP		
			125°C				449	
Active mode (AM) current (1 MHz)	$I_{AM, 1MHz}$	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 32,768 Hz, Program executes in RAM, BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1 MHz CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	-55°C to 105°C	2.2 V		230 TYP		µA
			125°C				267	
			-55°C to 105°C	3 V		321 TYP		
			125°C				370	
Active mode (AM) current (4 kHz)	$I_{AM, 4kHz}$	$f_{MCLK} = f_{SMCLK} = f_{ACLK}$ = 32,768 Hz/8 = 4096 Hz, f_{DCO} = 0 Hz, Program executes in flash, SELMx = 11, SELS = 1, DIVMx = DIVSx = DIVAx = 11, CPUOFF = 0, SCGO = 0, SCG1 = 0, OSCOFF = 0	-55°C to 105°C	2.2 V		1.5 TYP		µA
			125°C				10.5	
			-55°C to 105°C	3 V		2 TYP		
			125°C				12.2	
Active mode (AM) current (100 kHz)	$I_{AM, 100kHz}$	$f_{MCLK} = f_{SMCLK} = f_{DCO(0,0)} \approx$ 100 kHz, f_{ACLK} = 0 Hz, Program executes in flash, RSELx = 0, DCOx = 0, CPUOFF = 0, SCGO = 0, SCG1 = 0, OSCOFF = 1	-55°C to 105°C	2.2 V		55 TYP		µA
			125°C				81	
			-55°C to 105°C	3 V		67 TYP		
			125°C				100	
Low power mode 0, (LPM0) current 5/	$I_{LPM0, 1 MHz}$	f_{MCLK} = 0 MHz, $f_{SMCLK} = f_{DCO}$ = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1 MHz, DCOCTL = CALDCO_1 MHz, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	-55°C to 105°C	2.2 V		60 TYP		µA
			125°C				88	
			-55°C to 105°C	3 V		75 TYP		
			125°C				98	
Low power mode 0, (LPM0) current 5/	$I_{LPM0, 100 kHz}$	f_{MCLK} = 0 MHz, $f_{SMCLK} = f_{DCO(0,0)} \approx$ 100 kHz, f_{ACLK} = 0 Hz, RSELx = 0, DCOx = 0, CPUOFF = 1, SCGO = 0, SCG1 = 0, OSCOFF = 1	-55°C to 105°C	2.2 V		33 TYP		µA
			125°C				45	
			-55°C to 105°C	3 V		36 TYP		
			125°C				50	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	T_A	V_{CC}	Device type	Limits		Unit
						Min	Max	
Active mode supply current (into DVCC + AVCC) Excluding External current - Continued 3/ 4/								
Low power mode 2 (LPM2) current 6/	I_{LPM2}	$f_{MCLK} = f_{SMCLK}$= 0 MHz, f_{DCO} = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1 MHz, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	-55°C to 105°C	2.2 V	01	20 TYP		µA
			125°C				42	
			-55°C to 105°C	3 V		23 TYP		
			125°C				48	
Low power mode 3 (LPM3) current 6/	$I_{LPM3, LFXT1}$	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0 MHz, f_{ACLK} = 32,768 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-55°C	2.2 V		0.8 TYP		µA
			25°C				1.3	
			105°C				15	
			125°C				22	
			-55°C	3 V		0.9 TYP		
			25°C				1.4	
			105°C				17	
			125°C				27	
Low power mode 3 current (LPM3) 6/	$I_{LPM3, VLO}$	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0 MHz, f_{ACLK} = from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-55°C	2.2 V		0.3 TYP		µA
			25°C				0.9	
			105°C				4.5	
			125°C				15	
			-55°C	3 V		0.4 TYP		
			25°C				1	
			105°C				5.5	
			125°C				16	
Low power mode 4 current (LPM4) 7/		$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0 MHz, f_{ACLK} = 0 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	-55°C	2.2 V/ 3 V		0.1 TYP		µA
			25°C				0.5	
			105°C				13	
			125°C				22	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$ 2/ unless otherwise specified	V_{CC}	Device type	Limits		Unit
					Min	Max	
Schmitt-trigger inputs – ports P1, P2, P3, P4, P5, P6, RST/$\overline{\text{RST}}$, JTAG, XIN, and XT2IN) 8/							
Positive going input threshold voltage	V_{IT+}			01	0.45 V_{CC}	0.75 V_{CC}	V
			2.2 V		1	1.65	
			3 V		1.35	2.25	
Negative going input threshold voltage	V_{IT-}				0.25 V_{CC}	0.55V_{CC}	V
			2.2 V		0.55	1.2	
			3 V		0.75	1.65	
Input voltage hysteresis (V_{IT+} - V_{IT-})	V_{hys}		2.2 V		0.2	1	V
			3 V		0.3	1	
Pullup/Pulldown resistor	R_{Pull}	Pullup: $V_{IN} = V_{SS}$; Pulldown: $V_{IN} = V_{CC}$			20	50	kΩ
Input capacitance	C_I	$V_{IN} = V_{SS}$ or V_{CC}			5 TYP		pF
Inputs – ports P1 and P2							
External interrupt timing	$t_{(int)}$	Port P1, P2: P1.x to P2.x, external trigger pulse width to set interrupt flag 9/	2.2 V/ 3 V	01	20		ns
Timer_A, Timer_B capture timing	t_{cap}	TA0, TA1, TA2	2.2 V		62		
		TB0, TB1, TB2, TB3, TB4, TB5, TB6	3 V		50		
Timer_A, Timer_B clock frequency	f_{TAext}	TACLK, TBCLK, INCLK: $t_{(H)} = t_{(L)}$	2.2 V			8	MHz
externally applied to pin	f_{TBext}		3 V			10	
Timer_A, Timer_B clock frequency	f_{TAint}	SNCLK or ACLK signal selected	2.2 V			8	
	f_{TBint}		3 V			10	
Leakage current – ports P1, P2, P3, P4, P5, and P6							
High impedance leakage current	$I_{lkg(Px.x)}$	10/ 11/	2.2 V/ 3 V	01		±50	nA
Standard inputs - $\overline{\text{RST}}$/NMI							
Low level input voltage	V_{IL}		2.2 V/ 3 V	01	V_{SS}	V_{SS} + 0.6	V
High level input voltage	V_{IH}				0.8V_{CC}	V_{CC}	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$ 2/ unless otherwise specified	V_{CC}	Device type	Limits		Unit
					Min	Max	
Outputs – ports P1, P2, P3, P4, P5, and P6							
High level output voltage	V_{OH}	$I_{OH(max)}$ = -1.5 mA 12/	2.2 V	01	V_{CC}–0.25	V_{CC}	V
		$I_{OH(max)}$ = -6 mA 13/			V_{CC}–0.6	V_{CC}	
		$I_{OH(max)}$ = -1.5 mA 12/	3 V		V_{CC}–0.25	V_{CC}	
		$I_{OH(max)}$ = -6 mA 13/			V_{CC}–0.6	V_{CC}	
Low level output voltage	V_{OL}	$I_{OL(max)}$ = 1.5 mA 12/	2.2 V		V_{SS}	V_{SS}+0.25	V
		$I_{OL(max)}$ = 6 mA 13/			V_{SS}	V_{SS}+0.6	
		$I_{OL(max)}$ = 1.5 mA 12/	3 V		V_{SS}	V_{SS}+0.25	
		$I_{OL(max)}$ = 6 mA 13/			V_{SS}	V_{SS}+0.6	
Output frequency – ports P1, P2, P3, P4, P5, and P6							
Port output frequency (with load)	$f_{Px.y}$	P1.4/SMCLK, C_L = 20 pF, R_L = 1 kΩ 14/ 15/	2.2 V	01	DC	10	MHz
			3 V		DC	12	
Clock output frequency	f_{Port_CLK}	P2.0/ACLK/CA2, P1.4/SCMCLK, CL = 20 pF, R_L = 1 kΩ 15/	2.2 V		DC	12	MHz
			3 V		DC	16	
Duty cycle of output frequency	$t_{(Xdc)}$	P1.0/TACLK/CAOUT, C_L = 20 pF, LF mode			30		%
		P1.0/TACLK/CAOUT, C_L = 20 pF, XT1 mode			40		
		P1.0/TA0, C_L = 20 pF, XT1 mode			40		
		P1.0/TA0, C_L = 20 pF, DCO			50% - 15 ns	50% + 15 ns	
		P1.4/SMCLK, C_L = 20 pF, XT2 MODE			40	60	%
		P1.4/SMCLK, C_L = 20 pF, DCO			50% - 15 ns	50% + 15 ns	
POR/brownout reset (BOR) 16/ 17/							
Operating voltage	$V_{CC(start)}$	$dV_{CC}/dt \le 3$ V/s See figure 6		01	0.7x$V_{(B_IT-)}$ TYP		V
Negative going V_{CC} reset threshold voltage	$V_{(B\_IT-)}$	$dV_{CC}/dt \le 3$ V/s See figure 6-8				1.71	V
V_{CC} reset threshold hysteresis	$V_{hys(B\_IT-)}$	$dV_{CC}/dt \le 3$ V/s See figure 6			70	210	mV
BOR reset release delay time	$t_{d(BOR)}$	See figure 6				2000	µs
Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally	$t_{(reset)}$		2.2 V/ 3 V		2		µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$ 2/ unless otherwise specified		Device type	Limits		Unit
					Min	Max	
SVS (supply voltage supervisor/monitor)							
	$t_{(SVSR)}$	dV_{CC}/dt > 30 V/ms See figure 9		01	5	150	µs
		$dV_{CC}/dt \le 30$ V/ms				2000	
	$t_{d(SVSon)}$	SVSON, switch from VLD = 0 to VLD ≠ 0, V_{CC} = 3 V			20	150	
	t_{settle}	VLD ≠ 0 19/				12	
	$V_{(SVSstart)}$	VLD ≠ 0, $V_{CC}/dt \le 3$ V/s See figure 9				1.7	V
	$V_{hys(SVS\_IT-)}$	$dV_{CC}/dt \le 3$ V/s See figure 9	VLD = 1		70	210	mV
			VLD = 2 to 14		0.001 x $V_{(SVS\_IT-)}$	0.016 x $V_{(SVS\_IT-)}$	
		$dV_{CC}/dt \le 3$ V/s, External voltage applied on A7, See figure 9	VLD = 15		4.4	20	mV
	$V_{(SVS\_IT-)}$	$dV_{CC}/dt \le 3$ V/s See figure 9-10	VLD = 1		1.8	2.05	V
			VLD = 2		1.94	2.25	
			VLD = 3		2.05	2.37	
			VLD = 4		2.14	2.48	
			VLD = 5		2.24	2.60	
			VLD = 6		2.33	2.71	
			VLD = 7		2.46	2.86	
			VLD = 8		2.58	3.00	
			VLD = 9		2.69	3.13	
			VLD = 10		2.83	3.29	
			VLD = 11		2.94	3.42	
			VLD = 12		3.11	3.61 18/	
			VLD = 13		3.24	3.76 18/	
			VLD = 14		3.43	3.99 18/	
		$dV_{CC}/dt \le 3$ V/s, External voltage applied on A7, See figure 9-10	VLD = 15		1.1	1.3	
	$I_{CC(SVS)}$ 20/	VLD ≠ 0, V_{CC} = 2.2 V/3 V				15	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$ 2/ unless otherwise specified	V_{CC}	Device type	Limits		Unit
					Min	Max	
DCO frequency							
Supply voltage range	V_{CC}	RSELx < 14		01	1.8	3.6	V
		RSELx = 14			2.2	3.6	
		RSELx = 15			3.0	3.6	
DCO frequency (0, 0)	$f_{DCO(0,0)}$	RSELx = 0, DCOx = 0, MODx = 0	2.2 V/ 3V		0.06	0.14	MHz
DCO frequency (0, 3)	$f_{DCO(0, 3)}$	RSELx = 0, DCOx = 3, MODx = 0			0.07	0.17	
DCO frequency (1,3)	$f_{DCO(1, 3)}$	RSELx = 1, DCOx = 3, MODx = 0			0.10	0.20	
DCO frequency (2, 3)	$f_{DCO(2, 3)}$	RSELx = 2, DCOx = 3, MODx = 0			0.14	0.28	
DCO frequency (3, 3)	$f_{DCO(3, 3)}$	RSELx = 3, DCOx = 3, MODx = 0			0.20	0.40	
DCO frequency (4, 3)	$f_{DCO(4, 3)}$	RSELx = 4, DCOx = 3, MODx = 0			0.28	0.54	
DCO frequency (5, 3)	$f_{DCO(5, 3)}$	RSELx = 5, DCOx = 3, MODx = 0			0.39	0.77	
DCO frequency (6, 3)	$f_{DCO(6, 3)}$	RSELx = 6, DCOx = 3, MODx = 0			0.54	1.06	
DCO frequency (7, 3)	$f_{DCO(7, 3)}$	RSELx = 7, DCOx = 3, MODx = 0			0.80	1.50	
DCO frequency (8, 3)	$f_{DCO(8, 3)}$	RSELx = 8, DCOx = 3, MODx = 0			1.10	2.10	
DCO frequency (9, 3)	$f_{DCO(9, 3)}$	RSELx = 9, DCOx = 3, MODx = 0			1.60	3.00	
DCO frequency (10, 3)	$f_{DCO(10, 3)}$	RSELx = 10, DCOx = 3, MODx = 0			2.50	4.30	
DCO frequency (11, 3)	$f_{DCO(11, 3)}$	RSELx = 11, DCOx = 3, MODx = 0			3.00	5.50	
DCO frequency (12, 3)	$f_{DCO(12, 3)}$	RSELx = 12, DCOx = 3, MODx = 0			4.30	7.30	
DCO frequency (13, 3)	$f_{DCO(13, 3)}$	RSELx = 13, DCOx = 3, MODx = 0			6.00	9.60	
DCO frequency (14, 3)	$f_{DCO(14, 3)}$	RSELx = 14, DCOx = 3, MODx = 0			8.60	13.9	
DCO frequency (15, 3)	$f_{DCO(15, 3)}$	RSELx = 15, DCOx = 3, MODx = 0	3 V		12.0	18.5	
DCO frequency (15, 7)	$f_{DCO(15, 7)}$	RSELx = 15, DCOx = 7, MODx = 0	3 V		16.0	26.0	
Frequency step between range RSEL and RSEL+1	S_{RSEL}	SRSEL = $f_{DCO(RSEL+1, DCO)} / f_{DCO(RSEL,DCO)}$	2.2 V/ 3 V		1.35	2.00	ratio
Frequency step between tap DCO and DCO+1	S_{DCO}	SDCO = $f_{DCO(RSEL,DCO+1)}/f_{DCO(RSEL,DCO)}$			1.07	1.16	ratio
Duty cycle		Measured at P1.4/SMCLK			40	60	%

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$ 2/ unless otherwise specified	V_{CC}	Device type	Limits		Unit
					Min	Max	
Calibrated DCO frequencies (Tolerance at Calibration)							
Frequency tolerance at calibration		$T_A = 25°C$	3 V	01	-1	1	%
1 MHz calibration value	$f_{CAL(1\ MHz)}$	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, Gating time: 5 ms, $T_A = 25°C$			0.990	1.010	MHz
8 MHz calibration value	$f_{CAL(8\ MHz)}$	BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz, Gating time: 5 ms, $T_A = 25°C$			7.920	8.080	
12 MHz calibration value	$f_{CAL(12\ MHz)}$	BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz, Gating time: 5 ms, $T_A = 25°C$			11.88	12.12	
16 MHz calibration value	$f_{CAL(16\ MHz)}$	BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz, Gating time: 2 ms, $T_A = 25°C$			15.84	16.16	
Calibrated DCO frequencies (Tolerance over temperature)							
1 MHz tolerance over temperature			3 V	01	-2.5	2.5	%
8 MHz tolerance over temperature					-2.5	2.5	
12 MHz tolerance over temperature					-2.5	2.5	
16 MHz tolerance over temperature					-3.0	3.0	
1 MHz calibration value	$f_{CAL(1\ MHz)}$	BCSCTL1 = CALBC1_1MHz,	2.2 V		0.970	1.030	MHz
		DCOCTL = CALDCO_1MHz,	3 V		0.975	1.025	
		Gating time: 5 ms	3.6 V		0.970	1.030	
8 MHz calibration value	$f_{CAL(8\ MHz)}$	BCSCTL1 = CALBC1_8MHz,	2.2 V		7.760	8.400	
		DCOCTL = CALDCO_8MHz,	3 V		7.800	8.200	
		Gating time: 5 ms	3.6 V		7.600	8.240	
12 MHz calibration value	$f_{CAL(12\ MHz)}$	BCSCTL1 = CALBC1_12MHz,	2.2 V		11.64	12.36	
		DCOCTL = CALDCO_12MHz,	3 V		11.64	12.36	
		Gating time: 5 ms	3.6 V		11.64	12.36	
16 MHz calibration value	$f_{CAL(16\ MHz)}$	BCSCTL1 = CALBC1_16MHz,	3 V		15.52	16.48	
		DCOCTL = CALDCO_16MHz,	3.6 V		15.00	16.48	
		Gating time: 2 ms					

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$ 2/ unless otherwise specified	V_{CC}	Device type	Limits		Unit
					Min	Max	
Calibrated DCO frequencies (Tolerance over supply voltage V_{CC})							
1 MHz tolerance over V_{CC}		$T_A = 25°C$	1.8 V to 3.6 V	01	-3	3	%
8 MHz tolerance over V_{CC}			1.8 V to 3.6 V		-3	3	
12 MHz tolerance over V_{CC}			2.2 V to 3.6 V		-3	3	
16 MHz tolerance over V_{CC}			3 V to 3.6 V		-3	3	
1 MHz calibration value	$f_{CAL(1\ MHz)}$	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, Gating time: 5 ms, $T_A = 25°C$	1.8 V to 3.6 V		0.970	1.030	MHz
8 MHz calibration value	$f_{CAL(8\ MHz)}$	BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz, Gating time: 5 ms, $T_A = 25°C$	1.8 V to 3.6 V		7.760	8.240	
12 MHz calibration value	$f_{CAL(12\ MHz)}$	BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz, Gating time: 5 ms, $T_A = 25°C$	2.2 V to 3.6 V		11.64	12.36	
16 MHz calibration value	$f_{CAL(16\ MHz)}$	BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz, Gating time: 2 ms, $T_A = 25°C$	3 V to 3.6 V		15.00	16.48	
Calibrated DCO frequencies (Overall tolerance)							
1 MHz tolerance over temperature			1.8 V to 3.6 V	01	-5	+5	%
8 MHz tolerance over temperature			1.8 V to 3.6 V		-5	+5	
12 MHz tolerance over temperature			2.2 V to 3.6 V		-5	+5	
16 MHz tolerance over temperature			3 V to 3.6 V		-6	+6	
1 MHz calibration value	$f_{CAL(1\ MHz)}$	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, Gating time: 5 ms, $T_A = 25°C$	1.8 V to 3.6 V		0.950	1.050	MHz
8 MHz calibration value	$f_{CAL(8\ MHz)}$	BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz, Gating time: 5 ms	1.8 V to 3.6 V		7.6	8.4	
12 MHz calibration value	$f_{CAL(12\ MHz)}$	BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz, Gating time: 5 ms	2.2 V to 3.6 V		11.4	12.6	
16 MHz calibration value	$f_{CAL(16\ MHz)}$	BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz, Gating time: 2 ms	3 V to 3.6 V		15.00	17.00	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions -55°C ≤ T_A ≤ 125°C 2/ unless otherwise specified	V_{CC}	Device type	Limits		Unit
					Min	Max	
Wake up from lower power Modes (LPM3/4)							
DCO clock wake up time from LPM3/4 21/	$t_{DCO,LPM3/4}$	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz,	2.2 V/3 V	01		2	µs
		BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz,				1.5	
		BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz,				1	
		BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz,	3 V			1	
CPU wake up time from LPM3/4 22/	$t_{CPU,LPM3/4}$				$1/f_{MCLK} + t_{Clock,LPM3/4}$ TYP		
DCO with external resistor R_{OSC} 24/							
DCO output frequency with R_{OSC}	$f_{DCO,ROSC}$	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0, T_A = 25°C	2.2 V	01	1.8 TYP		MHz
			3 V		1.95 TYP		
Temperature drift	D_t	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0			±0.1 TYP		%/°C
Drift with V_{CC}	D_V	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0			10 TYP		%/V
Crystal Oscillator (LFXT1) Low frequency Modes 21/							
LFXT1 oscillator crystal frequency, LF mode 0, 1	$f_{LFXT1,LF}$	XTS = 0, LFXT1Sx = 0 or 1	1.8V to 3.6V	01	32,768 TYP		Hz
LFXT1 oscillator logic level square wave input frequency, LF mode	$f_{LFXT1,LF,logic}$	XTS = 0, LFXT1Sx = 3			10	50	kHz
Oscillation allowance for LF crystal	OA_{LF}	XTS = 0, LFXT1Sx = 0; $f_{LFXT1,LF}$ = 32,768 Hz, $C_{L,eff}$ = 6 pF			500 TYP		kΩ
		XTS = 0, LFXT1Sx = 0; $f_{LFXT1,LF}$ = 32,768 Hz, $C_{L,eff}$ = 12 pF			200 TYP		
Integrated effective load capacitance, LF mode 25/	$C_{L,eff}$	XTS = 0, XCAPx = 0			1 TYP		pF
		XTS = 0, XCAPx = 1			5.5 TYP		
		XTS = 0, XCAPx = 2			8.5 TYP		
		XTS = 0, XCAPx = 3			11 TYP		
LF mode	Duty cycle	XTS = 0, Measured at P1.4/ACLK, $f_{LFXT1,LF}$ = 32,768 Hz	2.2 V/3 V		30	70	%
Oscillator fault frequency threshold, LF mode 26/	$f_{Fault,LF}$	XTS = 0, LFXT1Sx = 3 27/	2.2 V/3 V		10	10000	Hz

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$ 2/ unless otherwise specified	V_{CC}	Device type	Limits		Unit
					Min	Max	
Internal very low power, Low frequency oscillator (VLO)							
VLO frequency	f_{VLO}	T_A = -55°C to 85°C	2.2 V/3 V	01	4	20	kHz
		T_A = 125°C				22	
VLO frequency temperature drift	df_{VLO}/dT	28/			0.5 TYP		%/°C
VLO frequency supply voltage drift	df_{VLO}/dV_{CC}	T_A = 25°C 29/	1.8 V to 3.6 V		4 TYP		%/V
Crystal Oscillator (LFXT1) high frequency modes 24/							
LFXT1 oscillator crystal frequency, HF mode 0	$f_{LFXT1,HF0}$	XTS = 1, LFXT1Sx = 0	1.8 V to 3.6 V	01	0.4	1	MHz
LFXT1 oscillator crystal frequency, HF mode 1	$f_{LFXT1,HF1}$	XTS = 1, LFXT1Sx = 1	1.8 V to 3.6 V		1	4	
LFXT1 oscillator crystal frequency, HF mode 2	$f_{LFXT1,HF2}$	XTS = 1, LFXT1Sx = 2	1.8 V to 3.6 V		2	10	
			2.2 V to 3.6 V		2	12	
			3 V to 3.6 V		2	16	
LFXT1 oscillator logic level square wave input frequency, HF mode	$f_{LFXT1,HF,logic}$	XTS = 1, LFXT1Sx = 3	1.8 V to 3.6 V		0.4	10	
			2.2 V to 3.6 V		0.4	12	
			3 V to 3.6 V		0.4	16	
Oscillation allowance for HF crystals See figure 11	OA_{HF}	XTS = 0, LFXT1Sx = 0; $f_{LFXT1,HF}$ = 1 MHz, $C_{L,eff}$ = 15 pF			2700 TYP		Ω
		XTS = 0, LFXT1Sx = 1; $f_{LFXT1,HF}$ = 1 MHz, $C_{L,eff}$ = 15 pF			800 TYP		
		XTS = 0, LFXT1Sx = 2; $f_{LFXT1,HF}$ = 1 MHz, $C_{L,eff}$ = 15 pF			300 TYP		
Integrated effective load capacitance, HF mode 25/	$C_{L,eff}$	XTS = 1, XCAPx = 0 30/			1 TYP		pF
HF mode	Duty cycle	XTS = 1, XCAPx = 0, Measured at P1.4/ACLK, $f_{LFXT1,HF}$ = 10 MHz	2.2 V/3 V		40	60	%
		XTS = 1, XCAPx = 0, Measured at P1.4/ACLK, $f_{LFXT1,HF}$ = 16 MHz			40	60	
Oscillator fault frequency, HF mode 26/	$f_{Fault,HF}$	XTS = 1, LFXT1Sx = 3, XCAPx = 0 27/	2.2 V/3 V		30	300	kHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$ 2/ unless otherwise specified	V_{CC}	Device type	Limits		Unit
					Min	Max	
Crystal Oscillator, XT2 24/							
XT2 oscillator crystal frequency, mode 0	f_{XT2}	XT2S = 0	1.8 V to 3.6 V	01	0.4	1	MHz
XT2 oscillator crystal frequency, mode 1	f_{XT2}	XT2S = 1	1.8 V to 3.6 V		1	4	
XT2 oscillator crystal frequency, mode 2	f_{XT2}	XT2S = 2	1.8 V to 3.6 V		2	10	
			2.2 V to 3.6 V		2	12	
			3 V to 3.6 V		2	16	
XT2 oscillator logic level square wave input frequency	f_{XT2}	XT2S = 3	1.8 V to 3.6 V		0.4	10	
			2.2 V to 3.6 V		0.4	12	
			3 V to 3.6 V		0.4	16	
Oscillation allowance See figure 12	OA	XT2S = 0, f_{XT2} = 1 MHz, $C_{L,,eff}$ = 15 pF			2700 TYP		
		XT2S = 1, f_{XT2} = 4 MHz, $C_{L,,eff}$ = 15 pF			800 TYP		
		XT2S = 2, $f_{XT1,\ HF}$ = 16 MHz, $C_{L,,eff}$ = 15 pF			300 TYP		
Integrated effective load capacitance, HF mode 25/	$C_{L,eff}$	30/			1 TYP		pF
	Duty cycle	Measured at P1.4/SMCLK, f_{XT2} = 10 MHz	2.2 V/3 V		40	60	%
		Measured at P1.4/SMCLK, f_{XT2} = 16 MHz			40	60	
Oscillator fault frequency, HF mode 26/	f_{Fault}	XT2S = 3 27/	2.2 V/3 V		30	300	kHz
Timer_A							
Timer_A clock frequency	f_{TA}	Internal: SMCLK, ACLK, External: TACLK, INCLK, Duty cycle = 50% ±10%	2.2 V	01		7.5	MHz
			3 V			16	
Timer_A, capture timing	$f_{TA,cap}$	TA0, TA1, TA2	2.2 V/3 V		20		ns
Timer_B							
Timer_B clock frequency	f_{TB}	Internal: SMCLK, ACLK, External: TBCLK, Duty cycle = 50% ±10%	2.2 V	01		7.5	MHz
			3 V			16	
Timer_B, capture timing	$f_{TB,cap}$	TB0, TB1, TB2	2.2 V/3 V		20		ns
USCI (UART mode)							
USCI input clock frequency	f_{USCI}	Internal: SMCLK, ACLK, External: TBCLK, Duty cycle = 50% ±10%		01		f_{SYSTEM}	MHz
BITCLK clock frequency (equals baud rate in MBaud)	f_{BITCLK}		2.2 V/3 V			1	
UART receive deglitch time 28/	t_ζ		2.2 V		50	600	ns
			3 V		50	600	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$ 2/ unless otherwise specified	V_{CC}	Device type	Limits		Unit
					Min	Max	
USCI (SPI Master mode) See figure 13 32/							
USCI input clock frequency		SMCLK, ACLK, Duty cycle = 50% ±10%		01		f_{SYSTEM}	MHz
SOMI input data setup time	$t_{SU,MI}$		2.2 V		110		ns
			3 V		75		
SOMI input data hold time	$t_{HD,MI}$		2.2 V		0		
			3 V		0		
SIMO output data valid	$t_{VALID,MO}$	UCLK edge to SIMO valid, C_L = 20 pF	2.2 V			30	
			3 V			20	
USCI (SPI Slave mode) See figure 14 32/							
STE lead time, STE low to clock	$t_{STE,LEAD}$		2.2 V/3 V	01	50 TYP		ns
STE lag time, last clock to STE high	$t_{STE,LAG}$		2.2 V/3 V		10		
STE access time, STE low to SOMI data out	$t_{STE,ACC}$		2.2 V/3 V		50 TYP		
STE disable time, STE high to SOMI high impedance	$t_{STE,DIS}$		2.2 V/3 V		50 TYP		
SIMO input data setup time	$t_{SU,SI}$		2.2 V		20		
			3 V		15		
SIMO input data hold time	$t_{HD,SI}$		2.2 V		10		
			3 V		10		
SOMI output data valid	$t_{VALID,SO}$	UCLK edge to SOMI valid, C_L = 20 pF	2.2 V			110	
			3 V			75	
USCI (I2C mode) See figure 15							
USCI clock frequency	f_{USCI}	Internal: SMCLK, ACLK, External: UCLK, Duty cycle = 50% ±10%		01	f_{SYSTEM} TYP		MHz
SCL clock frequency	f_{SCL}		2.2 V/3 V		0	400	µs
Hold time (repeated) START	$t_{HD,STA}$	$f_{SCL} \le 100$ kHz	2.2 V/3 V		4.0		
		$f_{SCL} > 100$ kHz			0.6		
Setup time for a repeated START	$t_{SU,STA}$	$f_{SCL} \le 100$ kHz	2.2 V/3 V		4.7		
		$f_{SCL} > 100$ kHz			0.6		
Data hold time	$t_{HD,DAT}$		2.2 V/3 V		0		ns
Data setup time	$t_{SU,DAT}$		2.2 V/3 V		250		
Setup time for STOP	$t_{SU,STO}$		2.2 V/3 V		4.0		µs
Pulse width of spikes suppressed by input filter	t_{SP}		2.2 V		50	600	ns
			3 V		50	600	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$ 2/ unless otherwise specified	V_{CC}	Device type	Limits		Unit
					Min	Max	
Comparator_A+ 33/							
	$I_{(DD)}$	CAON = 1, CARSEL = 0, CAREF = 0	2.2 V	01		40	µA
			3 V			60	
	$I_{(Refladder/Refdiode)}$	CAON = 1, CARSEL = 0, CAREF = 1/2/3, no load at p2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V			50	µA
			3 V			71	
Common mode input voltage	$V_{(IC)}$	CAON = 1	2.2 V/3 V			V_{CC} - 1	V
Voltage @ $0.25V_{CC}$ node / V_{CC}	$V_{(Ref025)}$	PCA0 = 1, CARSEL = 1, CAREF = 1, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V/3 V		0.23	0.25	
Voltage @ $0.5V_{CC}$ node / V_{CC}	$V_{(Ref050)}$	PCA0 = 1, CARSEL = 1, CAREF = 2, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V/3 V		0.47	0.50	
See figure 17	$V_{(RefVT)}$	PCA0 = 1, CARSEL = 1, CAREF = 3, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2, $T_A = 85°C$	2.2 V		390	540	mV
			3 V		400	550	
Offset voltage	$V_{(offset)}$	34/	2.2 V/3 V		-30	30	
Input hysteresis	V_{hys}	CAON = 1	2.2 V/3 V		0	1.4	
Low to high and high to low 35/	$t_{(response)}$	$T_A = 85°C$, Overdriver 10 mV, Without filter: CAF = 0	2.2 V		80	300	ns
			3 V		70	270	
		$T_A = 85°C$, Overdriver 10 mV, With filter: CAF = 1	2.2 V		1.4	2.8	
			3 V		0.9	2.2	
12 bit ADC, power supply and input range conditions							
Analog supply voltage	AV_{CC}	AV_{CC} and DV_{CC} are connected together AV_{SS} and DV_{SS} are connected together $V_{(AVSS)} = V_{(DVSS)} = 0$ V		01	2.2	3.6	V
Analog input voltage range 42/	$V_{(P6.x/Ax)}$	All P6.0/A0 to P6.7/A7 terminals. Analog inputs selected in ADC12MCTLx register, P6Sel.x =1, $0 \le x \le 7$, $V_{(AVSS)} \le V_{P6.x/Ax} \le V_{(AVCC)}$			0	V_{AVCC}	
Operating supply current into AV_{CC} terminal 43/	I_{ADC12}	$f_{ADC12CLK}$ = 5 MHz, ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV - 0	2.2 V			0.8	mA
			3 V			1	
Operating supply current into AV_{CC} terminal 43/	I_{REF+}	$f_{ADC12CLK}$ = 5 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 1	3 V			0.7	
		$f_{ADC12CLK}$ = 5 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 0	2.2 V			0.7	
			3 V			0.7	
Input capacitance	C_I 36/	Only one terminal can be selected at one time, P6.x/Ax	2.2 V			40	pF
Input MUX ON resistance	R_I 36/	$0 V \le V_{Ax} \le V_{AVCC}$	3 V			2000	Ω

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	T_A	V_{CC}	Device type	Limits		Unit
						Min	Max	
12 bit ADC, built in reference								
Positive built in reference voltage output	V_{REF+}	REF2_5V = 1 (2.5 V), I_{VREF} +max ≤ I_{VREF+} ≤ I_{VREF+}min	-55°C to 105°C	3 V	01	2.4	2.6	V
			125°C	3 V		2.37	2.64	
		REF2_5V = 0 (1.5 V), I_{VREF} +max ≤ I_{VREF+} ≤ I_{VREF+}min	-55°C to 105°C	2.2 V/3 V		1.44	1.56	
			125°C	2.2 V/3 V		1.42	1.57	
AVCC minimum voltage, Positive built in reference active	$AV_{CC(min)}$	REF2_5V = 0, I_{VREF} +max ≤ I_{VREF+} ≤ I_{VREF+}min				2.2		
		REF2_5V = 1, -0.5 mA ≤ I_{VREF+} ≤ I_{VREF+}min				2.8		
		REF2_5V = 1 (2.5 V), -1 mA ≤ I_{VREF+} ≤ I_{VREF+}min				2.9		
Load current out of V_{REF+} terminal	I_{VREF+}			2.2 V		0.01	-0.5	mA
				3 V		0.01	-1	
Load current regulation V_{REF+} terminal	$IL_{(VREF)+}$ 45/	I_{VREF+} = 500 µA ±100 µA Analog input voltage -0.75 V; REF2_5V = 0		2.2 V			±2	LSB
				3 V			±2	
		I_{VREF+} = 500 µA ±100 µA Analog input voltage ~1.25 V; REF2_5V = 1		3 V			±2	
Load current regulation V_{REF+} terminal	$IDL_{(VREF)+}$ 36/	I_{VREF+} = 500 µA → 900 µA CVREF+ = 5 µF; ax ~0.5 x V_{REF+} Error of conversion result ≤ 1 LSB		3 V			20	ns
Capacitance at pin V_{REF+} 46/	C_{VREF+}	REFON = 1, 0 mA ≤ I_{VREF+} ≤ I_{VREF+}mAX		2.2 V/3 V		5		µF
Temperature coefficient of built in reference	T_{REF+} 45/	I_{VREF+} is a constant in the range of 0 mA ≤ I_{VREF+} ≤ 1 mA		2.2 V/3 V			±100	ppm/°C
Settle time of internal reference voltage See figure 19 47/	t_{REFON} 45/	I_{VREF+} = 0.5 mA, C_{VREF+} = 10 µF, V_{REF+} = 1.5 V, V_{ACC} = 2.2 V					17	ms

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$ 2/ unless otherwise specified	V_{CC}	Device type	Limits		Unit
					Min	Max	
12 bit ADC, timing parameters							
	$f_{ADC12CLK}$	For specified performance of ADC12 linearity parameters	2.2 V/3 V	01	0.45	6.3	MHz
Internal ADC12 oscillator	$f_{ADC12osc}$	ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12osc}$	2.2 V/3 V		3.7	6.3	MHz
Conversion time	$t_{CONVERT}$	$C_{VREF+} \ge 5$ µF, Internal oscillator, $f_{ADC12osc}$ = 3.7 MHz to 6.3 MHz	2.2 V/3 V		2.06	3.51	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK, or SMCLK: ADC12SSEL ≠ 0			13 x ADC12DIV x $1/f_{ADC12CLK}$		
Turn on setting time of the ADC	$t_{ADC12ON}$ 48/	49/				100	ns
Sampling time	t_{Sample}	R_S = 400 Ω, R_I = 1000 Ω, C_I = 30 pF $\zeta = (R_S + R_I) \times C_I$ 50/	3 V		1220		ns
			2.2 V		1400		
12-bit ADC, linearity parameters							
Integral linearity error	E_I	1.4 V ≤ (V_{eREF+} - V_{REF-}/V_{eREF-}) min ≤ 1.6 V	2.2 V/3 V	01		±1.7	LSB
		1.6 V < (V_{eREF+} - V_{REF-}/V_{eREF-}) min ≤ [V_{AVCC}]				±1.7	
Differential linearity error	E_D	(V_{eREF+} - V_{REF-}/V_{eREF-})$_{min}$ ≤ (V_{eREF+} - V_{REF-}/V_{eREF-}), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)				±1	
Offset error	E_O	(V_{eREF+} - V_{REF-}/V_{eREF-})$_{min}$ ≤ (V_{eREF+} - V_{REF-}/V_{eREF-}), Internal impedance of source R_S < 100 Ω, C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)				±4	
Gain error	E_G	(V_{eREF+} - V_{REF-}/V_{eREF-})$_{min}$ ≤ (V_{eREF+} - V_{REF-}/V_{eREF-}), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)				±2	
Total unadjusted error	E_T	(V_{eREF+} - V_{REF-}/V_{eREF-})$_{min}$ ≤ (V_{eREF+} - V_{REF-}/V_{eREF-}), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)				±5	
12 bit ADC, temperature sensor and built-in V_{MID}							
Operating supply current into AV_{CC} terminal 52/	I_{SENSOR}	REFON = 0, INCH = 0Ah, ADC12ON = 1, T_A = 25°C	2.2 V	01		120	µA
			3 V			160	
53/	V_{SENSOR} 51/	ADC12ON = 1, INCH = 0Ah, T_A = 0°C	2.2 V		986 TYP		mV
			3 V		986 TYP		
	TC_{SENSOR}	ADC12ON = 1, INCH = 0Ah	2.2 V			3.55 ±3%	mV/°C
			3 V			3.55 ±3%	
Sample time required if channel 10 is selected 54/	t_{SENSOR} (sample)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V		30		µs
			3 V		30		
Current into divider at channel 11 55/	I_{VMID}	ADC12ON = 1, INCH = 0Bh	2.2 V			NA	µA
			3 V			NA	
AV_{CC} divider at channel 11	V_{MID}	ADC12ON = 1, INCH = 0Bh, V_{MID} is ~0.5 x V_{AVCC}	2.2 V			1.1 ±0.04	V
			3 V			1.1 ±0.04	
Sample time required if channel 11 is selected 56/	t_{VMID} (sample)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V		1400		ns
			3 V		1220		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

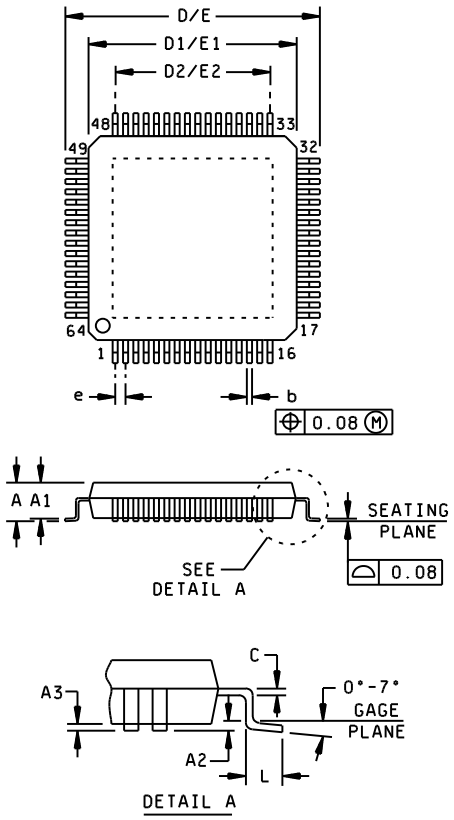
Test	Symbol	Conditions 2/ unless otherwise specified	V_{CC}	Device type	Limits		Unit
					Min	Max	
flash memory							
Program and erase supply voltage	$V_{CC(PGM/ERASE)}$			01	2.2	3.6	V
Flash timing generator frequency	f_{FTG}				257	476	kHz
Supply current from DV_{CC} during program	I_{PGM}		2.7 V/3.6 V			5	mA
Supply current from DV_{CC} during erase	I_{ERASE}		2.7 V/3.6 V			7	mA
Cumulative program time	t_{CPT}	57/	2.7 V/3.6 V			4	ms
Cumulative mass erase time	$t_{CMErase}$	58/	2.7 V/3.6 V		20		ms
Program/Erase endurance					10^4		cycles
Data retention duration	$t_{Retention}$	T_J = 25°C			100		years
Word or byte program time	t_{Word}	59/			35 TYP		t_{FTG}
Block program time for 1st byte or word	$t_{Block, 0}$				30 TYP		
Block program time for each additional byte or word	$t_{Block, 1-63}$				21 TYP		
Block program end-sequence wait time	$t_{Block, End}$				6 TYP		
Mass erase time 60/	$t_{Mass Erase}$				10593 TYP		
Segment erase time	$t_{Seg Erase}$				4819 TYP		
RAM							
61/	VRAMh	CPU halted		01	1.6		V
JTAG interface							
TCK input frequency	f_{TCK}	62/	2.2 V	01	0	5	MHz
			3 V		0	10	
Internal pullup resistance on TMS, TCK, TDI/TCLK	$R_{Internal}$	63/	2.2 V/3 V		25	90	Ω
JTAG fuse 64/							
Supply voltage during fuse-blow condition	$V_{CC(FB)}$	T_A = 25°C		01	2.5		V
Voltage level on TDI/TCLK for fuse blow	V_{FB}				6	7	V
Supply current into TDI/TCLK during fuse blow	I_{FB}					100	mA
Time to blow fuse	t_{FB}					1	ms

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ Over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted).
3/ All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
4/ The current are characterized with a micro crystal. See manufacture data for more information.
5/ Current for brownout and WDT+ is included. The WDT+ is clocked by SMCLK.
6/ Current for brownout and WDT+ is included. The WDT+ is clocked by ACLK.

7/ Current for brownout included.
8/ XIN and XT2IN only bypass mode.
9/ The external signal sets the interrupt flag every time the minimum $t_{(int)}$ parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$.
10/ The leakage current is measured with VSS or VCC applied to the corresponding pin(s), unless otherwise noted.
11/ The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.
12/ The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to satisfy the maximum voltage drop specified.
13/ The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to satisfy the maximum voltage drop specified.
14/ A resistive divider with 2 times 0.5 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
15/ The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.
16/ The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8 V.
17/ During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$, The default DCO settings must not be changed until $V_{CC} \geq V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency.
18/ The recommended operating voltage range is limited to 3.6 V.
19/ t_{settle} is the setting time that the comparator output must have a stable level after VLD is switched VLD ≠ 0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be > 50 mV.
20/ The current consumption of the SVS module is not included in the I_{CC} current consumption data.
21/ The DCO clock wake up time is measured from the edge of an external wake up signal (e.g., port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
22/ Parameter applicable only if DCOCLK is used for MCLK.
23/ R_{OSC} = 100kΩ. Metal film resistor, type 0257. 0.6 watt with 1% tolerance and TK = ±50ppm/°C.
24/ To improve EMI on the LFXT1 oscillator the following guidelines should be observed:
   a. Keep the trace between the device and the crystal as short as possible.
   b. Design a good ground plane around the oscillator pin.
   c. Prevent crosstalk from other clock or data lines into oscillator pin XIN and XOUT.
   d. Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   e. Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   f. If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between oscillator pins.
   g. Do not rout the XOUT line to the JTAG header to support the serial programming adapter as shown in other data. This signal is no longer required for the serial programming adapter.
25/ Includes parasitic bond and package capacitance (approximately 2 pF per pin). Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification on the used crystal.
26/ Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
27/ Measured with logic level input frequency, but also applies to operation with crystals.
28/ Calculated using the box method:
   I Version: [MAX(-55 to 85°C) – MIN(-40 to 85°C)]/ MIN(-40 to 85°C)]/[85°C – (-40°C)]
   T version: [MAX(-40 to 105°C) – MIN(-40 to 105°C)]/ MIN(-40 to 105°C)]/[105°C – (-40°C)]
29/ Calculated using the box method:[Max(1.8…3.6V) – MIN(1.8…3.6 V)]/MIN(1.8…3.6 V)/(3.6 V – 1.8 V)
30/ Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
31/ Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that the pulses correctly recognized, their width should exceed the maximum specification of the deglitch time.
32/ $fUCxCLK = \frac{1}{2t_{LO/HI}}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(Master)} + t_{VALID,SO(USCI)})$.
For the master's parameter $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ refer to manufacturer data sheet.

33/ The leakage current for the Comparator_A terminals is identical to $I_{lkg(Px.x)}$ specification.
34/ The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.
35/ The response time is measured at P2.2/CAOUT/TA0/CA4 with an input voltage step, with Comparator_A+ already enabled (CAON = 1). If CAON is set at the same time, a setting time of up to 300 ns is added to the response time.
36/ Not production tested, limits verified by design.
37/ The leakage current is defined in the leakage current table with Px.x/Ax parameter.
38/ The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion result.
39/ The internal reference supply current is not included in current consumption parameter I_{ADC12}.
40/ The internal reference current is supplied via terminal AV_{CC}. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables the built in reference to settle before starting an A/D conversion.
41/ The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog source impedance to allow the change to settle for 12 bit accuracy.
42/ The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
43/ The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
44/ The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
45/ Not production tested, limits characterized.
46/ The internal buffer operational amplifier and the accuracy specifications require an external capacitor. All INL and DNL tests uses two capacitors between pins V_{REF+} and AV_{SS} and V_{REF-}/V_{eREF-} and AV_{SS}:10 µF tantalum and 100 nF ceramic.
47/ The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSDB. The setting time depends on the external capacitive load.
48/ Limits verified by design.
49/ The condition is that the error in a conversion started after $t_{ADC12ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
50/ Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB:
$t_{Sample} = \ln(2^{n+1}) \times (R_s + R_i) \times C_i + 800$ ns where n = ADC resolution = 12, R_S = external source resistance.
51/ Limits characterized.
52/ The sensor current I_{SENSOR} is consumed if (ADC12ON = 1 and REFON = 1) or (ADC12ON =1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is included in I_{REF+}.
53/ The temperature sensor offset can be as much as ±20°C. A single point calibration is recommended in order to minimize the offset error of the built-in temperature sensor.
54/ The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor on time $t_{SENSOR(on)}$.
55/ No additional current is needed. The V_{MID} is used during sample.
56/ The on time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.
57/ The cumulative program time must not be exceeded when writing to a 64 byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
58/ The mass erase duration generated by the flash timing generator is at least 11.1 ms (= 5297 x $1/f_{FTG}$, max = 5297 x 1/476kHz). To achieve the required cumulative mass erase time the Flash Controller's mass erase can be repeated until this time is met. (A worst case minimum of 19 cycles are required).
59/ These values are hardwired into the Flash Controller's state machine ($t_{FTG} = 1/f_{FTG}$).
60/ To erase the complete code area the mass erase has to be performed once with a dummy address in the range of the lower 64kB. Flash addresses and once with the dummy address in the upper 64kB Flash addresses.
61/ This parameter defines the minimum supply voltage when the data in program memory RAM remains unchanged. No program execution should take place during this supply voltage condition.
62/ f_{TCK} may be restricted to meet the timing requirements of the module selected.
63/ TMS, TDI/TCLK, and TCK pullup resistor are implemented in all versions.
64/ Once the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.

Case X



Dimension					
Symbol	Min	Max	Symbol	Min	Max
A		1.60	D/E	11.80	12.20
A1	1.35	1.45	D1/E1	9.80	10.20
A2	0.25 TYP		D2/E2	7.50 TYP	
A3	0.05		e	0.50 BSC	
b	0.17	0.27	L	0.45	0.75
C	0.13 NOM				

NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Falls within JEDEC MS-026.
4. May also be thermally enhanced plastic with leads connected to the die pads.

FIGURE 1. Case outline.

Case outline X

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DV_{CC}	33	P3.5/UCA0RXD/UCA0SOMI
2	P6.3/A3	34	P3.6/UCA1TXD/UCA1SIMO
3	P6.4/A4	35	P3.7/UCA1RXD/UCA1SOMI
4	P6.5/A5	36	P4.0/TB0
5	P6.6/A6	37	P4.1/TB1
6	P6.7/A7/SVSIN	38	P4.2/TB2
7	V_{REF-}	39	P4.3/TB3
8	XIN	40	P4.4/TB4
9	XOUT	41	P4.5/TB5
10	Ve_{REF+}	42	P4.6/TB6
11	V_{REF-}/Ve_{REF-}	43	P4.7/TBCLK
12	P1.0/TACLK/CAOUT	44	P5.0/UCB1STE/UCA1CLK
13	P1.1/TA0	45	P5.1/UCB1SIMO/UCB1SDA
14	P1.2/TA1	46	P5.2/UCB1SOMI/UCB1SCL
15	P1.3/TA2	47	P5.3/UCB1CLK/UCA1STE
16	P1.4/SMCLK	48	P5.4/MCLK
17	P1.5/TA0	49	P5.5/SMCLK
18	P1.6/TA1	50	P5.6/ACLK
19	P1.7/TA2	51	P5.7/TBOUTH/SVSOUT
20	P2.0/ACLK/CA2	52	XT2OUT
21	P2.1/TAINCLK/CA3	53	XT2IN
22	P2.2/CAOUT/TA0/CA4	54	TDO/TDI
23	P2.3/CA0/TA1	55	TDI/TCLK
24	P2.4/CA1/TA2	56	TMS
25	$P2.5/R_{OSC}$/CA5	57	TCK
26	P2.6/ADC12CLK/CA6	58	$\overline{RST}$/NMI
27	P2.7/TA0/CA7	59	P6.0/A0
28	P3.0/UCB0STE/UCA0CLK	60	P6.1/A1
29	P3.1/UCB0SIMO/UCB0SDA	61	P6.2/A2
30	P3.2/UCB0SOMI/UCB0SCL	62	AV_{SS}
31	P3.3/UCB0CLK/UCA0STE	63	DV_{SS}
32	P3.4/UCA0TXD/UCA0SIMO	64	AV_{CC}

FIGURE 2. Terminal connections.

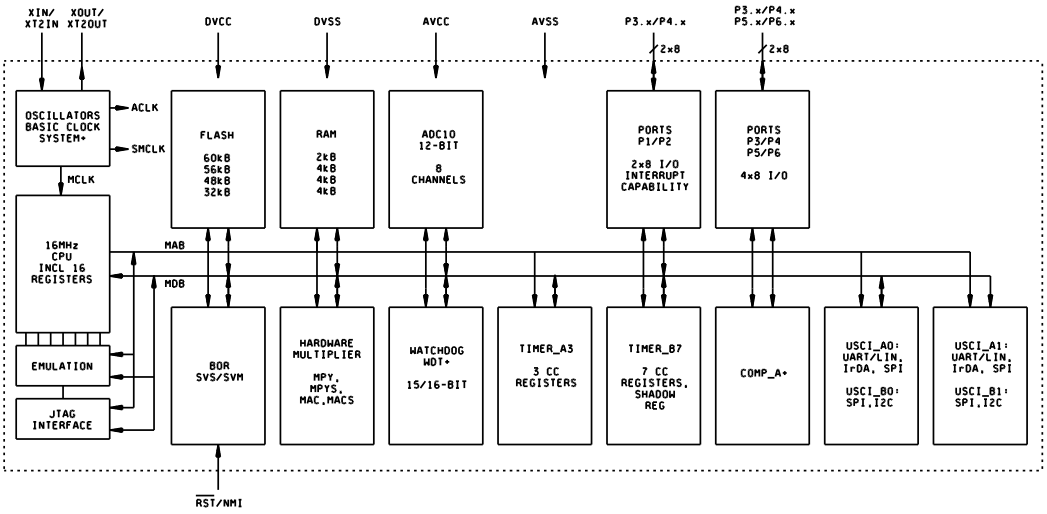
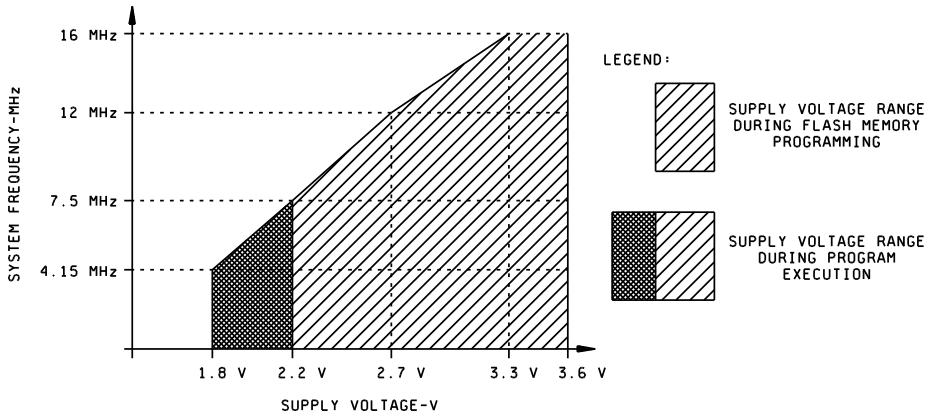
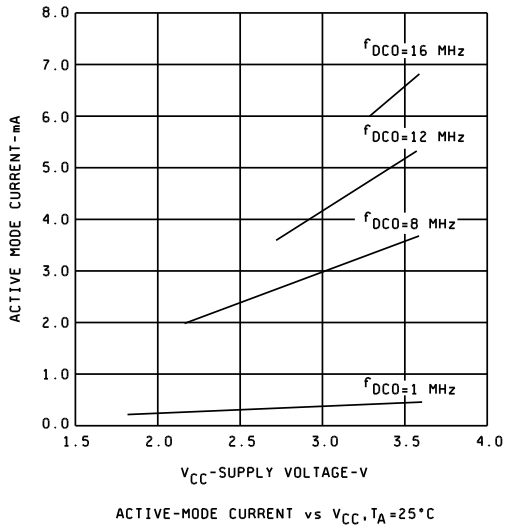


FIGURE 3. Functional block diagram.

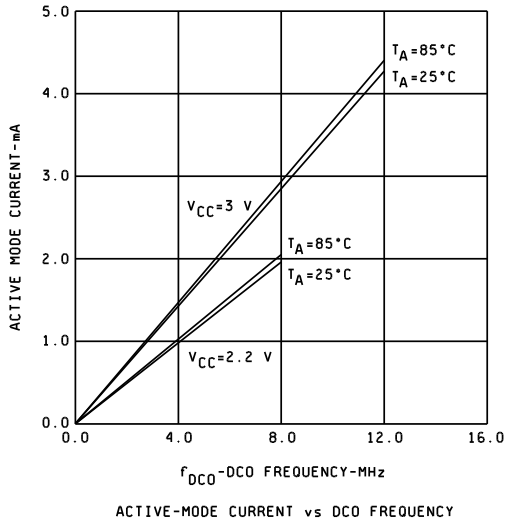


NOTE:
1. Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

FIGURE 4. Operating area.



ACTIVE-MODE CURRENT vs V_{CC}, T_A=25°C



ACTIVE-MODE CURRENT vs DCO FREQUENCY

FIGURE 5. Active mode supply current.

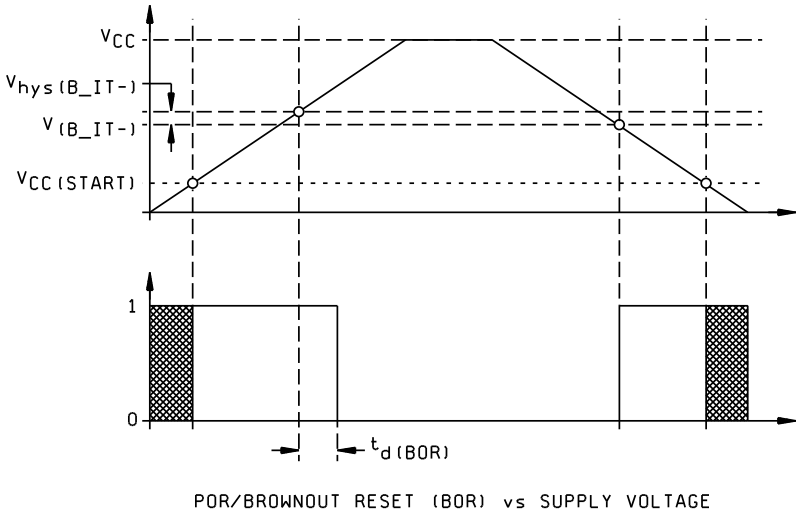
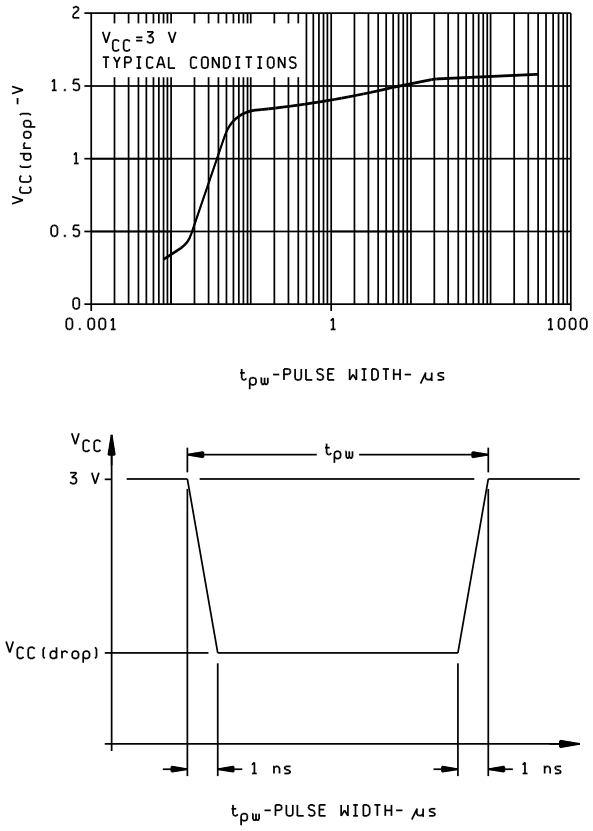
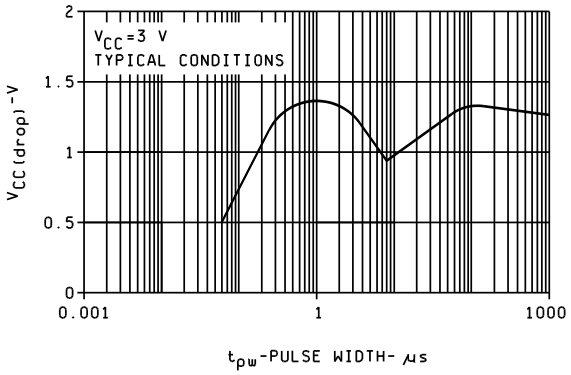


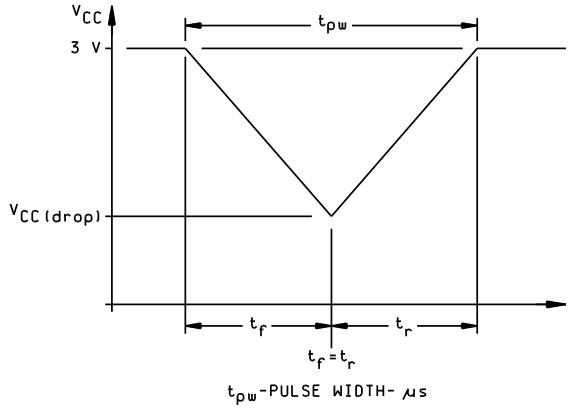
FIGURE 6. POR/Brownout reset.



$V_{CC(drop)}$ LEVEL WITH A SQUARE VOLTAGE DROP TO GENERATE A POR/BROWNOUT SIGNAL

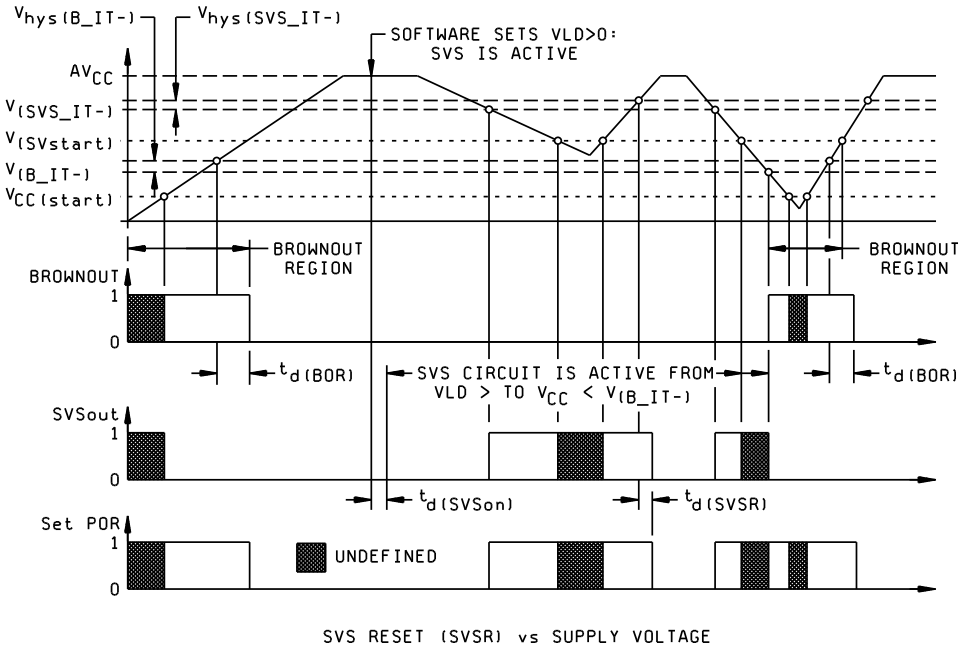
FIGURE 7. POR/Brownout reset.





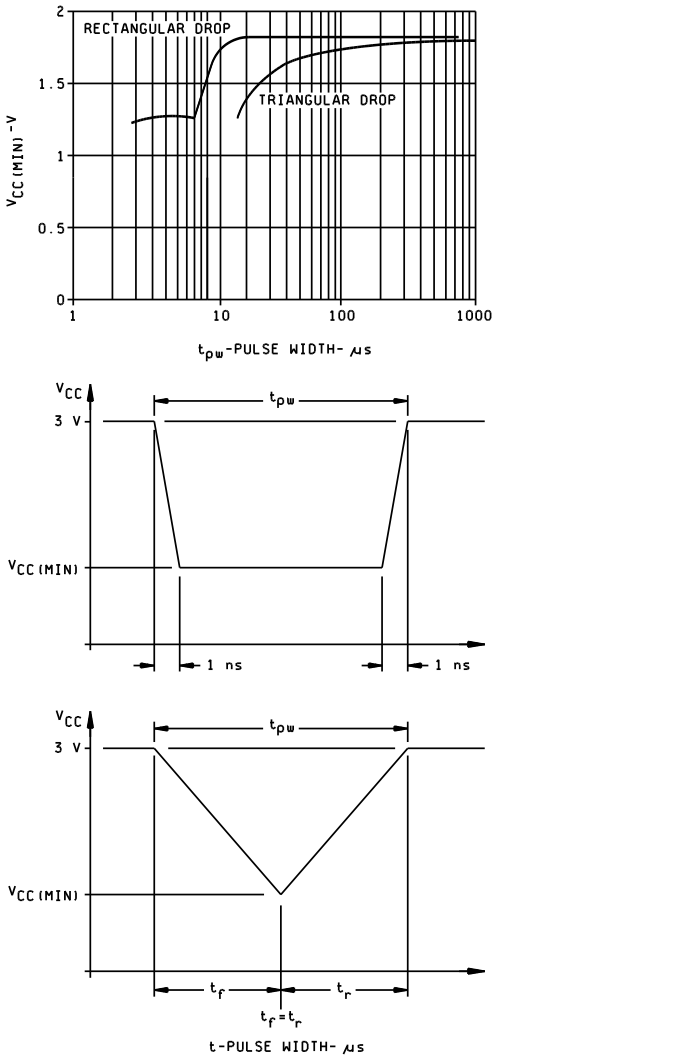
$V_{CC(drop)}$ LEVEL WITH A TRIANGLE VOLTAGE DROP TO GENERATE A POR/BROWNOUT SIGNAL

FIGURE 8. POR/Brownout reset.



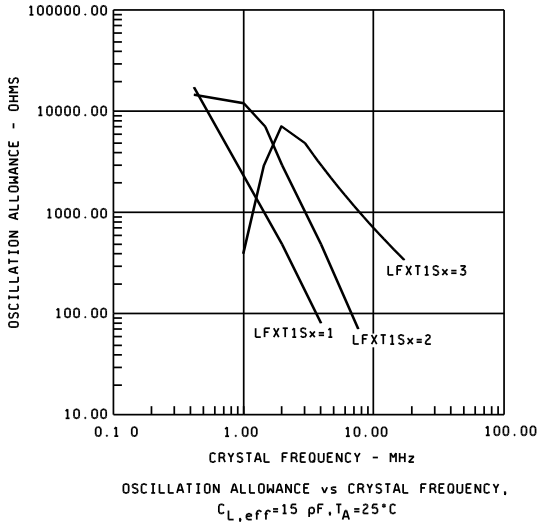
SVS RESET (SVSR) vs SUPPLY VOLTAGE

FIGURE 9. Test circuit and timing waveforms.



$V_{CC(MIN)}$: SQUARE VOLTAGE DROP AND TRIANGLE VOLTAGE DROP TO GENERATE AN SVS SIGNAL (VLD=1)

FIGURE 10. Test circuit and timing waveforms.



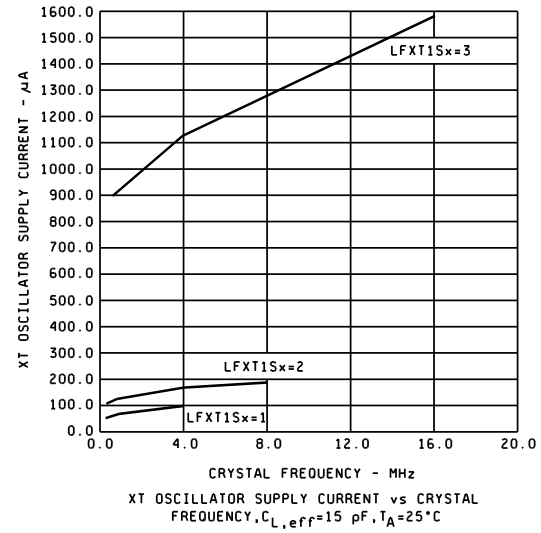
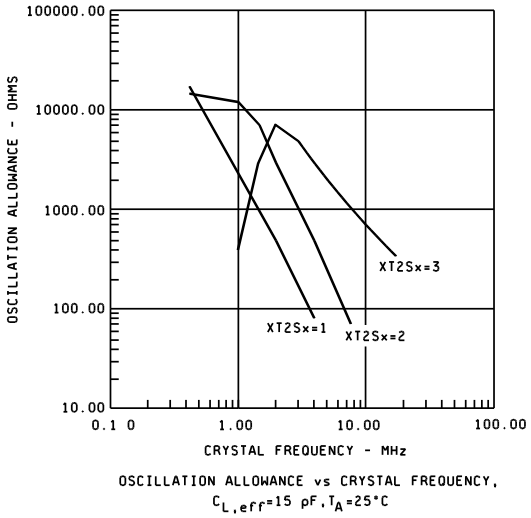


FIGURE 11. Test circuit and timing waveforms.



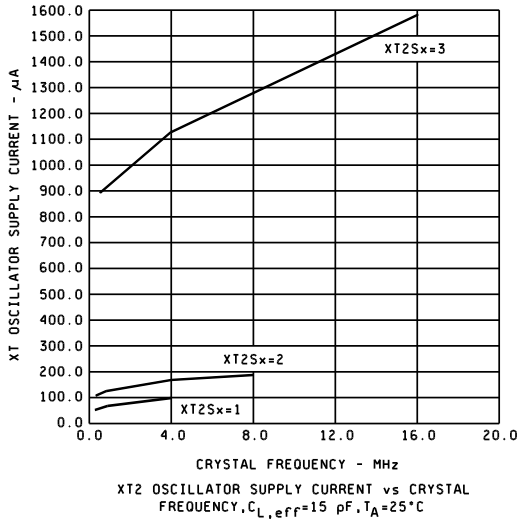
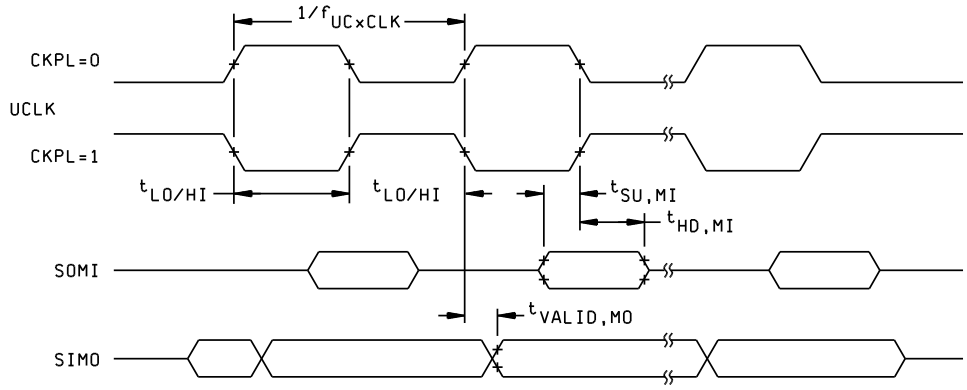
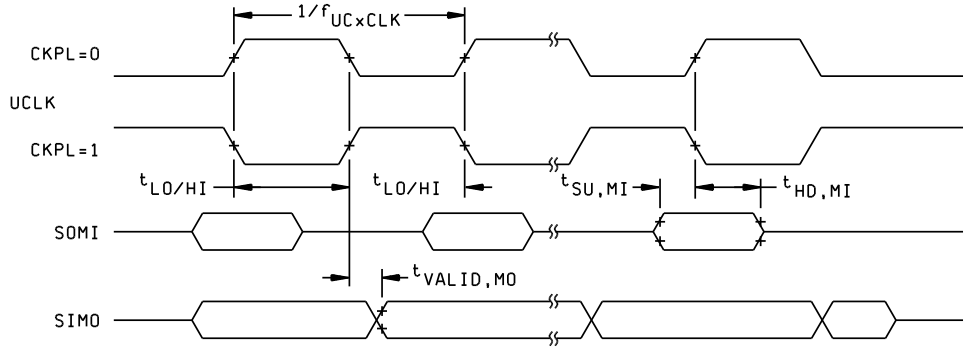


FIGURE 12. Test circuit and timing waveforms.



SPI SLAVE MODE, CKPH = 0



SPI SLAVE MODE, CKPH = 1

FIGURE 13. Test circuit and timing waveforms.

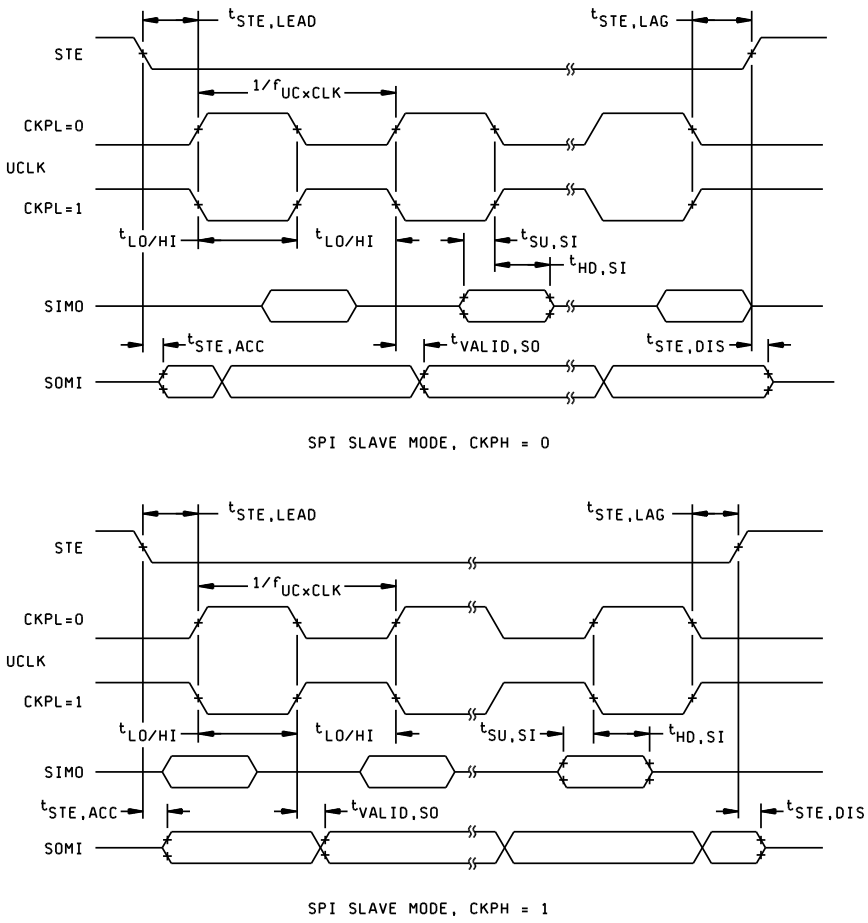
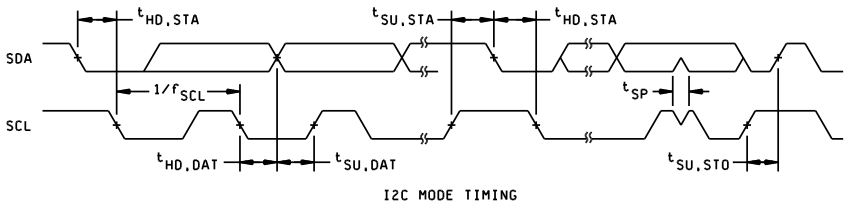
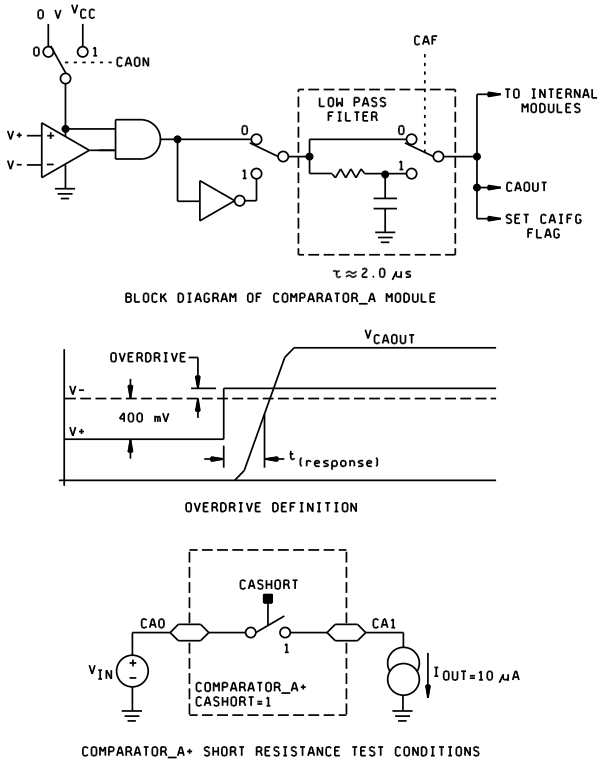


FIGURE 14. Test circuit and timing waveforms.



I2C MODE TIMING

FIGURE 15. Test circuit and timing waveforms.

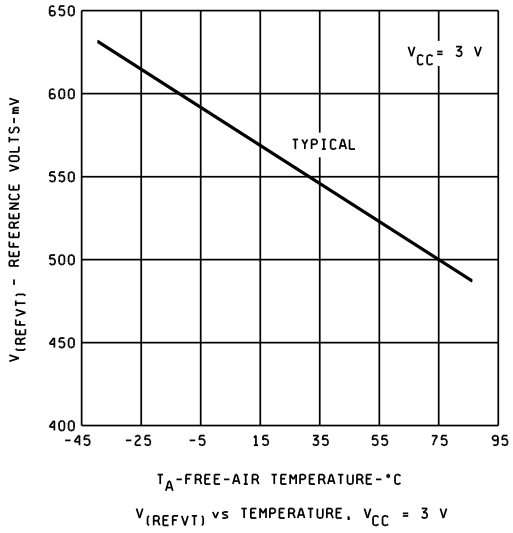


BLOCK DIAGRAM OF COMPARATOR_A MODULE

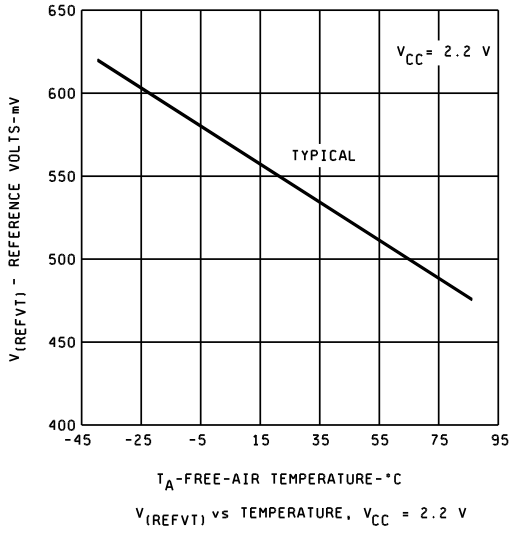
OVERDRIVE DEFINITION

COMPARATOR_A+ SHORT RESISTANCE TEST CONDITIONS

FIGURE 16. Test circuit and timing waveforms.



$V_{(REFVT)}$ vs TEMPERATURE, V_{CC} = 3 V



$V_{(REFVT)}$ vs TEMPERATURE, V_{CC} = 2.2 V

FIGURE 17. Test circuit and timing waveforms.

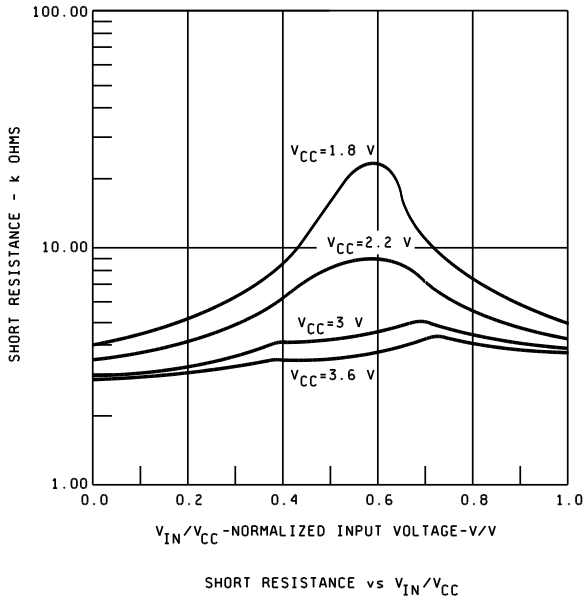


FIGURE 18. Test circuit and timing waveforms.

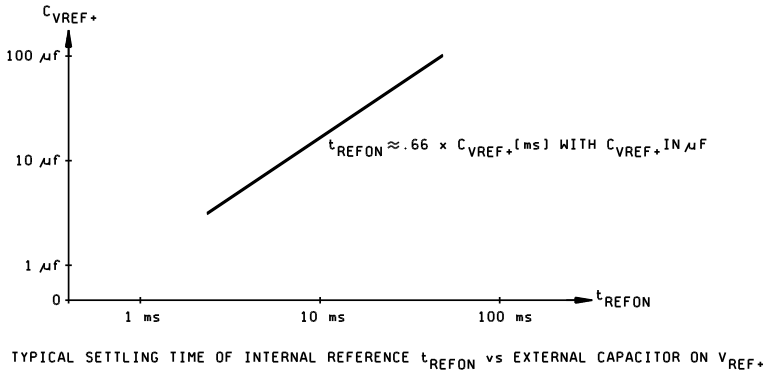


FIGURE 19. Test circuit and timing waveforms.

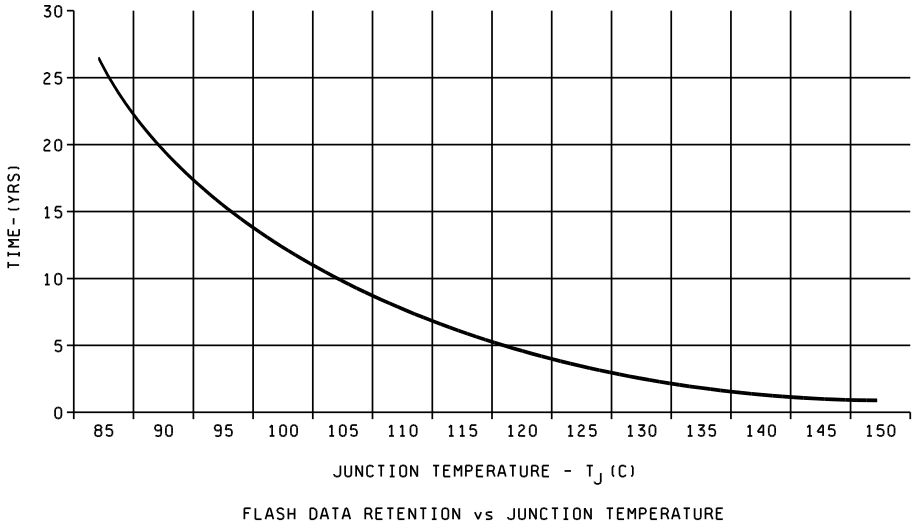


FIGURE 20. Test circuit and timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/09601-01XE	01295	MSP430F249MPMEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243