REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add case outline Y. - PHN	10-02-22	Thomas M. Hess
B	Change values for low power mode 3 current $I_{LPM3, VLO}$ and Input leakage current I_{lkg} , in Table I. - PHN	11-06-14	David J. Corbett
C	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	18-01-16	Thomas M. Hess
D	Update boilerplate paragraphs to current VID description requirements. - PHN	23-11-20	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
PAGE																						
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	
PAGE	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	
REV STATUS OF PAGES	**REV**					D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
	PAGE					1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

PMIC N/A

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Original date of drawing
YY MM DD
09-03-10

CHECKED BY
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Thomas M. Hess

TITLE
MICROCIRCUIT, DIGITAL, MIXED SIGNAL MICROCONTROLLER, MONOLITHIC SILICON

SIZE	**CODE IDENT. NO.**	**DWG NO.**
A	**16236**	**V62/08631**
REV **D**		**PAGE** 1 **OF** 38

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance mixed signal microcontroller microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/08631	-	01	X	A
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	MSP430F2274-EP	Mixed signal microcontroller

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	40	JEDEC MO-220	Plastic quad flatpack
Y	38	JEDEC MO-153	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Voltage applied at V_{CC} to V_{SS} ..... -0.3 V to 4.1 V
Voltage applied to any pin ..... -0.3 V to V_{CC} + 0.3 V 2/
Diode current at any device terminal ..... ±2 mA
Storage temperature range, T_{STG} (unprogrammed device) ..... -55°C to 150°C 3/
Storage temperature range, T_{STG} (programmed device) ..... -55°C to 125°C 3/

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ All voltages referenced to V_{SS}. The JTAG fuse blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the test pin when blowing the JTAG fuse.
3/ Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

1.4 Recommended operating conditions. 4/ 5/ 6/

Supply voltage during program execution (V_{CC}) ..... 1.8 V to 3.6 V
Supply voltage during program/erase flash memory (V_{CC}) ..... 2.2 V to 3.6 V
Supply voltage (V_{SS}) ..... 0 V
Processor frequency f_{SYSTEM} (Maximum MCLK frequency): 4/ 5/ 7/
V_{CC} = 1.8 V, Duty Cycle 50% ±10% ..... 4.15 MHz
V_{CC} = 2.7 V, Duty Cycle 50% ±10% ..... 12 MHz
V_{CC} ≥ 3.3 V, Duty Cycle 50% ±10% ..... 16 MHz
Operating free air temperature range, T_A ..... -55°C to 125°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JEDEC J-STD-020	–	Joint IPC/JEDEC standard for moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices.

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

4/ The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
5/ Modules might have a different maximum input clock specification. Refer to the data sheet from manufacturer.
6/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
7/ See figure 4.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Operating area. The operating area shall be as shown in figure 4.

3.5.5 Active mode supply current. The active mode supply current shall be as shown in figure 5.

3.5.6 POR/Brownout reset. The POR/Brownout reset shall be as shown in figure 6-8.

3.5.7 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as shown in figure 9-15.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	T_A	V_{CC}	Limits			Unit
					Min	Typ	Max	
Active mode supply current (into DV_{CC} + AV_{CC}) Excluding External current 3/ 4/ See figure 5.								
Active mode (AM) current (1 MHz)	$I_{AM, 1MHz}$	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 32,768 Hz, Program executes in flash, BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1 MHz CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	-55°C to 125°C	2.2 V		270	390	µA
				3 V		390	550	
Active mode (AM) current (1 MHz)	$I_{AM, 1MHz}$	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 32,768 Hz, Program executes in RAM, BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1 MHz CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		240		µA
				3 V		340		
Active mode (AM) current (4 kHz)	$I_{AM, 4kHz}$	$f_{MCLK} = f_{SMCLK} = f_{ACLK}$ = 32,768 Hz/8 = 4096 Hz, f_{DCO} = 0 Hz, Program executes in flash, SELMx = 11, SELS = 1, DIVMx = DIVSx = DIVAx = 11, CPUOFF = 0, SCGO = 0, SCG1 = 0, OSCOFF = 0	-55°C to 85°C	2.2 V		5	9	µA
			125°C				18	
			-55°C to 85°C	3 V		6	10	
			125°C				20	
Active mode (AM) current (100 kHz)	$I_{AM, 100 kHz}$	$f_{MCLK} = f_{SMCLK} = f_{DCO(0,0)} \approx$ 100 kHz, f_{ACLK} = 0 Hz, Program executes in flash, RSELx = 0, DCOx = 0, CPUOFF = 0, SCGO = 0, SCG1 = 0, OSCOFF = 1	-55°C to 85°C	2.2 V		60	85	µA
			125°C				95	
			-55°C to 85°C	3 V		72	95	
			125°C				125	
Low power mode 0, (LPM0) current 5/	$I_{LPM0, 1 MHz}$	f_{MCLK} = 0 MHz, $f_{SMCLK} = f_{DCO}$ = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1 MHz, DCOCTL = CALDCO_1 MHz, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	-55°C to 125°C	2.2 V		75	90	µA
				3 V		90	120	
Low power mode 0, (LPM0) current 5/	$I_{LPM0, 100 kHz}$	f_{MCLK} = 0 MHz, $f_{SMCLK} = f_{DCO(0,0)} \approx$ 100 kHz, f_{ACLK} = 0 Hz, RSELx = 0, DCOx = 0, CPUOFF = 1, SCGO = 0, SCG1 = 0, OSCOFF = 1	-55°C to 125°C	2.2 V		37	60	µA
				3 V		41	75	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	T_A	V_{CC}	Limits			Unit
					Min	Typ	Max	
Active mode supply current (into DV_{CC} + AV_{CC}) Excluding External current - Continued 3/ 4/								
Low power mode 2 (LPM2) current 6/	I_{LPM2}	$f_{MCLK} = f_{SMCLK}$= 0 MHz, f_{DCO} = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1 MHz, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	-55°C to 85°C	2.2 V		22	29	µA
			125°C				40	
			-55°C to 85°C	3 V		25	32	
			125°C				45	
Low power mode 3 (LPM3) current 6/	$I_{LPM3, LFXT1}$	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0 MHz, f_{ACLK} = 32,768 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-55°C	2.2 V		0.7	1.4	µA
			25°C			0.7	1.4	
			85°C			2.8	4.5	
			125°C			6	18	
			-55°C	3 V		0.9	1.5	
			25°C			0.9	1.5	
			85°C			3.0	5.0	
			125°C			6.5	19	
Low power mode 3 current (LPM3) 6/	$I_{LPM3, VLO}$	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0 MHz, f_{ACLK} = from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-55°C	2.2 V		0.4	1.0	µA
			25°C			0.5	1.0	
			85°C			2.2	4.2	
			125°C			5.7	18	
			-55°C	3 V		0.5	1.2	
			25°C			0.6	1.2	
			85°C			2.5	4.5	
			125°C			6.0	19	
Low power mode 4 current (LPM4) 7/	I_{LPM4}	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0 MHz, f_{ACLK} = 0 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	-55°C	2.2 V/ 3 V		0.1	0.5	µA
			25°C			0.1	0.5	
			85°C			1.9	4.0	
			125°C			5.5	16	
Schmitt-trigger inputs (Ports P1, P2, P3, P4, and RST/NMI) 8/								
Positive going input threshold voltage	V_{IT+}		-55°C to 125°C	2.2 V	1.00		1.65	
				3 V	1.35		2.25	
Negative going input threshold voltage	V_{IT-}		-55°C to 125°C	2.2 V	0.55		1.20	
				3 V	0.75		1.65	
Input voltage hysteresis (V_{IT+} - V_{IT-})	Vhys		-55°C to 125°C	2.2 V	0.2		1.0	
				3 V	0.3		1.0	
Pullup/Pulldown resistor	R_{Pull}	For Pullup: $V_{IN} = V_{SS}$; For Pulldown: $V_{IN} = V_{CC}$	-55°C to 125°C		20	35	50	kΩ
Input capacitance	C_I	$V_{IN} = V_{SS}$ or V_{CC}				5		pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	T_A	V_{CC}	Limits			Unit
					Min	Typ	Max	
Input (Ports P1 and P2)								
External interrupt timing	$t_{(int)}$	Port P1, P2: P1.x to P2.x, External trigger pulse width to set interrupt flag 9/	-55°C to 125°C	2.2 V/ 3 V	20			ns
Leakage current (Ports P1, P2, P3 and P4)								
High impedance leakage current	$I_{lkg(Px.x)}$	10/ 11/	-55°C to 125°C	2.2 V/ 3 V			±100	nA
Output (Ports P1, P2, P3, and P4)								
High level output voltage	V_{OH}	$I_{OH(max)}$ = -1.5 mA 12/	-55°C to 125°C	2.2 V	V_{CC} – 0.25		V_{CC}	V
		$I_{OH(max)}$ = -6 mA 13/			V_{CC} – 0.6		V_{CC}	
		$I_{OH(max)}$ = -1.5 mA 12/		3 V	V_{CC} – 0.25		V_{CC}	
		$I_{OH(max)}$ = -6 mA 13/			V_{CC} – 0.6		V_{CC}	
Low level output voltage	V_{OL}	$I_{OL(max)}$ = 1.5 mA 12/		2.2 V	V_{SS}		V_{SS} + 0.25	V
		$I_{OL(max)}$ = 6 mA 13/			V_{SS}		V_{SS} + 0.6	
		$I_{OL(max)}$ = 1.5 mA 12/		3 V	V_{SS}		V_{SS} + 0.25	
		$I_{OL(max)}$ = 6 mA 13/			V_{SS}		V_{SS} + 0.6	
Output frequency (Ports P1, P2, P3, and P4)								
Port output frequency (with load) 14/ 15/	$f_{Px.y}$	P1.4/SMCLK, C_L = 20 pF, R_L = 1 kΩ against $V_{CC}/2$	-55°C to 125°C	2.2 V			10	MHz
				3 V			12	
Clock output frequency	f_{Port_CLK}	P2.0/ACLK, P1.4/SCMCLK, CL = 20 pF 15/		2.2 V			12	MHz
				3 V			16	
POR/Brownout Reset (BOR) 16/ 17/								
See figure 6	$V_{CC(start)}$	$dV_{CC}/dt \le 3$ V/s				0.7 x $V_{(B\_IT-)}$		V
See figure 6 through 8	$V_{(B\_IT-)}$	$dV_{CC}/dt \le 3$ V/s	-55°C to 125°C				1.71	V
See figure 6	$V_{hys(B\_IT-)}$	$dV_{CC}/dt \le 3$ V/s	-55°C to 125°C		70	130	210	mV
See figure 6	$t_{d(BOR)}$		-55°C to 125°C				2000	µs
Pulse length needed at $\overline{RST}$ /NMI pin to accepted reset internally	$t_{(reset)}$		-55°C to 125°C	2.2 V/ 3V	2			µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ -55°C ≤ T_A ≤ 125°C unless otherwise specified	V_{CC}	Limits			Unit
				Min	Typ	Max	
DCO frequency							
Supply voltage range	V_{CC}	RSELx < 14		1.8		3.6	V
		RSELx = 14		2.2		3.6	
		RSELx = 15		3.0		3.6	
DCO frequency (0, 0)	$f_{DCO(0,0)}$	RSELx = 0, DCOx = 0, MODx = 0	2.2 V/3 V	0.06		0.14	MHz
DCO frequency (0, 3)	$f_{DCO(0, 3)}$	RSELx = 0, DCOx = 3, MODx = 0		0.07		0.17	
DCO frequency (1,3)	$f_{DCO(1, 3)}$	RSELx = 1, DCOx = 3, MODx = 0		0.10		0.20	
DCO frequency (2, 3)	$f_{DCO(2, 3)}$	RSELx = 2, DCOx = 3, MODx = 0		0.14		0.28	
DCO frequency (3, 3)	$f_{DCO(3, 3)}$	RSELx = 3, DCOx = 3, MODx = 0		0.20		0.40	
DCO frequency (4, 3)	$f_{DCO(4, 3)}$	RSELx = 4, DCOx = 3, MODx = 0		0.28		0.54	
DCO frequency (5, 3)	$f_{DCO(5, 3)}$	RSELx = 5, DCOx = 3, MODx = 0		0.39		0.77	
DCO frequency (6, 3)	$f_{DCO(6, 3)}$	RSELx = 6, DCOx = 3, MODx = 0		0.54		1.06	
DCO frequency (7, 3)	$f_{DCO(7, 3)}$	RSELx = 7, DCOx = 3, MODx = 0		0.80		1.50	
DCO frequency (8, 3)	$f_{DCO(8, 3)}$	RSELx = 8, DCOx = 3, MODx = 0		1.10		2.10	
DCO frequency (9, 3)	$f_{DCO(9, 3)}$	RSELx = 9, DCOx = 3, MODx = 0		1.60		3.00	
DCO frequency (10, 3)	$f_{DCO(10, 3)}$	RSELx = 10, DCOx = 3, MODx = 0		2.50		4.30	
DCO frequency (11, 3)	$f_{DCO(11, 3)}$	RSELx = 11, DCOx = 3, MODx = 0		3.00		5.50	
DCO frequency (12, 3)	$f_{DCO(12, 3)}$	RSELx = 12, DCOx = 3, MODx = 0		4.30		7.30	
DCO frequency (13, 3)	$f_{DCO(13, 3)}$	RSELx = 13, DCOx = 3, MODx = 0		6.00		9.60	
DCO frequency (14, 3)	$f_{DCO(14, 3)}$	RSELx = 14, DCOx = 3, MODx = 0		8.60		13.9	
DCO frequency (15, 3)	$f_{DCO(15, 3)}$	RSELx = 15, DCOx = 3, MODx = 0	3 V	12.0		18.5	
DCO frequency (15, 7)	$f_{DCO(15, 7)}$	RSELx = 15, DCOx = 7, MODx = 0	3 V	16.0		26.0	
Frequency step between range RSEL and RSEL+1	S_{RSEL}	SRSEL = $f_{DCO(RSEL+1, DCO)}/f_{DCO(RSEL,DCO)}$	2.2 V/3 V			1.55	ratio
Frequency step between tap DCO and DCO+1	S_{DCO}	SDCO = $f_{DCO(RSEL,DCO+1)}/f_{DCO(RSEL,DCO)}$		1.05	1.08	1.12	ratio
Duty cycle		Measured at P1.4/SMCLK		40	50	60	%

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ $-55°C \le T_A \le 125°C$ unless otherwise specified	V_{CC}	Limits			Unit
				Min	Typ	Max	
Calibrated DCO frequencies (Tolerance at Calibration)							
Frequency tolerance at calibration		$T_A = 25°C$	3 V	-1	±0.2	1	%
1 MHz calibration value	$f_{CAL(1\ MHz)}$	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, Gating time: 5 ms, $T_A = 25°C$		0.990	1	1.010	MHz
8 MHz calibration value	$f_{CAL(8\ MHz)}$	BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz, Gating time: 5 ms, $T_A = 25°C$		7.920	8	8.080	
12 MHz calibration value	$f_{CAL(12\ MHz)}$	BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz, Gating time: 5 ms, $T_A = 25°C$		11.88	12	12.12	
16 MHz calibration value	$f_{CAL(16\ MHz)}$	BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz, Gating time: 2 ms, $T_A = 25°C$		15.84	16	16.16	
Calibrated DCO frequencies (Tolerance over temperature)							
1 MHz tolerance over temperature			3 V	-2.5	±0.5	2.5	%
8 MHz tolerance over temperature				-2.5	±1.0	2.5	
12 MHz tolerance over temperature				-2.5	±1.0	2.5	
16 MHz tolerance over temperature				-3.0	±2.0	3.0	
1 MHz calibration value	$f_{CAL(1\ MHz)}$	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, Gating time: 5 ms	2.2 V	0.970	1	1.030	MHz
			3V	0.975	1	1.025	
			3.6 V	0.970	1	1.030	
8 MHz calibration value	$f_{CAL(8\ MHz)}$	BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz, Gating time: 5 ms	2.2 V	7.760	8	8.400	
			3V	7.800	8	8.200	
			3.6 V	7.600	8	8.240	
12 MHz calibration value	$f_{CAL(12\ MHz)}$	BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz, Gating time: 5 ms	2.2 V	11.70	12	12.30	
			3V	11.70	12	12.30	
			3.6 V	11.70	12	12.30	
16 MHz calibration value	$f_{CAL(16\ MHz)}$	BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz, Gating time: 2 ms	3V	15.52	16	16.48	
			3.6 V	15.00	16	16.48	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ $-55°C \le T_A \le 125°C$ unless otherwise specified	V_{CC}	Limits			Unit
				Min	Typ	Max	
Calibrated DCO frequencies (Tolerance over supply voltage V_{CC})							
1 MHz tolerance over V_{CC}		$T_A = 25°C$	1.8 V to 3.6 V	-3	±2	3	%
8 MHz tolerance over V_{CC}			1.8 V to 3.6 V	-3	±2	3	
12 MHz tolerance over V_{CC}			2.2 V to 3.6 V	-3	±2	3	
16 MHz tolerance over V_{CC}			3 V to 3.6 V	-3	±2	3	
1 MHz calibration value	$f_{CAL(1\ MHz)}$	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, Gating time: 5 ms, $T_A = 25°C$	1.8 V to 3.6 V	0.970	1	1.030	MHz
8 MHz calibration value	$f_{CAL(8\ MHz)}$	BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz, Gating time: 5 ms, $T_A = 25°C$	1.8 V to 3.6 V	7.760	8	8.240	
12 MHz calibration value	$f_{CAL(12\ MHz)}$	BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz, Gating time: 5 ms, $T_A = 25°C$	2.2 V to 3.6 V	11.64	12	12.36	
16 MHz calibration value	$f_{CAL(16\ MHz)}$	BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz, Gating time: 2 ms, $T_A = 25°C$	3 V to 3.6 V	15.00	16	16.48	
Calibrated DCO frequencies (Overall tolerance)							
1 MHz tolerance over temperature			1.8 V to 3.6 V	-5	±2	+5	%
8 MHz tolerance over temperature			1.8 V to 3.6 V	-5	±2	+5	
12 MHz tolerance over temperature			2.2 V to 3.6 V	-5	±2	+5	
16 MHz tolerance over temperature			3 V to 3.6 V	-6	±3	+6	
1 MHz calibration value	$f_{CAL(1\ MHz)}$	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz, Gating time: 5 ms, $T_A = 25°C$	1.8 V to 3.6 V	0.950	1	1.050	MHz
8 MHz calibration value	$f_{CAL(8\ MHz)}$	BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz, Gating time: 5 ms	1.8 V to 3.6 V	7.6	8	8.4	
12 MHz calibration value	$f_{CAL(12\ MHz)}$	BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz, Gating time: 5 ms	2.2 V to 3.6 V	11.4	12	12.6	
16 MHz calibration value	$f_{CAL(16\ MHz)}$	BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz, Gating time: 2 ms	3 V to 3.6 V	15.00	16	17.00	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ -55°C ≤ T_A ≤ 125°C unless otherwise specified	V_{CC}	Limits			Unit
				Min	Typ	Max	
Wake up from lower power Modes (LPM3/4)							
DCO clock wake up time from LPM3/4 18/	$t_{DCO,LPM3/4}$	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz,	2.2 V/3 V			2	µs
		BCSCTL1 = CALBC1_8MHz, DCOCTL = CALDCO_8MHz,	2.2 V/3 V			1.5	
		BCSCTL1 = CALBC1_12MHz, DCOCTL = CALDCO_12MHz,	3 V			1	
		BCSCTL1 = CALBC1_16MHz, DCOCTL = CALDCO_16MHz,	3 V			1	
CPU wake up time from LPM3/4 19/	$t_{CPU,LPM3/4}$				$1/f_{MCLK}$ + $t_{Clock,LPM3/4}$		
DCO with external resistor R_{OSC}							
DCO output frequency with R_{OSC}	$f_{DCO,ROSC}$	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0, T_A = 25°C	2.2 V		1.8		MHz
			3 V		1.95		
Temperature drift	D_t	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V		±0.1		%/°C
Drift with V_{CC}	D_V	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V		10		%/V
Crystal Oscillator (LFXT1) Low frequency Modes -55°C ≤ T_A ≤ 105°C 21/							
LFXT1 oscillator crystal frequency, LF mode 0, 1	$f_{LFXT1,LF}$	XTS = 0, LFXT1Sx = 0 or 1	1.8 V to 3.6 V		32,768		Hz
LFXT1 oscillator logic level square wave input frequency, LF mode	$f_{LFXT1,LF,logic}$	XTS = 0, LFXT1Sx = 3		10,000	32,768	50,000	Hz
Oscillation allowance for LF crystal	OA_{LF}	XTS = 0, LFXT1Sx = 0; $f_{LFXT1,LF}$ = 32,768 Hz, $C_{L,eff}$ = 6 pF			500		kΩ
		XTS = 0, LFXT1Sx = 0; $f_{LFXT1,LF}$ = 32,768 Hz, $C_{L,eff}$ = 12 pF			200		
Integrated effective load capacitance, LF mode 22/	$C_{L,eff}$	XTS = 0, XCAPx = 0			1		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			11		
LF mode	Duty cycle	T_A = -55°C to 125°C XTS = 0, Measured at P1.4/ACLK, $f_{LFXT1,LF}$ = 32,768 Hz	2.2 V/3 V	30	50	70	%
Oscillator fault frequency threshold, LF mode 23/	$f_{Fault,LF}$	T_A = -55°C to 125°C XTS = 0, LFXT1Sx = 3 24/	2.2 V/3 V	10		10000	Hz

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ -55°C ≤ T_A ≤ 125°C unless otherwise specified	V_{CC}	Limits			Unit
				Min	Typ	Max	
Internal very low power, Low frequency oscillator (VLO)							
VLO frequency	f_{VLO}	T_A = -55°C to 85°C	2.2 V/3 V	4	12	20	kHz
		T_A = 125°C				22	
VLO frequency temperature drift	df_{VLO}/dT	25/			0.5		%/°C
VLO frequency supply voltage drift	df_{VLO}/dV_{CC}	T_A = 25°C 26/	1.8 V – 3.6 V		4		%/V
Crystal Oscillator (LFXT1) high frequency modes 21/							
LFXT1 oscillator crystal frequency, HF mode 0	$f_{LFXT1,HF0}$	XTS = 1, LFXT1Sx = 0	1.8 V to 3.6 V	0.4		1	MHz
LFXT1 oscillator crystal frequency, HF mode 1	$f_{LFXT1,HF1}$	XTS = 1, LFXT1Sx = 1	1.8 V to 3.6 V	1		4	
LFXT1 oscillator crystal frequency, HF mode 2	$f_{LFXT1,HF2}$	XTS = 1, LFXT1Sx = 2	1.8 V to 3.6 V	2		10	
			2.2 V to 3.6 V	2		12	
			3 V to 3.6 V	2		16	
LFXT1 oscillator logic level square wave input frequency, HF mode	$f_{LFXT1,HF,logic}$	XTS = 1, LFXT1Sx = 3	1.8 V to 3.6 V	0.4		10	
			2.2 V to 3.6 V	0.4		12	
			3 V to 3.6 V	0.4		16	
Oscillation allowance for HF crystals See figure 9	OA_{HF}	XTS = 0, LFXT1Sx = 0; $f_{LFXT1,HF}$ = 1 MHz, $C_{L,eff}$ = 15 pF			2700		Ω
		XTS = 0, LFXT1Sx = 1; $f_{LFXT1,HF}$ = 1 MHz, $C_{L,eff}$ = 15 pF			800		
		XTS = 0, LFXT1Sx = 2; $f_{LFXT1,HF}$ = 1 MHz, $C_{L,eff}$ = 15 pF			300		
Integrated effective load capacitance, HF mode 22/		XTS = 1 27/			1		pF
HF mode	Duty cycle	XTS = 1, Measured at P1.4/ACLK, $f_{LFXT1,HF}$ = 10 MHz	2.2 V/3 V	40	50	60	%
		XTS = 1, Measured at P1.4/ACLK, $f_{LFXT1,HF}$ = 16 MHz		40	50	60	
Oscillator fault frequency, HF mode 23/	$f_{Fault,HF}$	XTS = 1, LFXT1Sx = 3 24/	2.2 V/3 V	30		300	kHz
Timer_A							
Timer_A clock frequency	f_{TA}	Internal: SMCLK, ACLK, External: TACLK, INCLK, Duty cycle = 50% ±10%	2.2 V			10	MHz
			3 V			16	
Timer_A, capture timing	$f_{TA,cap}$	TA0, TA1, TA2	2.2 V/3 V	20			ns
Timer_B							
Timer_B clock frequency	f_{TB}	Internal: SMCLK, ACLK, External: TBCLK, Duty cycle = 50% ±10%	2.2 V			10	MHz
			3 V			16	
Timer_B, capture timing	$f_{TB,cap}$	TB0, TB1, TB2	2.2 V/3 V	20			ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ $-55°C \le T_A \le 125°C$ unless otherwise specified	V_{CC}	Limits			Unit
				Min	Typ	Max	
USCI (UART mode)							
USCI input clock frequency	f_{USCI}	Internal: SMCLK, ACLK, External: TBCLK, Duty cycle = 50% ±10%				f_{SYSTEM}	MHz
BITCLK clock frequency (equals baud rate in MBaud)	f_{BITCLK}		2.2 V/3 V			1	
UART receive deglitch time 28/	t_ζ		2.2 V	50	150	600	ns
			3 V	50	150	600	
USCI (SPI Master mode) See figure 10							
USCI input clock frequency		SMCLK, ACLK, Duty cycle = 50% ±10%				f_{SYSTEM}	MHz
SOMI input data setup time	$t_{SU,MI}$		2.2 V	110			ns
			3 V	75			
SOMI input data hold time	$t_{HD,MI}$		2.2 V	0			
			3 V	0			
SIMO output data valid	$t_{VALID,MO}$	UCLK edge to SIMO valid, C_L = 20 pF	2.2 V			30	
			3 V			20	
USCI (SPI Slave mode) See figure 11							
STE lead time, STE low to clock	$t_{STE,LEAD}$		2.2 V/3 V		50		ns
STE lag time, last clock to STE high	$t_{STE,LAG}$		2.2 V/3 V	10			
STE access time, STE low to SOMI data out	$t_{STE,ACC}$		2.2 V/3 V		50		
STE disable time, STE high to SOMI high impedance	$t_{STE,DIS}$		2.2 V/3 V		50		
SIMO input data setup time	$t_{SU,SI}$		2.2 V	20			
			3 V	15			
SIMO input data hold time	$t_{HD,SI}$		2.2 V	10			
			3 V	10			
SOMI output data valid	$t_{VALID,SO}$	UCLK edge to SOMI valid, C_L = 20 pF	2.2 V		75	110	
			3 V		50	75	
USCI (I2C mode) See figure 12							
USCI clock frequency	f_{USCI}	Internal: SMCLK, ACLK, External: UCLK, Duty cycle = 50% ±10%			f_{SYSTEM}		MHz
SCL clock frequency	f_{SCL}		2.2 V/3 V	0		400	µs
Hold time (repeated) START	$t_{HD,STA}$	$f_{SCL} \le 100$ kHz	2.2 V/3 V	4.0			
		$f_{SCL} > 100$ kHz		0.6			
Setup time for a repeated START	$t_{SU,STA}$	$f_{SCL} \le 100$ kHz	2.2 V/3 V	4.7			
		$f_{SCL} > 100$ kHz		0.6			
Data hold time	$t_{HD,DAT}$		2.2 V/3 V	0			ns
Data setup time	$t_{SU,DAT}$		2.2 V/3 V	250			
Setup time for STOP	$t_{SU,STO}$		2.2 V/3 V	4.0			µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	T_A	V_{CC}	Limits			Unit
					Min	Typ	Max	
USCI (I2C mode) - Continued								
Pulse width of spikes suppressed by input filter	t_{SP}		-55°C to 125°C	2.2 V	50	150	600	ns
				3 V	50	150	600	
10 Bit ADC, Power supply and input range conditions								
Analog supply voltage range 30/	V_{CC}	V_{SS} = 0 V			2.2		3.6	V
Analog input voltage range	V_{Ax}	All Ax terminal, Analog input selected in ADC10AE register	-55°C to 125°C		0		V_{CC}	V
ADC10 supply current 31/	I_{ADC10}	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 1, REFON = 0, ADC10SHT0 = 1, ADC10SHT1 = 0, ADC10DIV = 0	-55°C to 125°C	2.2 V		0.52	1.05	mA
				3 V		0.6	1.2	
Reference supply current, reference buffer disabled 32/	I_{REF+}	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REF2_5 = 0, REFON = 1, REFOUT = 0	-55°C to 125°C	2.2 V/3 V		0.25	0.4	
		$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REF2_5 = 1, REFON = 1, REFOUT = 0	-55°C to 125°C	3 V				
Reference buffer supply current with ADC10SR = 0 32/	$I_{REFB,0}$	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REFON = 1,REF2_5 = 0, REFOUT = 1, ADC10SR = 0	-55°C to 85°C	2.2 V/3 V		1.1	1.4	
			125°C	2.2 V/3 V			1.8	
Reference buffer supply current with ADC10SR = 1 32/	$I_{REFB,0}$	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REFON = 1,REF2_5 = 0, REFOUT = 1, ADC10SR = 0	-55°C to 85°C	2.2 V/3 V		0.5	0.7	
			125°C	2.2 V/3 V			0.8	
Input capacitance	C_I	Only one terminal Ax selected at a time				27		pF
Input MUX ON resistance	R_I	0 V ≤ V_{AX} ≤ V_{CC}		2.2 V/3 V		2000		Ω

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ $-55°C \le T_A \le 125°C$ unless otherwise specified		V_{CC}	Limits			Unit
					Min	Typ	Max	
10 Bit ADC, Built in voltage reference								
Positive built in reference analog supply voltage range	$V_{CC,REF+}$	$I_{VREF+} \le 1$ mA, REF2_5V = 0			2.2			V
		$I_{VREF+} \le 0.5$ mA, REF2_5V = 1			2.8			
		$I_{VREF+} \le 1$ mA, REF2_5V = 1			2.9			
Positive built in reference voltage	V_{REF+}	$I_{VREF+} \le I_{VREF+}$max, REF2_5V = 0		2.2 V/3 V	1.41	1.5	1.59	
		$I_{VREF+} \le I_{VREF+}$max, REF2_5V = 1		3 V	2.35	2.5	2.65	
Maximum V_{REF+} load current	$I_{LD,REF+}$			2.2 V			±0.5	mA
				3 V			±1	
V_{REF+} load regulation		I_{VREF+} = 500 µA ±100 µA, Analog input voltage $V_{Ax} \approx 0.75$ V, REF2_5V = 0					±2	LSB
		I_{VREF+} = 500 µA ±100 µA, Analog input voltage $V_{Ax} \approx 1.25$ V, REF2_5V = 1					±2	
V_{REF+} load regulation response time		I_{VREF+} = 100 µA to 900 µA $V_{Ax} \approx 0.5 \times V_{REF+}$, Error conversion result ≤ 1 LSB	ADC10SR = 0				400	ns
			ADC10SR = 1				2000	
Maximum capacitance at pin V_{REF+} 33/	C_{VREF+}	$I_{VREF+} \le 1$ mA, REFON = 1, REFOUT = 1		2.2 V/3 V			100	pF
Temperature coefficient	TC_{REF+}	$I_{VREF+} \le$ const. with 0 mA ≤ $I_{VREF+} \le 1$ mA		2.2 V/3 V			±100	ppm/°C
Setting time of internal reference voltage 34/	t_{REFON}	I_{VREF+} = 0.5 mA, REF2_5V = 0, REFON = 0 to 1		3.6 V			30	µs
Setting time of reference buffer 34/	$t_{REFBURST}$	I_{VREF+} = 0.5 mA, REF2_5V = 0, REFON = 1, REFBURST = 1	ADC10SR = 0	2.2 V			1	
			ADC10SR = 1				2.5	
		I_{VREF+} = 0.5 mA, REF2_5V = 0, REFON = 1, REFBURST = 1	ADC10SR = 0	3 V			2	
			ADC10SR = 1				4.5	
Positive external reference input voltage range 36/	V_{eREF+}	$V_{eREF+} > V_{eREF-}$, SREF1 = 1, SREF0 = 0			1.4		V_{CC}	V
		$V_{eREF-} \le V_{eREF+} \le V_{CC} - 0.15$ V, SREF1 = 1, SREF0 = 1 37/			1.4		3.0	
Negative external reference input voltage range 38/	V_{eREF-}	$V_{eREF+} > V_{eREF-}$			0		1.2	
Differential external reference input voltage range, $\Delta V_{eREF} = V_{eREF+} - V_{eREF-}$	ΔV_{eREF}	$V_{eREF+} > V_{eREF-}$ 39/			1.4		V_{CC}	
Static input current into V_{eREF-}	I_{VeREF+}	$0 V \le V_{eREF+} \le V_{CC}$,SREF1 = 1, SREF0 = 0		2.2 V/3 V			±1	µA
		$0 V \le V_{eREF+} \le V_{CC} - 0.15 V \le 3 V$, SREF1 = 1, SREF0 = 1 37/		2.2 V/3 V			0	
Static input current into V_{eREF-}	I_{VeREF-}	$0 V \le V_{eREF-} \le V_{CC}$		2.2 V/3 V			±1	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ -55°C ≤ T_A ≤ 125°C unless otherwise specified		V_{CC}	Limits			Unit
					Min	Typ	Max	
10 Bit ADC, Timing parameters								
ADC10 input clock frequency	$f_{ADC10CLK}$	For specified performance of ADC10 linearity parameters	ADC10SR = 0	2.2 V/3 V	0.45		6.5	MHz
			ADC10SR = 1	2.2 V/3 V	0.45		1.5	
ADC10 built in oscillator frequency	$f_{ADC10OSC}$	ADC10DIVx = 0, adc10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$		2.2 V/3 V	3.25		6.45	
Conversion time	$t_{CONVERT}$	ADC10 built in oscillator, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$		2.2 V/3 V	2.06		3.51	µs
		$f_{ADC10CLK}$ from ACLK, MCLK, or SMCLK: ADC10SSELx ≠ 0			13 = ADC10DIVx $1/f_{ADC10CLK}$			
Turn on setting time of ADC 40/	$t_{ADC10ON}$						100	ns
10 Bit ADC, Linearity parameters								
Integral linearity error	E_I			2.2 V/3 V			±1	LSB
Differential linearity error	E_D			2.2 V/3 V			±1	
Offset error	E_O	Source impedance R_S < 100 Ω		2.2 V/3 V			±1	
Gain error	E_G	SREFx = 010, un-buffered external reference, V_{eREF+} = 1.5 V		2.2 V		±1.1	±2	
		SREFx = 010, un-buffered external reference, V_{eREF+} = 2.5 V		3 V		±1.1	±2	
		SREFx = 011, buffered external reference, V_{eREF+} = 1.5 V 42/		2.2 V		±1.1	±4	
		SREFx = 011, buffered external reference, V_{eREF+} = 2.5 V 42/		3 V		±1.1	±3	
Total unadjusted error	E_T	SREFx = 010, un-buffered external reference, V_{eREF+} = 1.5 V		2.2 V		±2	±5	
		SREFx = 010, un-buffered external reference, V_{eREF+} = 2.5 V		3 V		±2	±5	
		SREFx = 011, buffered external reference, V_{eREF+} = 1.5 V 42/		2.2 V		±2	±7	
		SREFx = 011, buffered external reference, V_{eREF+} = 2.5 V 42/		3 V		±2	±6	

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See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ $-55°C \le T_A \le 125°C$ unless otherwise specified	V_{CC}	Limits			Unit
				Min	Typ	Max	
10 Bit ADC, Temperature Sensor and Built in V_{MID}							
Temperature sensor supply current 43/	I_{SENSOR}	REFON = 0, INCHx = 0Ah, $T_A = 25°C$	2.2 V		40	120	µA
			3 V		60	160	
	TC_{SENSOR}	ADC10ON = 1, INCHx = 0Ah 44/	2.2 V/3 V	3.44	3.55	3.66	mV/°C
Sensor offset voltage	$V_{Offset,Sensor}$	ADC10ON = 1, INCHx = 0Ah 44/		-100		100	mV
Sensor output voltage 45/		Temperature sensor voltage at $\le T_A = 125°C$ (T version only)	2.2 V/3 V	1265	1365	1465	mV
		Temperature sensor voltage at $T_A = 85°C$		1195	1295	1395	
		Temperature sensor voltage at $T_A = 25°C$		985	1085	1185	
		Temperature sensor voltage at $T_A = 0°C$		895	995	1095	
Sample time required if channel 10 is selected 46/	$t_{Sensor(sample)}$	ADC10ON = 1, INCHx = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V/3 V	30			µs
Current into divider at channel 11 47/	I_{VMID}	ADC10ON = 1, INCHx = 0Bh	2.2 V			NA	µA
			3 V			NA	
V_{CC} divider at channel 11	V_{MID}	ADC10ON = 1, INCHx = 0Bh V_{MID} is ≈ 0.5 x V_{CC}	2.2 V	1.06	1.1	1.14	V
			3 V	1.46	1.5	1.54	
Sample time required if channel 11 is selected 48/	$t_{VMID(sample)}$	ADC10ON = 1, INCHx = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V	1400			ns
			3 V	1220			
Operational Amplifier (OA) supply specifications							
Supply voltage range	V_{CC}			2.2		3.6	V
Supply current 49/	I_{CC}	Fast mode	2.2 V/3 V		180	290	µA
		Medium mode			110	190	
		Slow mode			50	80	
Power supply rejection ratio	PSSR	Noninverting			70		dB

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See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ -55°C ≤ T_A ≤ 125°C unless otherwise specified		V_{CC}	Limits			Unit
					Min	Typ	Max	
Operational Amplifier (OA) Input/Output specifications								
Input voltage range	$V_{I/P}$				-0.1		V_{CC} – 1.2	V
Input leakage current 50/ 51/	I_{lkg}	-55°C ≤ T_A ≤ 55°C		2.2 V/3 V	-15	±0.5	15	nA
		55°C ≤ T_A ≤ 85°C			-20	±5	20	
		85°C ≤ T_A ≤ 125°C			-100		100	
Voltage noise density, I/P	V_n	Fast mode	$f_{V(I/P)}$ = 1 kHz			50		nV/$\sqrt{Hz}$
		Medium mode				80		
		Slow mode				140		
		Fast mode	$f_{V(I/P)}$ = 10 kHz			30		
		Medium mode				50		
		Slow mode				65		
Offset voltage, I/P	V_{IO}			2.2 V/3 V			±10	mV
Offset temperature drift, I/P		52/				±10		µV/°C
Offset temperature drift with supply, I/P		0.3 V ≤ V_{IN} ≤ V_{CC} – 1.0 V, ΔV_{CC} ≤ ±10%, T_A = 25°C					±1.5	mV/V
High level output voltage, O/P	V_{OH}	Fast mode, I_{SOURCE} ≤ -500 µA			V_{CC} – 0.2		V_{CC}	V
		Slow mode, I_{SOURCE} ≤ -150 µA			V_{CC} – 0.1		V_{CC}	
Low level output voltage, O/P	V_{OL}	Fast mode, I_{SOURCE} ≤ 500 µA			V_{SS}		0.2	
		Slow mode, I_{SOURCE} ≤ 150 µA			V_{SS}		0.1	
Output resistance 53/ See figure 13	$R_{O/P(OAx)}$	R_{Load} = 3 kΩ, C_{Load} = 50 pF, $V_{O/P(OAx)}$ < 0.2 V				150		Ω
		R_{Load} = 3 kΩ, C_{Load} = 50 pF, $V_{O/P(OAx)}$ > V_{CC} – 1.2 V				150		
		R_{Load} = 3 kΩ, C_{Load} = 50 pF, 0.2 V ≤ $V_{O/P(OAx)}$ ≤ V_{CC} – 1.2 V				0.1		
Common mode rejection ratio	CMRR	Noninverting				70		dB
Operational Amplifier (OA) Dynamic specifications								
Slew rate	SR	Fast mode				1.2		V/µs
		Medium mode				0.8		
		Slow mode				0.3		
Open loop voltage gain						100		dB
Phase margin		C_L = 50 pF				60		deg
Gain margin						20		dB
Gain bandwidth product See figure 14	GBW	Noninverting, Fast mode, R_L = 47 kΩ, C_L = 50 pF		2.2 V/3 V		2.2		MHz
		Noninverting, Medium mode, R_L = 300 kΩ, C_L = 50 pF				1.4		
		Noninverting, Slow mode, R_L = 300 kΩ, C_L = 50 pF				0.5		
Enable time on	$t_{en(on)}$	t_{on}, noninverting, Gain = 1				10	20	µs
Enable time off	$t_{en(off)}$						1	

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See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	T_A	V_{CC}	Limits			Unit
					Min	Typ	Max	
Operational Amplifier (OA) Feedback network, Resistor network 54/								
Total resistance of resistor string	R_{total}					96		kΩ
Unit resistor of resistor string 55/	R_{unit}					6		
Operational Amplifier (OA) Feedback network, Comparator mode (OAFCx = 3)								
Comparator level	V_{Level}	OAFBRx = 1, OARRIP = 0	-55°C to 125°C	2.2 V/3 V	0.242	0.25	0.262	V_{CC}
		OAFBRx = 2, OARRIP = 0	-55°C to 125°C		0.492	0.5	0.512	
		OAFBRx = 3, OARRIP = 0	-55°C to 125°C		0.619		0.639	
		OAFBRx = 4, OARRIP = 0			N/A 56/			
		OAFBRx = 5, OARRIP = 0			N/A 56/			
		OAFBRx = 6, OARRIP = 0			N/A 56/			
		OAFBRx = 7, OARRIP = 0			N/A 56/			
		OAFBRx = 1, OARRIP = 1	-55°C to 125°C		0.057	0.0625	0.071	
		OAFBRx = 2, OARRIP = 1	-55°C to 125°C		0.122	0.125	0.128	
		OAFBRx = 3, OARRIP = 1	-55°C to 125°C		0.182	0.187	0.197	
		OAFBRx = 4, OARRIP = 1	-55°C to 125°C		0.242	0.25	0.262	
		OAFBRx = 5, OARRIP = 1	-55°C to 125°C		0.367	0.375	0.383	
		OAFBRx = 6, OARRIP = 1	-55°C to 125°C		0.492	0.50	0.512	
		OAFBRx = 7, OARRIP = 1	-55°C to 125°C		N/A 56/			
Propagation delay (low high and high low)	t_{PLH}, t_{PHL}	Fast mode, Overdrive 10 mV		2.2 V/3 V		40		µs
		Fast mode, Overdrive 100 mV				4		
		Fast mode, Overdrive 500 mV				3		
		Medium mode, Overdrive 10 mV				60		
		Medium mode, Overdrive 100 mV				6		
		Medium mode, Overdrive 500 mV				5		
		Slow mode, Overdrive 10 mV				160		
		Slow mode, Overdrive 100 mV				20		
		Slow mode, Overdrive 500 mV				15		
Operational Amplifier (OA) Feedback network, Noninverting Amplifier Mode (OAFCx = 4)								
Gain	G	OAFBRx = 0	-55°C to 125°C	2.2 V/3 V	0.970	1.00	1.035	
		OAFBRx = 1	-55°C to 125°C		1.325	1.334	1.345	
		OAFBRx = 2	-55°C to 125°C		1.985	2.001	2.017	
		OAFBRx = 3	-55°C to 125°C		2.638	2.667	2.696	
		OAFBRx = 4	-55°C to 125°C		3.94	4.00	4.06	
		OAFBRx = 5	-55°C to 125°C		5.22	5.33	5.44	
		OAFBRx = 6	-55°C to 125°C		7.76	7.97	8.18	
		OAFBRx = 7	-55°C to 125°C		15.0	15.8	16.7	
Total harmonic distortion/nonlinearity	THD	All gains		2.2 V		-60		dB
				3 V		-70		
Setting time 57/	t_{Settle}	All power modes	-55°C to 125°C	2.2 V/3 V		7	12	µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	T_A	V_{CC}	Limits			Unit
					Min	Typ	Max	
Operational Amplifier (OA) Feedback network, Noninverting Amplifier Mode (OAFCx = 6) 58/								
Gain	G	OAFBRx = 1	-55°C to 125°C	2.2 V/3 V	-0.385	-0.335	-0.305	
		OAFBRx = 2	-55°C to 125°C		-1.023	-1.002	-0.979	
		OAFBRx = 3	-55°C to 125°C		-1.712	-1.668	-1.624	
		OAFBRx = 4	-55°C to 125°C		-3.10	-3.00	-2.90	
		OAFBRx = 5	-55°C to 125°C		-4.51	-4.33	-4.15	
		OAFBRx = 6	-55°C to 125°C		-7.37	-6.97	-6.57	
		OAFBRx = 7	-55°C to 125°C		-16.6	-14.8	-13.1	
Total harmonic distortion/nonlinearity	THD	All gains		2.2 V		-60		dB
				3 V		-70		
Setting time 57/	t_{Settle}	All power modes	-55°C to 125°C	2.2 V/3 V		7	12	µs
Flash memory								
Program and erase supply voltage	$V_{CC(PGM/ERASE)}$		-55°C to 125°C		2.2		3.6	V
Flash timing generator frequency	f_{FTG}		-55°C to 125°C		257		476	kHz
Supply current from V_{CC} during program	I_{PGM}		-55°C to 125°C	2.2 V/3.6 V		1	5	mA
Supply current from V_{CC} during erase	I_{ERASE}		-55°C to 125°C	2.2 V/3.6 V		1	10.5	mA
Cumulative program time 59/	t_{CPT}		-55°C to 125°C	2.2 V/3.6 V			10	ms
Cumulative mass erase time	$t_{CMErase}$		-55°C to 125°C		20			ms
Program/Erase endurance			-55°C to 125°C		10^4	10^5		cycles
Data retention duration 60/	$t_{Retention}$	T_J = 25°C			100			yeras
Word or byte program time	t_{Word}	61/				30		t_{FTG}
Block program time for 1st byte or word	$t_{Block, 0}$	61/				25		
Block program time for each additional byte or word	$t_{Block, 1-63}$	61/				18		
Block program end-sequence wait time	$t_{Block, End}$	61/				6		
Mass erase time	$t_{Mass Erase}$	61/				10593		
Segment erase time	$t_{Seg Erase}$	61/				4819		
RAM								
RAM retention supply voltage 62/	$V_{(RAMh)}$	CPU halted	-55°C to 125°C		1.6			V

.

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	T_A	V_{CC}	Limits			Unit
					Min	Typ	Max	
JTAG and Spy-Bi-Wire interface								
Spy-Bi-Wire input frequency	f_{SBW}		-55°C to 125°C	2.2 V/3 V	0		20	MHz
Spy-Bi-Wire low clock pulse length	$t_{SBW,Low}$		-55°C to 125°C	2.2 V/3 V	0.025		15	µs
Spy-Bi-Wire enable time (Test high to acceptance of first clock edge 63/)	$t_{SBW,En}$		-55°C to 125°C	2.2 V/3 V			1	
Spy-Bi-Wire return to normal operation time	$t_{SBW,Ret}$		-55°C to 125°C	2.2 V/3 V	15		100	
TCK input frequency 64/	f_{TCK}		-55°C to 125°C	2.2 V	0		5	MHz
				3 V	0		10	
Internal pulldown resistance on TEST	$R_{Internal}$		-55°C to 125°C	2.2 V/3 V	25	60	90	kΩ
JTAG Fuse 65/								
Supply voltage during fuse-blow condition	$V_{CC(FB)}$		25°C		2.5			V
Voltage level on TEST for fuse blow	V_{FB}		-40°C to 125°C		6		7	V
Supply current into TEST during fuse blow	I_{FB}		-40°C to 125°C				100	mA
Time to blow fuse	t_{FB}		-40°C to 125°C				1	ms

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
2/ Over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted).
3/ All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
4/ The current are characterized micro crystal. See manufacture data for more information.
5/ Current for brownout and WDT clocked by SMCLK included.
6/ Current for brownout and WDT clocked by ACLK included.
7/ Current for brownout included.
8/ RST/NMI limit values specified for -55°C to 125°C.
9/ An external signal sets the interrupt flag every time the minimum interrupt pulse width $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$.
10/ The leakage current is measured with VSS or VCC applied to the corresponding pin(s), unless otherwise noted.
11/ The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.
12/ The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
13/ The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
14/ A resistive divider with 2 times 0.5 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.

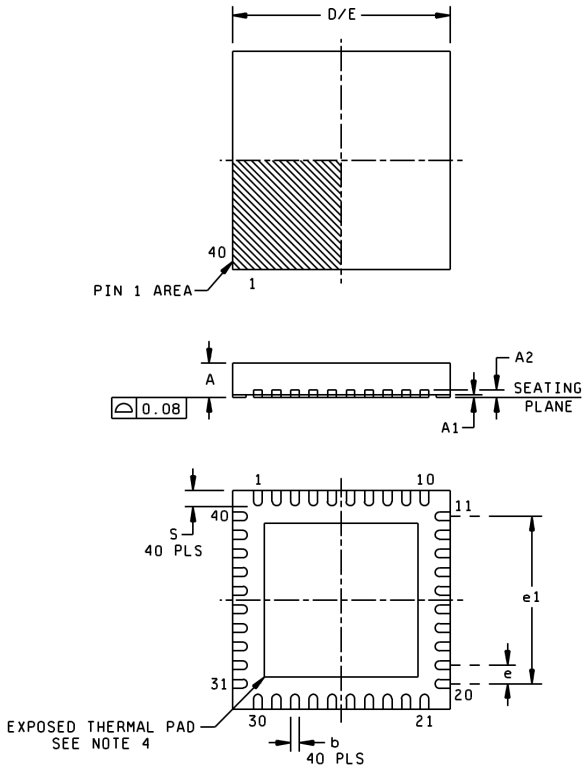
TABLE I. Electrical performance characteristics – Continued. 1/

15/ The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.
16/ The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8 V.
17/ During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$, The default DCO settings must not be changed until $V_{CC} \geq V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency.
18/ The DCO clock wake up time is measured from the edge of an external wake up signal (e.e., port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK)
19/ Parameter applicable only if DCOCLK is used for MCLK.
20/ R_{OSC} = 100kΩ. Metal film resistor, type 0257. 0.6 watt with 1% tolerance and TK = ±50ppm/°C.
21/ To improve EMI on the LFXT1 oscillator the following guidelines should be observed:
   a. Keep as short of a trace as possible between the device and the crystal.
   b. Design a good ground plane around the oscillator pin.
   c. Prevent crosstalk from other clock or data lines into oscillator pin XIN and XOUT.
   d. Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   e. Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   f. If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between oscillator pins.
   g. Do not rout the XOUT line to the JTAG header to support the serial programming adapter as shown in other data. This signal is no longer required for the serial programming adapter.
22/ Includes parasitic bond and package capacitance (approximately 2 pF per pin). Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification on the used crystal.
23/ Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
24/ Measured with logic level input frequency, but also applies to operation with crystals.
25/ Calculated using the box method:
I Version: [MAX(-55…85°C) – MIN(-55…85°C)]/ MIN(-55…85°C)]/[85°C – (-55°C)]
26/ Calculated using the box method:[Max(1.8…3.6V) – MIN(1.8…3.6 V)]/MIN(1.8…3.6 V)/(3.6 V – 1.8 V)
27/ Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
28/ Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that the pulses correctly recognized, their width should exceed the maximum specification of the deglitch time.
29/ The leakage current is defined in the leakage current table with Px.x/Ax parameter.
30/ The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion result.
31/ The internal reference supply current is not included in current consumption parameter I_{ADC10}.
32/ The internal reference current is supplied via terminal VCC. Consumption is independent of the ADC10)N control bit, unless a conversion is active. The REFON bit enables the built in reference to settle before starting an A/D conversion.
33/ The capacitance applied to the internal buffer operational amplifier, if switched to terminal P2.4/TA2/A4/V_{REF+}/V_{eREF+} (REFOUT = 1), must be limited; the reference buffer may become unstable otherwise.
34/ The condition is that the error in a conversion started after t_{REFON} or t_{RefBuf} is less than ±0.5 LSB.
35/ The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog source impedance to allow the change to settle for 10 bit accuracy.
36/ The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.

TABLE I. Electrical performance characteristics – Continued. 1/

37/ Under this condition the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current I_{REFB}. The current consumption can be limited to the sample and conversion period with REBURST = 1.
38/ The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
39/ The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
40/ The condition is that the error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
41/ 2.2 V not production test.
42/ The reference buffer's offset adds to the gain and total unadjusted error.
43/ The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON =1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is included in I_{REF+}. When REFON = 0, I_{SENSOR} applies during conversion of the temperature sensor input (INCH = 0Ah).
44/ The following formula can be used to calculate the temperature sensor output voltage:
$V_{Sensor,typ} = TC_{Sensor} (273+ T[°C]) + V_{Offset,sensor}$ [mV] or
$V_{Sensor,typ} = TC_{Sensor} T[°C] + V_{sensor}(T_A = 0°C)$ [mV]
45/ Results based on characterization and/or production test, not TC_{Sensor} or $V_{Offet,sensor}$.
46/ The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor on time $t_{SENSOR(on)}$.
47/ No additional current is needed. The VMID is used during sample.
48/ The on time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.
49/ Corresponding pins configured as OA inputs and outputs, respectively.
50/ ESD damage can degrade input current leakage.
51/ The input bias current is overridden by the input leakage current.
52/ Calculated using the box method.
53/ Specification valid for voltage-follower OAx configuration.
54/ A single resistor string is composed of 4 R_{unit} + 4 R_{unit} + 2 R_{unit} + 2 R_{unit} + 1 R_{unit} + 1 R_{unit} + 1 R_{unit} + 1 R_{unit} = 16 R_{unit} = R_{total}
55/ For the matching (i.e., the relative accuracy) of the unit resistor on a device, refer to the gain and level specifications of the respective configurations.
56/ The level is not available due to the analog input voltage range of the operational amplifier.
57/ The setting time specifies the time until an ADC result is stable. This includes the minimum required sampling time of the ADC. The setting time of the amplifier itself might be faster.
58/ This includes the 2 OA configuration "Inverting amplifier with input buffer". Both OA needs to be set to the same power mode OAPMx.
59/ The cumulative program time must not be exceeded when writing to a 64 byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
60/ To test the fash data retention at various temperatures we make use of accelerated test on the flash with 500 hours baking time at 250°C. These tests are wholly based on Arrhenius law and equation. For more information refer to figure 15.
61/ These values are hardwired into the Flash Controller's state machine ($t_{FTG} = 1/f_{FTG}$).
62/ This parameter defines the minimum supply voltage VCC when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.
63/ Tools accessing the Spy-Bi-Wire interface need to wait for the maximum $t_{SBW,En}$ time after pulling the TEST/SBWCLK pin high before applying the first SBWCLK clock edge.
64/ f_{TCK} may be restricted to meet the timing requirements of the module selected.
65/ Once the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.

Case X

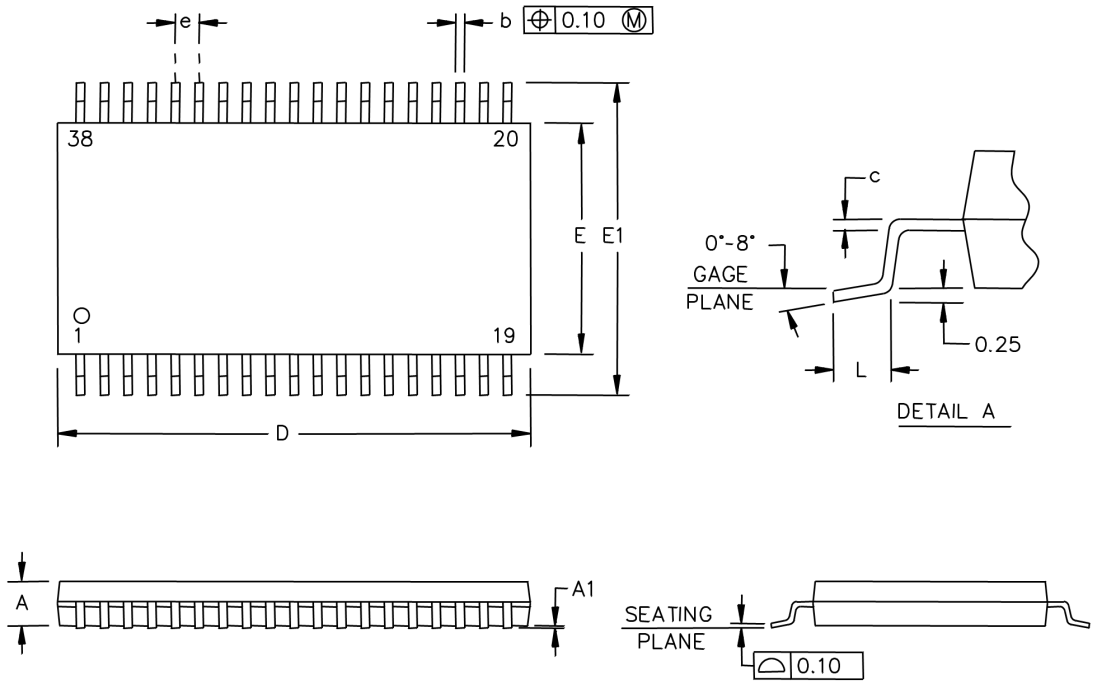


Dimension					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.80	1.00	D/E	5.85	6.15
A1	0.00	0.05	e	0.50 BSC	
A2	0.20 NOM		e1	4.50 BSC	
b	0.18	0.30	S	0.30	0.50

NOTES:
1. All linear dimensions are in millimeters. Dimensioning and tolerance per ASME Y14.5 – 1994.
2. This drawing is subject to change without notice.
3. Quad flatpack, No-leads (QFN) package configuration.
4. The package thermal pad must be soldered to the board for thermal and mechanical performance. See manufacturer data for details regarding the exposed thermal pad dimensions.
5. Package complies to JEDEC MO-220 variation VJJD-2.

FIGURE 1. Case outline.

Case Y



Dimension					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	E	6.00	6.20
A1	0.05	0.15	E1	7.90	8.30
b	0.19	0.30	e	0.65 BSC	
c	0.15 NOM		L	0.50	0.75
D	12.40	12.60			

NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 mm per side.
4. Fall within JEDEC MO-153.

FIGURE 1. Case outline - Continued.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DVSS	21	P4.6/TBOUTH/A15/OA1I3
2	XOUT/P2.7	22	P4.7/TBCLK
3	XIN/P2.6	23	P3.4/UCA0TXD/UCA0SIMO
4	DVSS	24	P3.5/UCA0RXD/UCA/0SOMI
5	RST/NMI/SBWTDIO	25	P3.6/A6/OA0I2
6	P2.0/ACLK/A0/OA0O	26	P3.7/A7/OA1I2
7	P2.1/TAINCLK/SMCLK/A1/OA0O	27	P2.3/TA1/A3/VREF-/VeREF-/OA1I1/OA10
8	P2.2/TA0/A2/OA0I1	28	P2.4/TA2/A4/VREF+/VeREF+/OA1I0
9	P3.0/UCB0STE/UCA0CLK/A5	29	P1.0/TACLK/ADC10CLK
10	P3.1/UCB0SIMO/UCB0SDA	30	P1.1/TA0
11	P3.2/UCB0SOMI/UCB0SCL	31	P1.2/TA1
12	P3.3/UCB0CLK/UCA0STE	32	P1.2/TA2
13	AVSS	33	P1.4/SMCLK/TCK
14	AVCC	34	P1.5/TA0/TMS
15	P4.0/TB0	35	P1.6/TA1/TDI/TCLK
16	P4.1/TB1	36	P1.7/TA2/TDO/TDI
17	P4.2/TB2	37	TEST/SBWTCK
18	P4.0/TB0/A12/OA0O	38	DVCC
19	P4.4/TB1/A13/OA1O	39	DVCC
20	P4.5/TB2/A14/OA0I3	40	P2.5/Rosc

Case outline Y			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	TEST/SBWTCK	20	P4.3/TB0/A12/OA0O
2	DVCC	21	P4.4/TB1/A13/OA1O
3	P2.5/Rosc	22	P4.5/TB2/A14/OA1I3
4	DVSS	23	P4.6/TBOUTH/A15/OA1I3
5	XOUT/P2.7	24	P4.7/TBCLK
6	XIN/P2.6	25	P3.4/UCA0TXD/UCA0SIMO
7	RST/NMI/SBWTDIO	26	P3.5/UCA0RXD/UCA0SIMO
8	P2.0/ACLK/A0/OA0I0	27	P3.6/A6/OA0I2
9	P2.1/TAINCLK/SMCLK/A1/OA00	28	P3.7/A7/OA1I2
10	P2.2/TA0/A2/OA0I1	29	P2.3/TA1/A3/VREF-/VeREF-/OA1I1/OA10
11	P3.0/UCB 0STE/UCA 0CLK/A5	30	P2.4/TA2/A4/VREF+/VeREF+/OA1I0
12	P3.1/UCB 0SIMO/UCB 0SDA	31	P1.0/TACLK/ADC 10CLK
13	P3.2/UCB 0SOMI/ UCB 0SCL	32	P1.1/TA0
14	P3.3/UCB 0CLK/UCA 0STE	33	P1.2/TA1
15	AVSS	34	P1.3/TA2
16	AVCC	35	P1.4/SMCLK/TCK
17	P4.0/TB0	36	P1.5/TA0/TMS
18	P4.1/TB1	37	P1.6/TA1/TDI
19	P4.2/TB2	38	P1.7/TA2/TDO/TDI

FIGURE 2. Terminal connections.

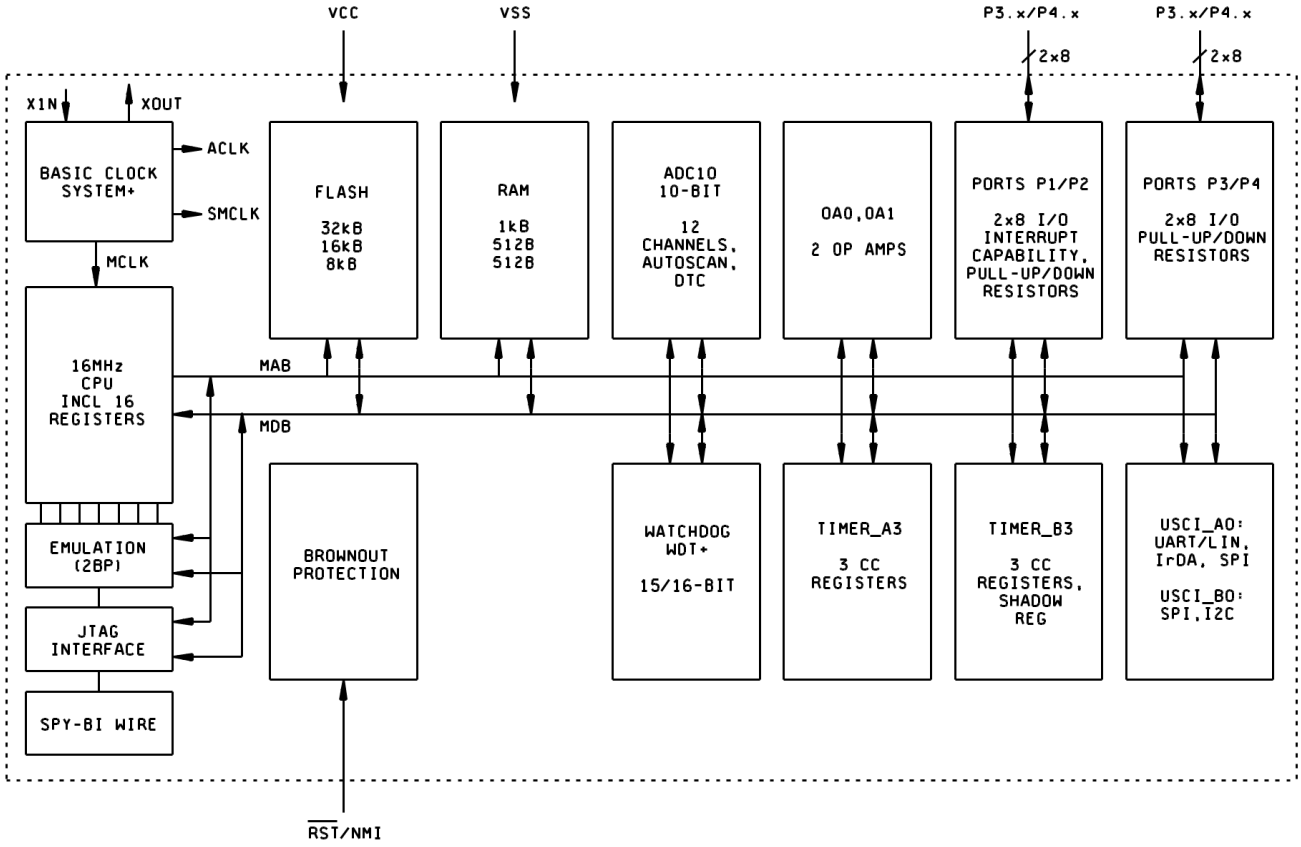


FIGURE 3. Functional block diagram.

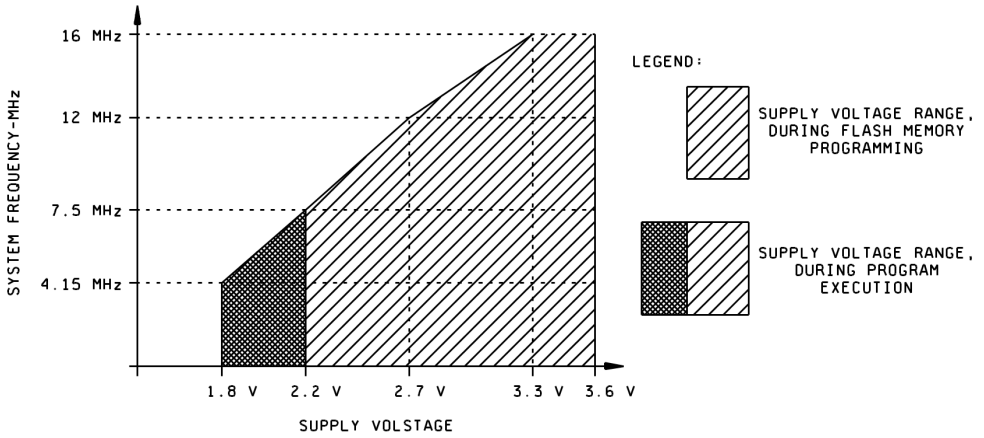
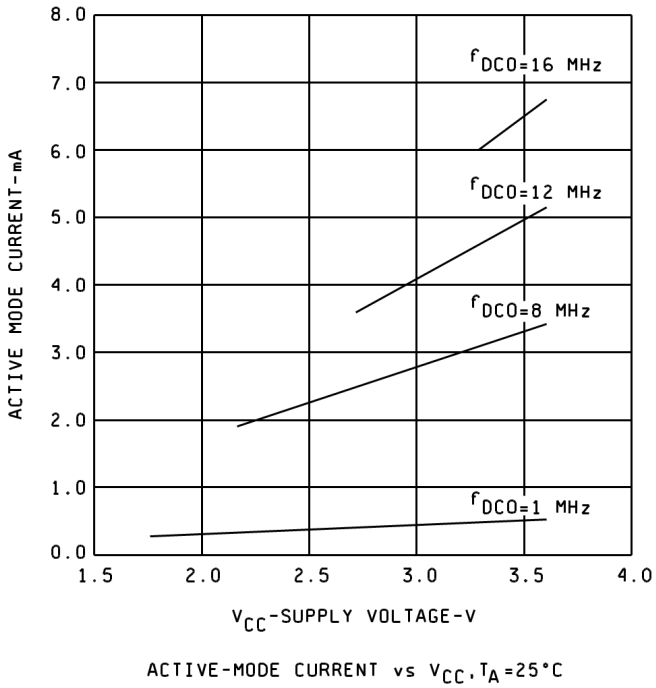


FIGURE 4. Operating area.



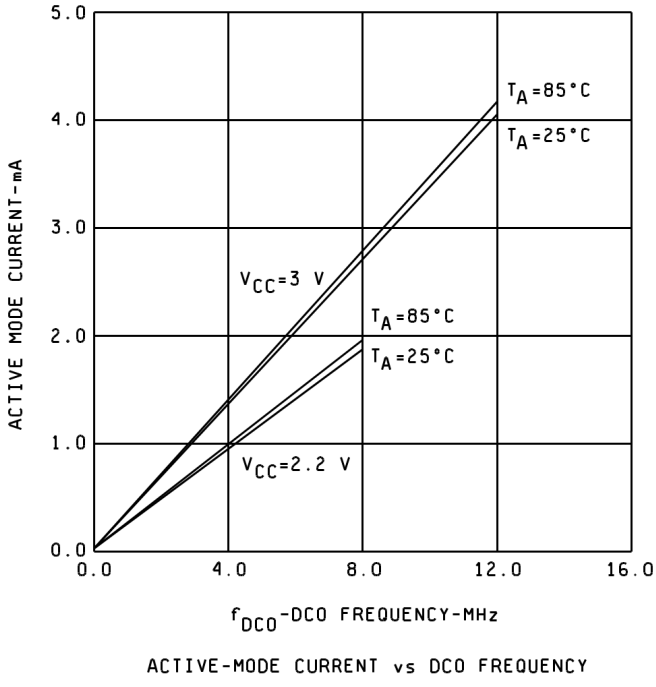


FIGURE 5. Active mode supply current.

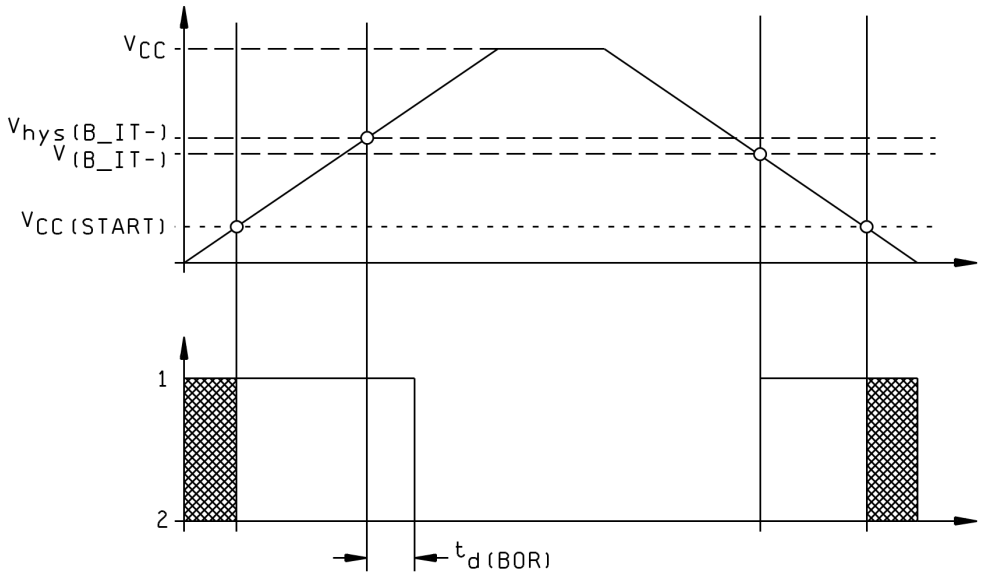
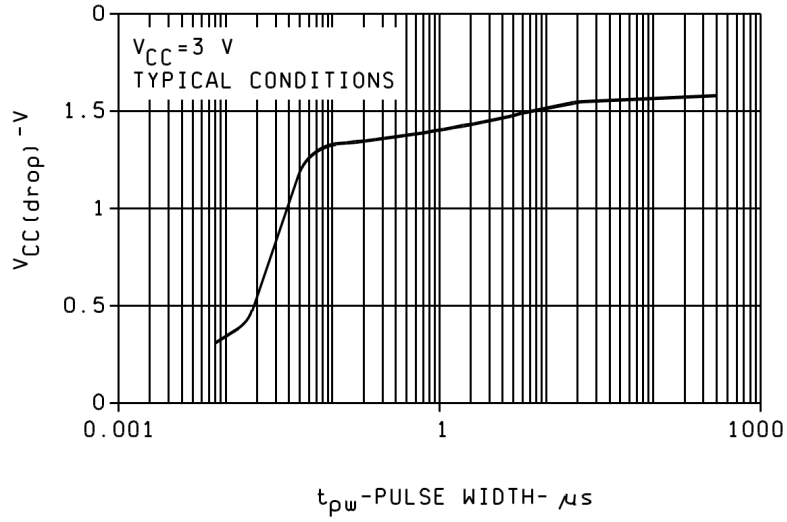
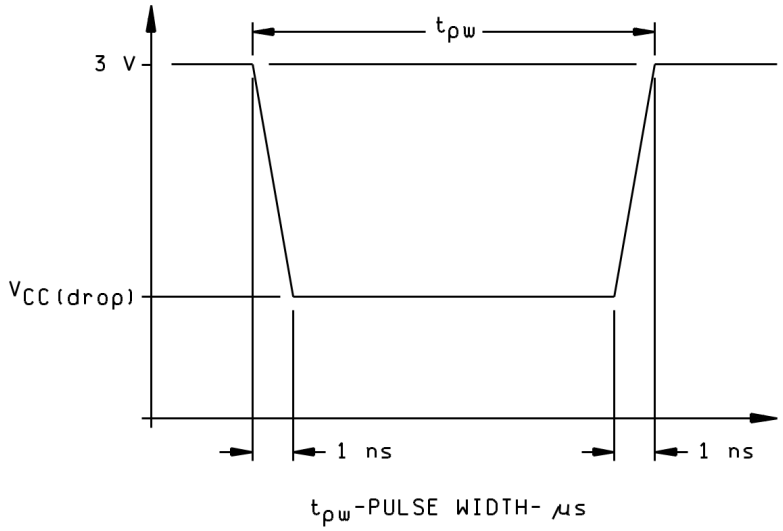


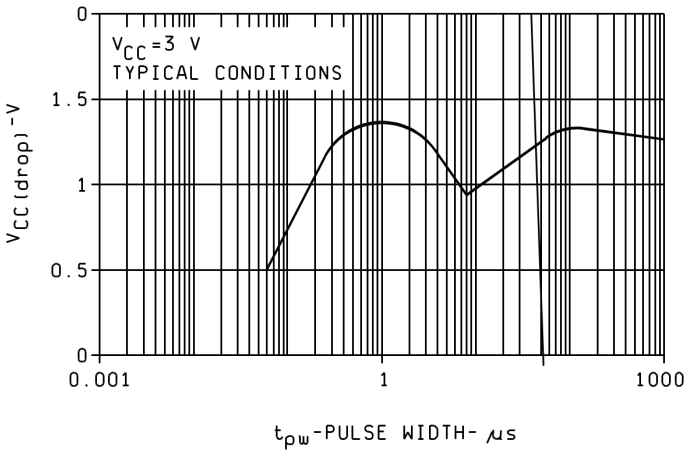
FIGURE 6. POR/Brownout reset.

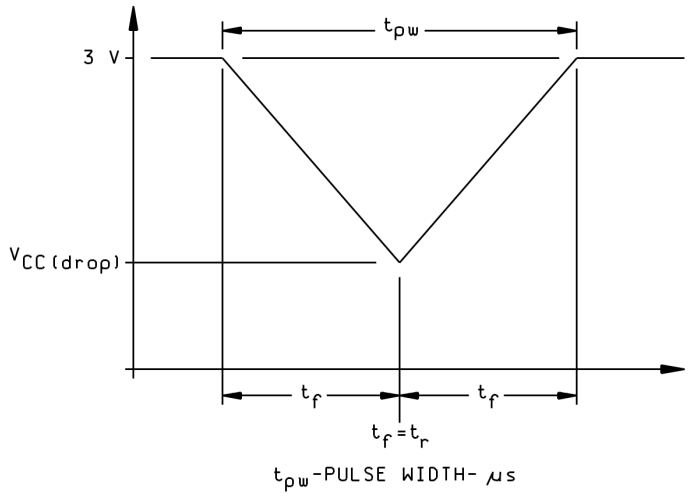




$V_{CC(drop)}$ LEVEL WITH A SQUARE VOLTAGE DROP TO GENERATE A POR/BROWNOUT SIGNAL

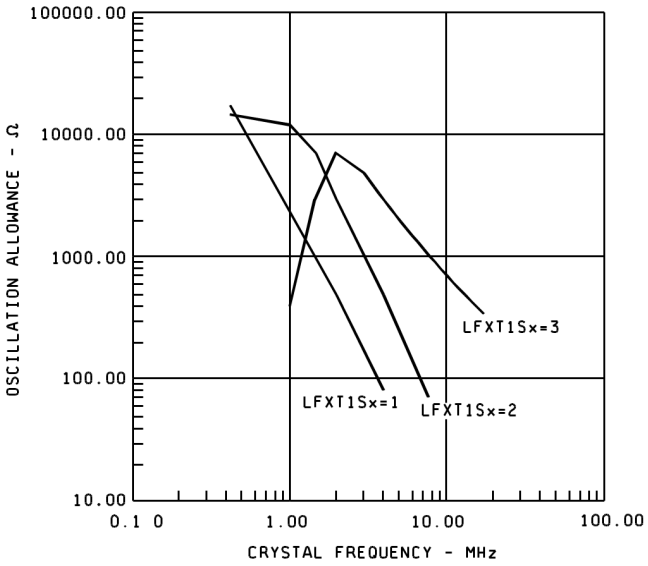
FIGURE 7. POR/Brownout reset.



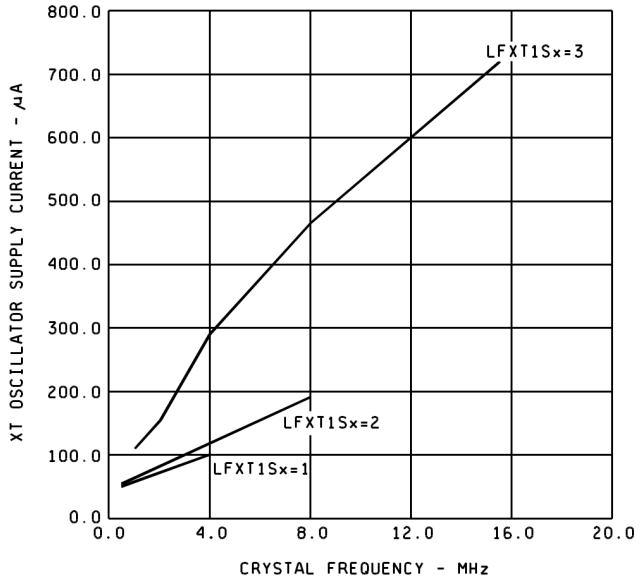


$V_{CC(drop)}$ LEVEL WITH A TRIANGLE VOLTAGE DROP TO GENERATE A POR/BROWNOUT SIGNAL

FIGURE 8. POR/Brownout reset.

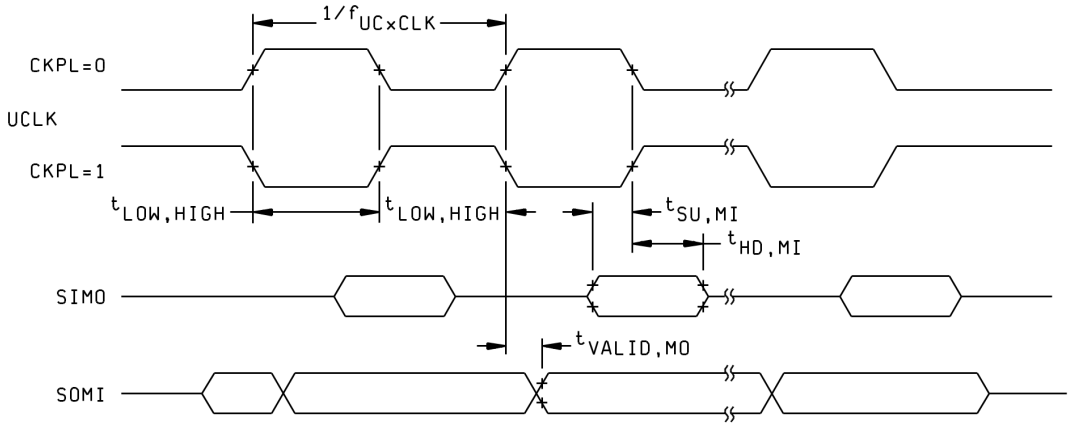


OSCILLATION ALLOWANCE vs CRYSTAL FREQUENCY, $C_{L,eff}$=15 pF, T_A=25°C

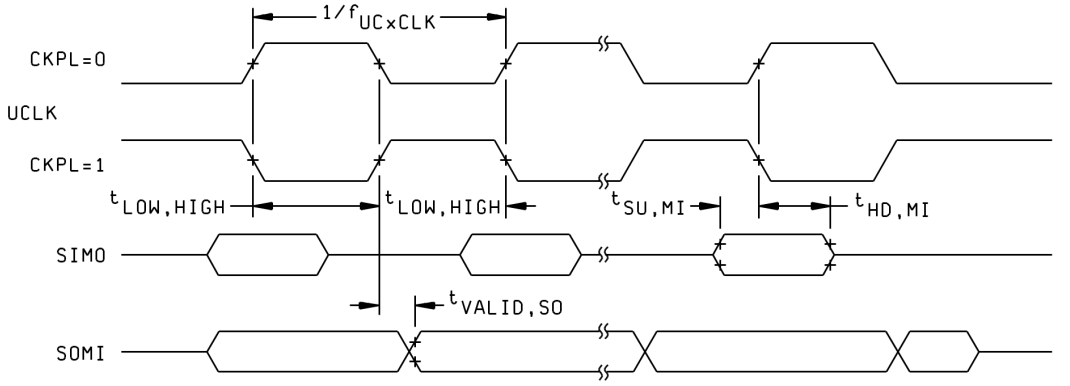


XT OSCILLATOR SUPPLY CURRENT vs CRYSTAL FREQUENCY, $C_{L,eff}$=15 pF, T_A=25°C

FIGURE 9. Test circuit and timing waveforms.

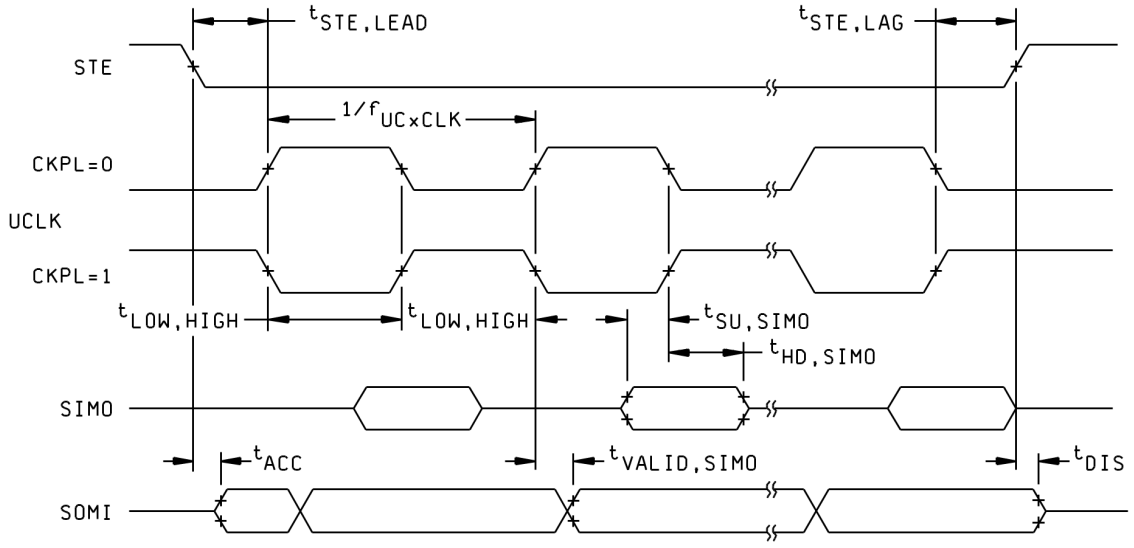


SPI SLAVE MODE, CKPH = 0

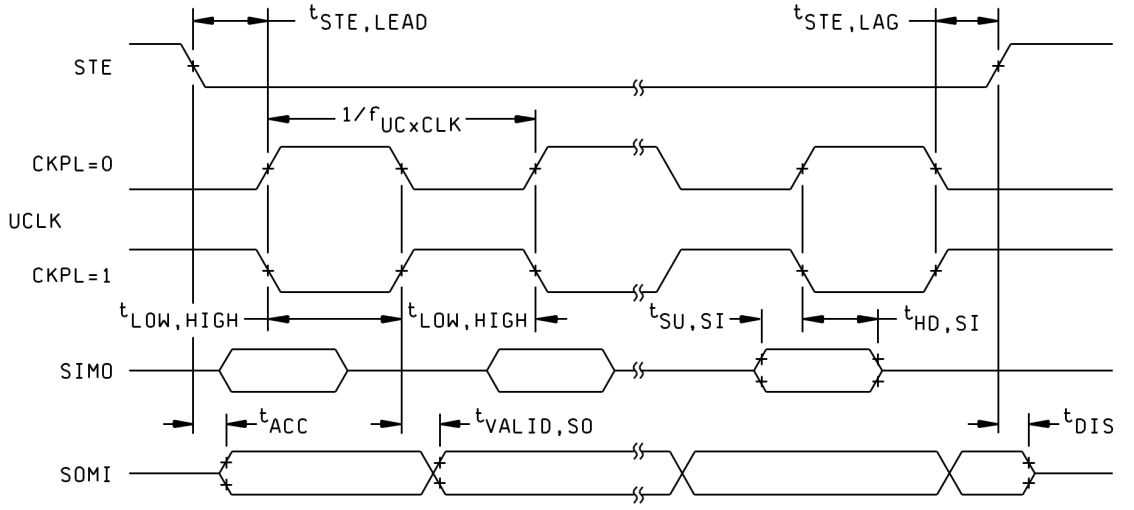


SPI SLAVE MODE, CKPH = 1

FIGURE 10. Test circuit and timing waveforms.



SPI SLAVE MODE, CKPH = 0



SPI SLAVE MODE, CKPH = 1

FIGURE 11. Test circuit and timing waveforms.

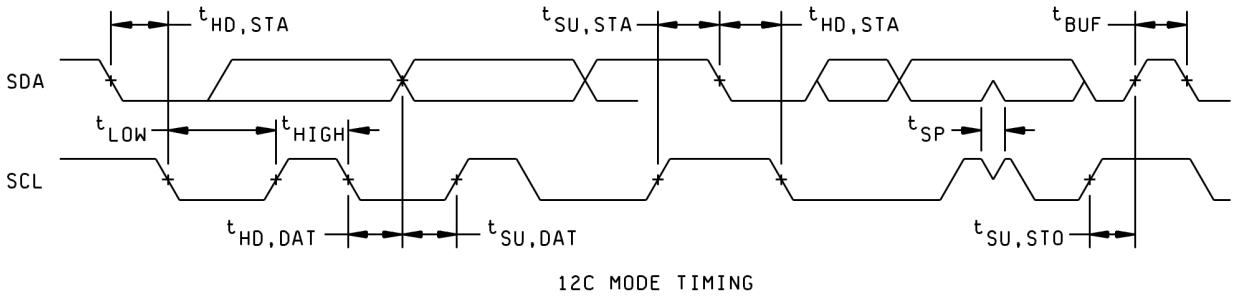


FIGURE 12. Test circuit and timing waveforms.

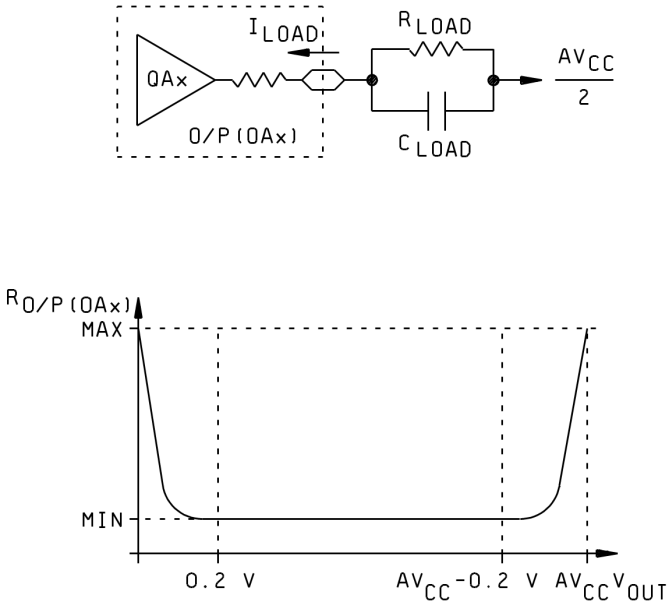


FIGURE 13. Test circuit and timing waveforms.

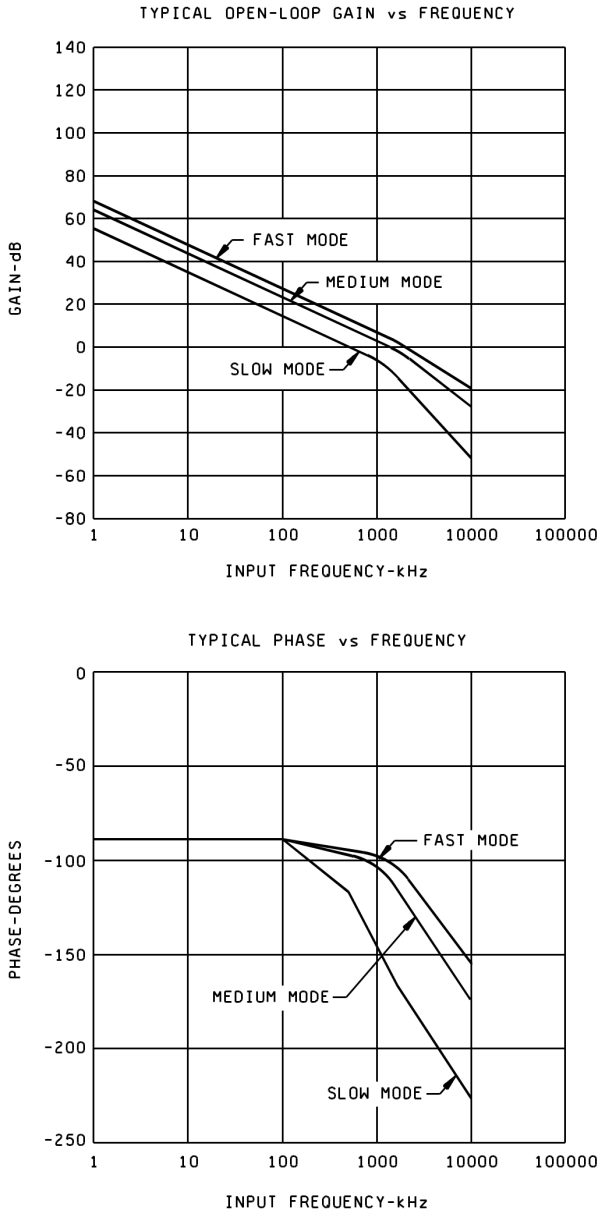


FIGURE 14. Test circuit and timing waveforms.

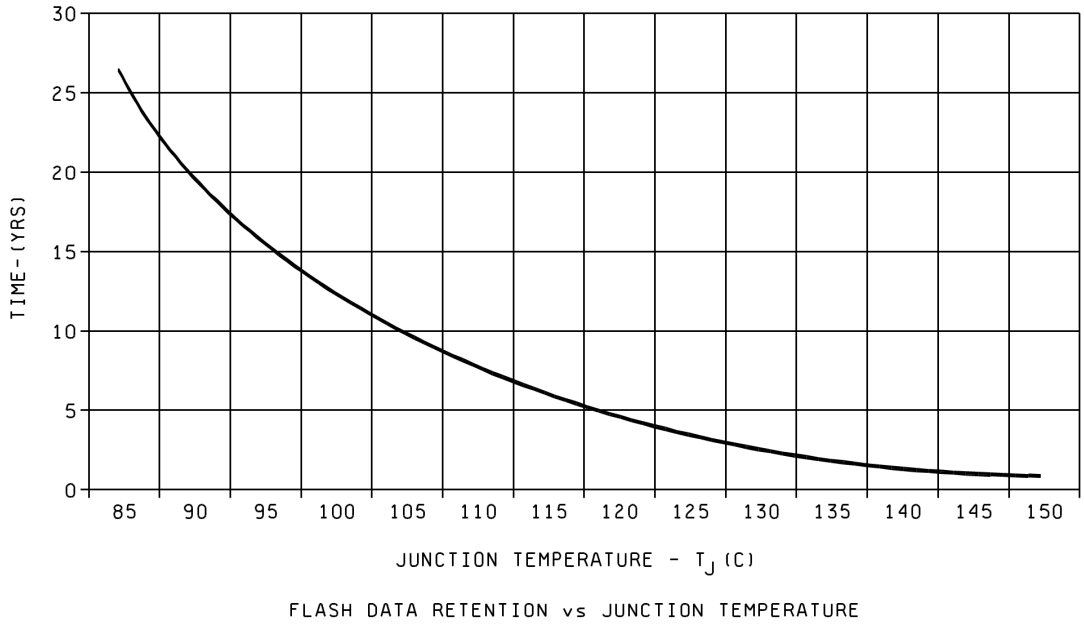


FIGURE 15. Test circuit and timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/08631-01XE	01295	MSP430F2274MRHATEP
V62/08631-01YE	01295	MSP430F2274MDATEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243