REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Make change to operating junction temperature under paragraph 1.3. Make correction to GND2 and IAIN2 terminal connection descriptions under figure 2. Update document paragraphs to current requirements. - ro	15-06-02	C. SAFFLE
B	Make correction to the Vendor part number. Update document paragraphs to current requirements. - ro	21-01-14	J. ESCHMEYER

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	**REV**			B	B	B	B	B	B	B	B	B	B	B	B	B	B			
	PAGE			1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 08-08-12	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** ROBERT M. HEBER	**TITLE** MICROCIRCUIT, LINEAR, SENSOR SIGNAL CONDITIONING DEVICE FOR CLOSED LOOP MAGNETIC CURRENT SENSOR, MONOLITHIC SILICON
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/08630**
	REV **B**	**PAGE** 1 **OF** 14

AMSC N/A

5962-V095-20

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance sensor signal conditioning device for closed loop magnetic current sensor microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/08630	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	DRV401-EP	Sensor signal conditioning device for closed loop magnetic current sensor

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	SO-20	Plastic surface mount with thermal pad

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{DD}) ..... +7 V maximum
Signal input terminals:
  Voltage ..... -0.5 V to V_{DD} + 0.5 V 2/
  Differential amplifier ..... -10 V to +10 V 3/
  Current at IS1 and IS2 ..... ±75 mA maximum
  Current (pins other than IS1 and IS2) ..... ±25 mA maximum 2/
I_{COMP} short circuit ..... +250 mA 4/
Operating junction temperature range (T_J) ..... -55°C to +150°C
Storage temperature range (T_{STG}) ..... -55°C to +150°C
Electrostatic discharge rating:
  Human body model (HBM) :
    Pins IA_{IN1} and IA_{IN2} only ..... 1 kV
    All other pins ..... 4 kV
Power dissipation (P_D) ..... 231 mW
Thermal resistance, junction to case (θ_{JC}) ..... 0.37°C/W
Thermal resistance, junction to ambient (θ_{JA}) ..... 27°C/W

1.4 Recommended operating conditions. 5/

Operating free-air temperature range (T_A) ..... -55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Input terminals are diode clamped to the power supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be limited, except for the differential amplifier input pins.
3/ These inputs are not internally protected against over voltage. The differential amplifier input pins must be limited to 5 mA, maximum or ±10 V, maximum.
4/ Power limited; observe maximum junction temperature.
5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Test circuit. The test circuit shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Differential amplifier		R_L = 10 kΩ to 2.5 V, V_{REFIN} = 2.5 V					
Offset voltage section							
Offset voltage, RTO 3/	V_{OS}	Gain 4 V/V	+25°C	01		±0.1	mV
Offset voltage drift, RTO 3/	dVOS / dT		-55°C to +125°C	01	±0.1 typical		µV / °C
Offset voltage, RTO 3/	V_{OS}	Gain 4 V/V	-55°C to +125°C	01		±0.17	mV
CMRR versus common mode, RTO	CMRR	-1 V to +6 V, V_{REF} = 2.5 V	+25°C	01		±280	µV / V
PSRR versus power supply, RTO	PSRR	V_{REF} not included	+25°C	01		±50	µV / V
Signal input section							
Common mode voltage range	V_{CM}		+25°C	01	-1	V_{DD} + 1	V
Signal output section							
Signal over range indication (over range), delay		V_{IN} = 1 V step 4/	-55°C to +125°C	01	2.5 to 3.5 typical		µs
Voltage output swing from negative rail, over range trip level		I = +2.5 mA, CMP trip level	+25°C	01		+85	mV
Voltage output swing from positive rail, over range trip level		I = -2.5 mA, CMP trip level	+25°C	01	V_{DD} - 85		mV
Short circuit current	I_{SC}	V_{OUT} connected to GND	+25°C	01	-18 typical		mA
		V_{OUT} connected to V_{DD}			+20 typical		
Gain, V_{OUT} / $V_{IN\ DIFF}$			-55°C to +125°C	01	4 typical		V/V
Gain error			+25°C	01		±0.3	%
Gain error drift			-55°C to +125°C	01	±0.1 typical		ppm/°C
Linearity error		R_L = 1 kΩ	+25°C	01	10 typical		ppm

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Frequency response section							
Bandwidth	BW	-3 dB	+25°C	01	2 typical		MHz
Slew rate	SR	CMVR = -1 V to +4 V	+25°C	01	6.5 typical		V / μs
Settling time, large signal		dV ± 2 V to 1 %, no external filter	+25°C	01	0.9 typical		μs
Settling time		dV ± 0.4 V to 0.01 %	+25°C	01	14 typical		μs
Input resistance section							
Differential			+25°C	01	16.5	23.5	kΩ
Common mode			+25°C	01	41	59	kΩ
External reference input			+25°C	01	41	59	kΩ
Noise section							
Output voltage noise density, RTO		Compensation loop disabled, f = 1 kHz	+25°C	01	170 typical		nV / $\sqrt{Hz}$
Compensation loop section							
DC stability		Probe f = 250 kHz, R_{LOAD} = 20 Ω					
Offset error 5/		Deviation from 50% PWM, Pin gain = L	+25°C	01	0.03 typical		%
Offset error drift 5/		Deviation from 50% PWM, Pin gain = L	-55°C to +125°C	01	7.5 typical		ppm/°C
Gain, pin gain = L		| V_{ICOMP1} | - | V_{ICOMP2} |	+25°C	01	-200	200	ppm / V
Power supply rejection ratio	PSRR	Probe loop f = 250 kHz	+25°C	01	500 typical		ppm / V
Frequency response section							
Open loop gain, two modes, 7.8 kHz		Pin gain H/L	+25°C	01	24 typical	32 typical	dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Probe coil loop section							
Input voltage clamp range		Field probe current < 50 mA	+25°C	01	-0.7		V
Internal resistor, IS1 or IS2 to V_{DD1}			+25°C	01	47	71	Ω
Internal resistor, IS1 or IS2 to GND	R_{HIGH}		+25°C	01	60	90	Ω
Resistance mismatch between IS1 and IS2	R_{LOW}	ppm of R_{HIGH} + R_{LOW}	+25°C	01		1500	ppm
Total input resistance		6/	-55°C to +125°C	01		200	Ω
Comparator threshold current		6/	+25°C	01	22	34	mA
Minimum probe loop half cycle			+25°C	01	250	310	ns
Probe loop minimum frequency			+25°C	01	250		kHz
No oscillation detect (error) suppression			+25°C	01	35 typical		μs
Compensation coil driver section, H bridge section							
Peak current		V_{ICOMP1} – V_{ICOMP2} = 4.0 V_{PP}	-55°C to +125°C	01	250 typical		mA
Voltage swing		20 Ω load	+25°C	01	4.2		V_{PP}
Output common mode voltage			+25°C	01	V_{DD2}/2 typical		V
Wire break detect, threshold current		I_{COMP1} and I_{COMP2} railed	+25°C	01		57	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Voltage reference section							
Voltage		No load	+25°C	01	2.495	2.505	V
Drift		No load	-55°C to +125°C	01	±5 typical		ppm/°C
Drift		No load	-55°C to +125°C	01	2.491	2.509	V
Power supply rejection ratio	PSRR		+25°C	01		±200	µV/V
Load regulation		Load to GND / V_{DD}, dI = 0 mA to 5 mA	+25°C	01	0.15 typical		mV/mA
Short circuit current	I_{SC}	REF_{OUT} connected to V_{DD}	+25°C	01	+20 typical		mA
		REF_{OUT} connected to GND			-18 typical		
Demagnetization section							
Duration		6/	-55°C to +125°C	01		130	ms
Digital input/output section							
Logic inputs, DEMAG, GAIN, and CCdiag pins section, CMOS type levels							
Pull up high current (CCdiag)		3.5 V < V_{IN} < V_{DD}	+25°C	01	160 typical		µA
Pull up low current (CCdiag)		0 V < V_{IN} < 1.5 V	+25°C	01	5 typical		µA
Logic input leakage current		0 V < V_{IN} < V_{DD}	-55°C to +125°C	01		5	µA
Logic level, input: L/H			+25°C	01	2.1 typical	2.8 typical	V
Hysteresis			+25°C	01	0.7 typical		V
Outputs section		(ERROR and OVER RANGE pins)					
Logic level, output: low		4 mA sink	+25°C	01	0.3 typical		V
Logic level, output: high			+25°C	01	No internal pull up		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Outputs section		(PWM and $\overline{PWM}$ pins)	Push pull type				
Logic level : low		4 mA sink	+25°C	01	0.2 typical		V
Logic level : high		4 mA source	+25°C	01	V_{DD} – 0.4 typical		V
Power supply section							
Specified voltage range	V_{DD}		-55°C to +125°C	01	4.5	5.5	V
Power on reset threshold	V_{RST}		+25°C	01	1.8 typical		V
Quiescent current [|(V_{DD1})|+ (V_{DD2})]	I_Q	I_{COMP} = 0 mA, sensor not connected	+25°C	01		6.8	mA
Brownout voltage level			+25°C	01	5 typical		V
Brownout indication delay			+25°C	01	135 typical		µs
Temperature range section							
Specified range	T_J			01	-40	+125	°C
Operating range	T_J			01	-50	+150	°C
Package thermal resistance	θ_{JA}		+25°C	01	27 typical		°C/W

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{DD1} and V_{DD2} = +5 with external 100 kHz filter bandwidth, and zero output current I_{COMP}.

3/ Parameter value referred to output (RTO).

4/ Total input resistance and comparator threshold current are inversely related.

5/ For VAC sensors, 0.2 % of pulse width modulator (PWM) offset approximately corresponds to 10 mA primary current offset per winding.

6/ Total input resistance and comparator threshold current are inversely related. See figure 3.

Case X

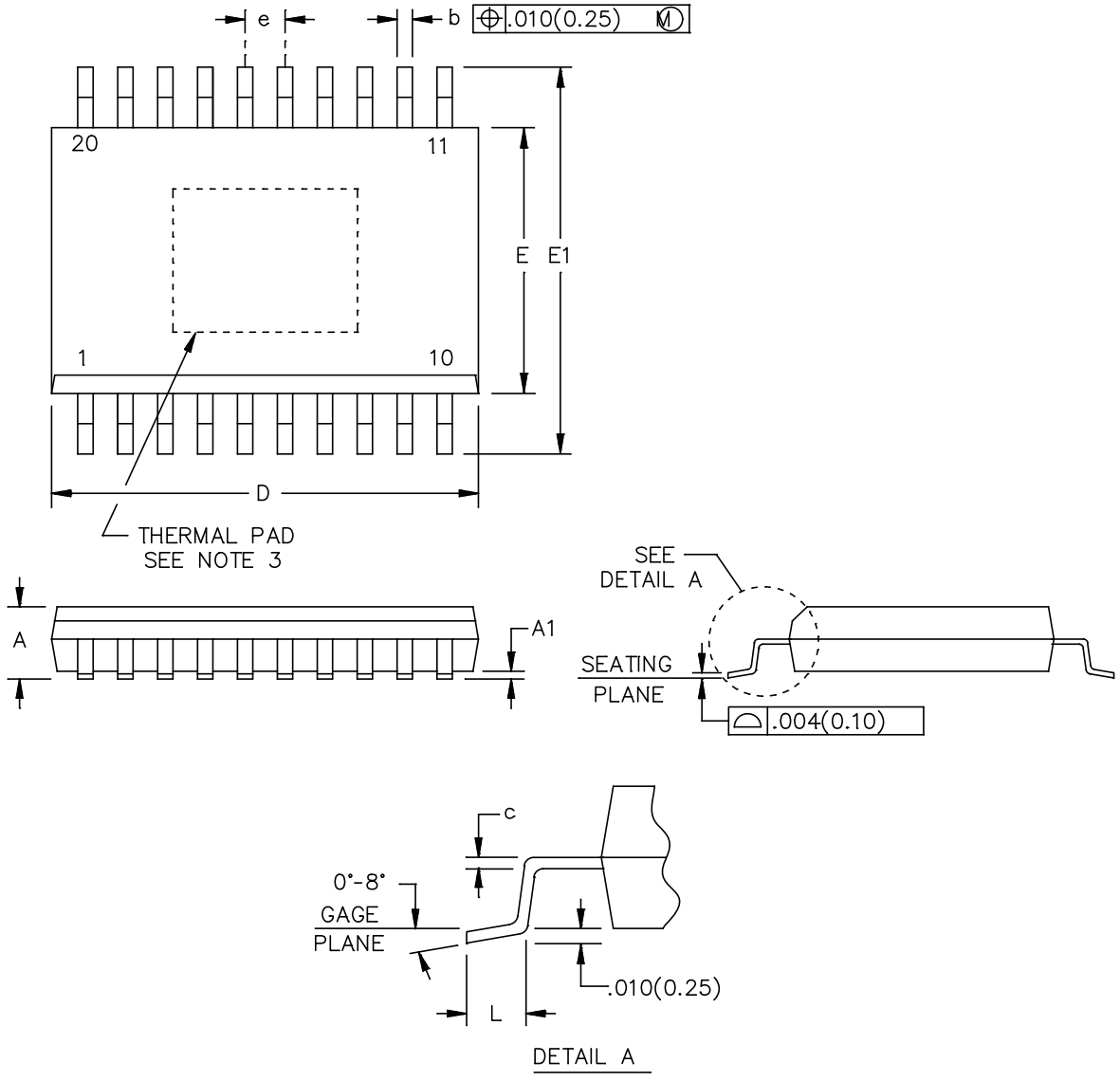


FIGURE 1. Case outline.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/08630
		REV B	PAGE 10

Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.104	---	2.65
A1	0.002	0.006	0.05	0.15
b	0.014	0.020	0.35	0.51
c	0.010 NOM		0.25 NOM	
D	0.500	0.510	12.70	12.95
e	0.050 BSC		1.27 BSC	
E	0.293	0.299	7.45	7.59
E1	0.400	0.419	10.16	10.65
L	0.016	0.050	0.40	1.27

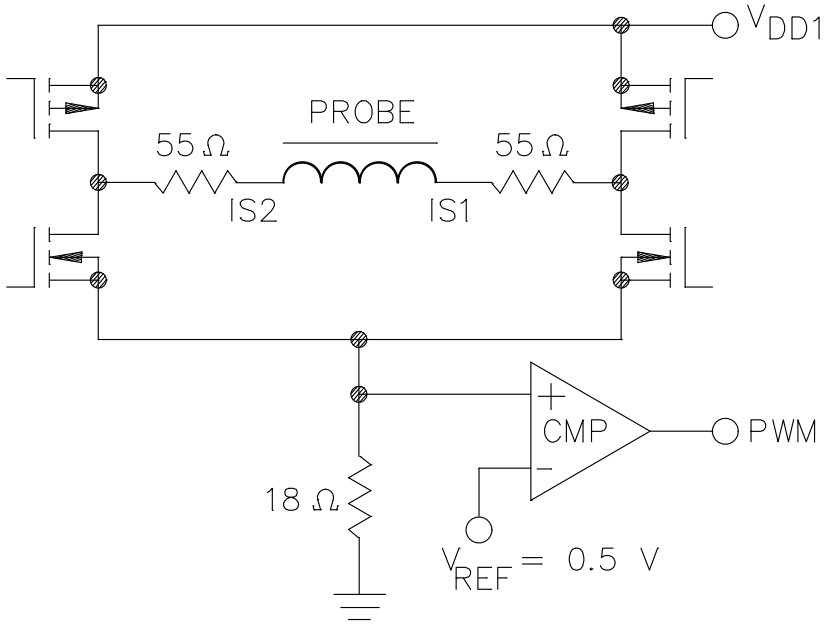
NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.006 inch (0.15 mm).
3. This package is designed to be soldered to a thermal pad on the board. Refer to technical brief, powerpad thermally enhanced package, manufacturer's literature number SLMA002 for information regarding recommended board layout. This document is available from the manufacturer. See the product data sheet for details regarding the exposed thermal pad dimensions.
4. Falls within reference to JEDEC SO-20.

FIGURE 1. Case outline – continued.

Device type	01	
Case outline	X (See note)	
Terminal number	Terminal symbol	Description
1	$\overline{PWM}$	Pulse width modulator (PWM) output from probe circuit (inverted).
2	PWM	PWM output from probe circuit.
3	ERROR	Error flag: open drain output.
4	DEMAG	Control input.
5	GAIN	Control input for open loop gain: low = normal, high = -8 dB.
6	REF_{OUT}	Output for internal 2.5 V reference voltage.
7	REF_{IN}	Input for zero reference to differential amplifier.
8	V_{OUT}	Output for differential amplifier.
9	IA_{IN2}	Noninverting input of differential amplifier. Connect to GND1.
10	IA_{IN1}	Inverting input of differential amplifier.
11	GND2	Ground connection.
12	I_{COMP2}	Output 2 of compensation coli driver.
13	I_{COMP1}	Output 1 of compensation coli driver.
14	V_{DD2}	Supply voltage. Connect to V_{DD1}.
15	CCdiag	Control input for wire break detection: high = enable
16	OVER RANGE	Open drain output for over range indication: low = over range.
17	V_{DD1}	Supply voltage.
18	IS2	Probe connection 2.
19	GND1	Ground connection.
20	IS1	Probe connection 1.

NOTE: Exposed thermal pad on underside, connect to GND1.

FIGURE 2. Terminal connections.



NOTES:

1. This is a simplified probe interface circuit. The probe is connected between S1 and S2.
2. MOS components function as switches only.

FIGURE 3. Test circuit.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/ 2/ 3/	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/08630-01XE	01295	DRV401M	DRV401AMDWPREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet.

3/ Package drawings, standard packaging quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available from the manufacturer.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243