REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. Update boilerplate paragraphs to current requirements. - PHN	13-05-28	Thomas M. Hess
B	Update boilerplate paragraphs to current VID description requirements. - DRH	22-09-26	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B		
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		

PMIC N/A

Original date of drawing

08-10-21

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DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
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TITLE
MICROCIRCUIT, DIGITAL, QUAD CHANNEL, 14 BIT, 125 MSPS ADC WITH SERIAL LVDS OUTPUT, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/08628
REV B		PAGE 1 OF 20

AMSC N/A

5962-V115-22

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance quad channel, 14 bit, 125 MSPS ADC with serial LVDS outputs microcircuit for device type 01 and a quad channel, 14 bit, 105 MSPS ADC with serial LVDS outputs microcircuit for device type 02, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/08628	-	01	X	A
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADS6445-EP	Quad channel, 14 bit, 125 MSPS ADC with serial LVDS outputs
02	ADS6444-EP	Quad channel, 14 bit, 105 MSPS ADC with serial LVDS outputs

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	Package style
X	64	Plastic quad flatpack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range:
- ADVDD ..... -0.3 V to 3.9 V
- LVDD ..... -0.3 V to 3.9 V

Voltage between AGND and DGND ..... -0.3 V to 0.3 V
Voltage between AVDD to LVDD ..... -0.3 V to 3.3 V
Voltage applied to external pin, VCM ..... -0.3 V to 2.0 V
Voltage applied to analog input pins .....-0.3 V to minimum (3.6, AVDD + 0.3) V
Operating junction temperature range, T_J ..... 150°C
Storage temperature range, T_{STG} ..... -65°C to 150°C
Lead temperature 1.6 mm (1/16") from the case for 10 seconds ..... 220°C

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

1.4 Thermal characteristics.

Thermal metric 2/	Case outline X	Units
Junction to ambient thermal resistance, θ_{JA} 3/	23.6	°C/W
Junction to case (top) thermal resistance, θ_{JCtop} 4/	7.7	
Junction to board thermal resistance, θ_{JB} 5/	3	
Junction to top characterization parameter, Ψ_{JT} 6/	0.1	
Junction to board characterization parameter, Ψ_{JB} 7/	3	
Junction to case (bottom) thermal resistance, θ_{JCbot} 8/	0.3	

1.5 Recommended operating conditions.

SUPPLIES
- Analog supply voltage, AVDD ..... 3.0 V to 3.6 V
- LVDS buffer supply voltage, LVDD ..... 3.0 V to 3.6 V

ANALOG INPUTS
- Differential input voltage range ..... 2.0 V_{P-P} Typical
- Input common-mode voltage ..... 1.5 V ±0.1 Typical
- Voltage applied on VCM in external reference mode ..... 1.45 V to 1.55 V

CLOCK INPUTS
- Input clock sample rate, F_{srated}:
  - Device type 01 .....5 to 125 MSPS
  - Device type 02 .....5 to 105 MSPS
- Input clock amplitude differential ($V_{CLKP} – V_{CLKM}$):
  - Minimum sine wave, ac coupled ..... 0.4 V_{P-P}
  - LVPECL, ac coupled ..... ±0.8 V_{P-P} Typical
  - LVDS, ac coupled ..... ±0.35 V_{P-P} Typical
  - LVCMOS, ac coupled ..... 3.3 V_{P-P} Typical
- Input clock duty cycle ..... 35% to 65%

DIGITAL INPUTS
- Maximum external load capacitance from each output pin to DGND, C_{LOAD}:
  - Without internal termination ..... 5 pF Typical
  - With internal termination ..... 10 pF Typical
- Differential load resistance (external) between the LVDS output pairs, R_{LOAD} ..... 100 Ω Typical

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2/ For more information about traditional and new thermal metrics, see manufacturer data.
3/ The junction to ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K-board, as specified in JESD51-7, in an environment described in JESD51-2a.
4/ The junction to case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specified JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
5/ The junction to board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
6/ The junction to top characterization parameter, Ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
7/ The junction to board characterization parameter, Ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
8/ The junction to case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specified JEDEC- standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

2. APPLICABLE DOCUMENTS

SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP 95	–	Registered and Standard Outlines for Semiconductor Devices
JESD 51	–	Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device).
JESD 51-2a	–	Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
JESD 51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JESD 51-8	–	Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-board

(Copies of these documents are available online at https://www.jedec.org.)

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI) STANDARD

ANSI SEMI STANDARD G30-88	–	Test Method for Junction-to-Case Thermal Resistance Measurements for Ceramic Packages

(Copies of these documents are available online at https://www.ansi.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal description. The terminal description shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

3.5.5 Latency. The latency shall be as shown in figure 5.

3.5.6 LVDS timing. The LVDS timing shall be as shown in figure 6.

3.5.7 Reset timing. The Reset timing shall be as shown in figure 7.

3.5.8 Serial interface timing. The serial interface timing shall be as shown in figure 8.

TABLE I. Electrical performance characteristics. 1/ 2/

Test	Symbol	Device type 01 F_s = 125 MSPS			Device type 02 F_s = 105 MSPS			Unit
		Min	TYP	Max	Min	TYP	Max	
Resolution			14			14		Bits
Analog input								
Differential input voltage range			2.0			2.0		V_{PP}
Differential input capacitance			7			7		pF
Analog input bandwidth			500			500		MHz
Analog input common mode current (per input pin of each ADC)			155			130		µA
Reference voltages								
Internal reference bottom voltage	VREFB		1.0			1.0		V
Internal reference top voltage	VREFT		2.0			2.0		V
Internal reference error (VREFT-VREFB)	ΔV_{REF}	0.985	1	1.015	0.985	1	1.015	V
Common mode output voltage	VCM		1.5			1.5		V
VCM output current capability			±4			±4		mA
DC accuracy								
No missing code			Assured			Assured		
Offset error, across devices and across channels within a device	E_O	-15	±2	15	-15	±2	15	mV
Offset error temperature coefficient, across devices and across channels within a device			0.05			0.05		mV/°C
There are two source of gain error – internal reference inaccuracy and channel gain error								
Gain error due to internal reference inaccuracy alone, (ΔV_{REF} /2.0)%	E_{GREF}	-0.75	0.1	0.75	-0.75	0.1	0.75	%FS
Reference gain error temperature coefficient			0.0125			0.0125		Δ%/°C
Gain error of channel alone, across devices and across channels within a device	E_{GCHAN}		±0.3			±0.3		%FS
Channel gain error temperature coefficient, across devices and across channels within a device			0.005			0.005		Δ%/°C
Differential nonlinearity, Fin = 50 MHz	DNL	-0.99	±0.6	2.0	-0.99	±0.6	2.0	LSB
Integral nonlinearity, Fin = 50 MHz	INL	-5	±3	5	-5	±3	5	LSB
DC power supply rejection ratio	PSRR		0.5			0.5		mV/V
Power supply								
Total supply current	I_{CC}		502			410		mA
Analog supply current	I_{AVDD}		410			322		mA
LVDS supply current	I_{LVDD}		92			88		mA
Total power			1.65	1.8		1.35	1.5	W
Power down (within input clock stopped)			77	150		77	150	mW

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 2/ unless otherwise specified		Device type 01 F_s = 125 MSPS			Device type 02 F_s = 105 MSPS			Unit
				Min	TYP	Max	Min	TYP	Max	
Dynamic AC characteristics										
Signal to noise ratio	SNR	Fin = 10 MHz			73.7			73.8		dBFS
		Fin = 50 MHz		68.5	73.1			73.2		
		Fin = 70 MHz			72.7		69	73		
		Fin = 100 MHz			72.1			72.2		
		Fin = 170 MHz	0 dB gain		69.9			70.2		
			3.5 dB Coarse gain		69.4			69.7		
		Fin =230 MHz	0 dB gain		68.7			68.8		
			3.5 dB Coarse gain		68.1			68.2		
Signal to noise and distortion ratio	SINAD	Fin = 10 MHz			73.4			73.4		dBFS
		Fin = 50 MHz		67.75	72.3			71.7		
		Fin = 70 MHz			71.2		68.5	72		
		Fin = 100 MHz			71.8			72		
		Fin = 170 MHz	0 dB gain		67.9			69.8		
			3.5 dB Coarse gain		68.3			69.3		
		Fin =230 MHz	0 dB gain		67.8			67.7		
			3.5 dB Coarse gain		67.9			67.6		
Output noise	RMS	Inputs tied to common-mode			1.05			1.05		LSB
Spurious free dynamic range	SFDR	Fin = 10 MHz			87			91		dBc
		Fin = 50 MHz		69	81			80		
		Fin = 70 MHz			78		74	81		
		Fin = 100 MHz			86			88		
		Fin = 170 MHz	0 dB gain		76			79		
			3.5 dB Coarse gain		79			83		
		Fin =230 MHz	0 dB gain		77			77		
			3.5 dB Coarse gain		80			80		
Second harmonic	HD2	Fin = 10 MHz			93			94		dBc
		Fin = 50 MHz		69	87			88		
		Fin = 70 MHz			87		74	88		
		Fin = 100 MHz			89			90		
		Fin = 170 MHz	0 dB gain		83			84		
			3.5 dB Coarse gain		85			86		
		Fin =230 MHz	0 dB gain		80			81		
			3.5 dB Coarse gain		82			83		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 2/ unless otherwise specified		Device type 01 F_s = 125 MSPS			Device type 02 F_s = 105 MSPS			Unit
				Min	TYP	Max	Min	TYP	Max	
Dynamic AC characteristics - continued										
Third harmonic	HD3	Fin = 10 MHz			87			91		dBc
		Fin = 50 MHz		69	81			80		
		Fin = 70 MHz			78		74	81		
		Fin = 100 MHz			86			88		
		Fin = 170 MHz	0 dB gain		76			79		
			3.5 dB Coarse gain		79			83		
		Fin =230 MHz	0 dB gain		77			77		
			3.5 dB Coarse gain		80			80		
Worst harmonic (other than HD2, HD3)		Fin = 10 MHz			91			91		dBc
		Fin = 50 MHz			87			87		
		Fin = 100 MHz			90			91		
		Fin = 170 MHz			88			88		
		Fin = 230 MHz			87			87		
Total harmonic distortion	THD	Fin = 10 MHz			86			89.5		dBc
		Fin = 50 MHz		69	80			80		
		Fin = 100 MHz			84.5		72	79		
		Fin = 170 MHz			73.5			86		
		Fin = 230 MHz			74			77		
Effective number of bits	ENOB	Fin = 50 MHz		10.95	11.7					Bits
		Fin = 70 MHz					11.3	11.7		
2-Tone inter-modulation distortion	IMD	F1 = 46.09 MHz, F2 = 50.09 MHz			88			90		dBFS
		F1 = 185.09 MHz, F2 = 190.09 MHz			86			88		
Cross talk		Near channel Cross talk signal frequency = 10 MHz			90			92		dBc
		Far channel Cross talk signal frequency = 10 MHz			103			105		
Input overload recovery		Recovery to within 1% (of final value) for 6-dB overload with sine wave input			1			1		Clock cycles
Power supply rejection ratio	AC PSRR	< 100 MHz signal, 100 mV_{PP} on AVDD supply			35			35		dBc

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 3/ unless otherwise specified	Device type 01 F_s = 125 MSPS			Device type 02 F_s = 105 MSPS			Unit
			Min	TYP	Max	Min	TYP	Max	
Digital inputs									
High level input voltage			2.4			2.4			V
Low level input voltage					0.8			0.8	V
High level input current				10			10		µA
Low level input current				10			10		µA
Input capacitance				4			4		pF
Digital outputs									
High level output voltage				1375			1375		mV
Low level output voltage				1025			1025		mV
Output differential voltage	$\|V_{OD}\|$		250	350	450	250	350	450	mV
Output offset voltage	V_{OS}	Common mode voltage of OUTP and OUTM		1200			1200		mV
Output capacitance		Output capacitance inside the device, from either output to ground		2			2		pF
TIMING SPECIFICATIONS 5/ 6/									
Aperture jitter	t_J	Uncertainty in the sampling instant		250			250		fs ms
Interface: 2-wire, DDR bit clock, 14x serialization									
Data setup time 8/ 9/ 10/	t_{su}	From data cross over to bit clock cross over		0.55			0.65		ns
Data hold time 8/ 9/ 10/	t_h	From bit clock cross over to data cross over		0.58			0.7		ns
Clock propagation delay 10/	t_{pd_clk}	Input clock rising edge cross over to frame clock rising edge cross over		4.4			4.4		ns
Bit clock cycle-cycle jitter 9/				350			350		ps pp
Frame clock cycle-cycle jitter 9/				75			75		ps pp

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 3/ unless otherwise specified	Device type 01 F_s = 125 MSPS			Device type 02 F_s = 105 MSPS			Unit
			Min	TYP	Max	Min	TYP	Max	
The following specifications apply for 5 MSPS ≤ Fs ≤ 125 MSPS and all interface options									
Aperture delay	t_A	Delay from input clock rising edge to the actual sampling instant		2			2		ns
Aperture delay variation		Channel-channel within same device		±80			±80		ps
ADC latency 11/		Time for a sample to propagate to ADC outputs, See FIGURE 5		12			12		Clock cycles
Wake up time		Time to valid data after coming out of global power down		100			100		µs
		Time to valid data after input clocks is re-started		100			100		µs
		Time to valid data after coming out of channel standby		200			200		Clock cycles
Data rise time	t_{RISE}	From -100 mV to +100 mV		100			100		ps
Data fall time	t_{FALL}	From +100 mV to -100 mV		100			100		
Bit clock and frame clock rise time	t_{RISE}	From -100 mV to +100 mV		100			100		
Bit clock and frame clock fall time	t_{FALL}	From +100 mV to -100 mV		100			100		
LVDS bit clock duty cycle				50%			50%		
LVDS frame clock duty cycle				50%			50%		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 12/ unless otherwise specified	Device type	Limits			Unit
				Min	TYP	Max	
SERIAL INTERFACE TIMING CHARACTERISTICS							
SCLK frequency, $f_{SCLK} = 1/t_{SCLK}$	f_{SCLK}		All	>DC		20	MHz
SEN to SCLK setup time	t_{SLOADS}				25		ns
SCLK to SEN hold time	t_{SLOADH}				25		
SDATA setup time	t_{DSU}				25		
SDATA hold time	t_{DH}				25		
Time taken for register write to take effect after 16th SCLK falling edge					100		
RESET TIMING							
Power on delay time	t_1	Delay from power-up of AVDD and LVDD to RESET pulse active	All		5		ms
Reset pulse width	t_2	Pulse width of active RESET signal			10		ns
Register writer delay time	t_3	Delay from RESET disable to SEN active			25		ns
Power up delay time	t_{PO}	Delay from power-up of AVDD and LVDD to output stable			6.5		ms

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Typical values are at 25°C, min and max values are across the full junction temperature range $T_{J,MIN}$ = -55°C to $T_{J,MAX}$ = 125°C, AVDD = LVDD = 3.3 V, maximum rated sampling frequency, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode (unless otherwise noted).

3/ The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1 AVDD = LVDD = 3.3 V, I_O = 3.5 mA, RLOAD = 100 Ω 4/. All LVDS specifications are characterized, but not tested at production.

4/ I_O refers to the LVDS buffer current setting; R_L is the external differential load resistance between the LVDS output pair.

5/ Timing parameters are ensured by design and characterization and not tested in production.

6/ Typical values are at 25°C, min and max values are across the full junction temperature range $T_{J,MIN}$ = -55°C to $T_{J,MAX}$ = 125°C, AVDD = LVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 Vpp clock amplitude, C_L = 5 pF 7/, I_O = 3.5 mA, R_L = 100 Ω 4/, no internal termination, unless otherwise noted.

7/ C_L is the external single ended load capacitance between each output pin and ground.

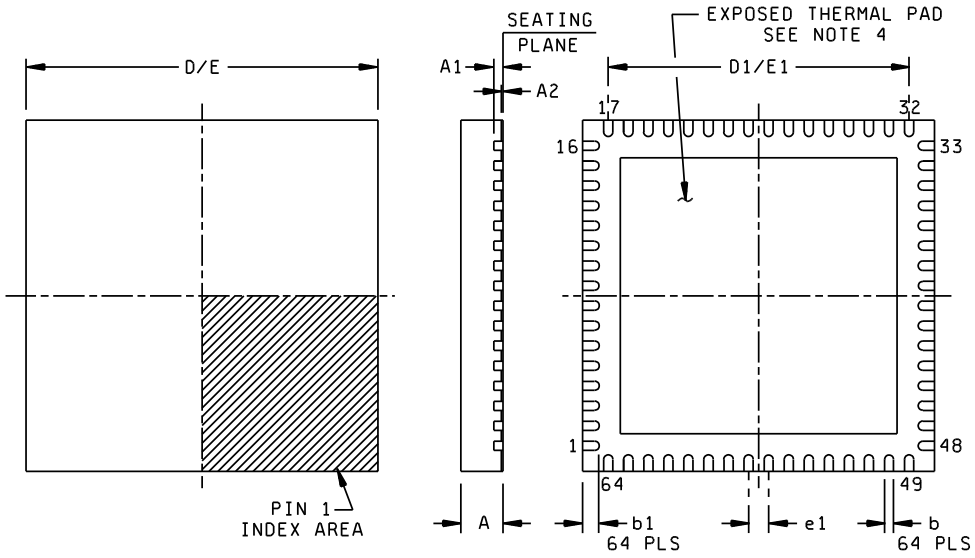
8/ Timing parameters are measured at the end of a 2 inch PCB trace (100 Ω characteristic impedance) terminated by R_L and C_L.

9/ Setup and hold time specifications take into account the effect of jitter on the output data and clock.

10/ Refer to output timing application section in manufacturer data for timing at lower sampling frequencies and other interface options.

11/ Note that the total latency = ADC latency + internal serialized latency. The serialized latency depends on the interface option selected as in manufacturer data.

12/ Typical values are at 25°C, min and max values are across the full junction temperature range $T_{J,MIN}$ = -55°C to $T_{J,MAX}$ = 125°C, AVDD = LVDD = 3.3 V, unless otherwise noted.



Dimension					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.80	1.00	b1	0.30	0.50
A1	0.20 REF		D/E	8.85	9.15
A2	0.00	0.05	D1/E1	7.50 REF	
b	0.18	0.30	e1	0.50 BSC	

NOTES:
1. All linear dimensions are in millimeters. Dimensioning and tolerance per ASME Y14.5 – 1994.
2. This drawing is subject to change without notice.
3. Quad flatpack, No-leads (QFN) package configuration.
4. The package thermal pad must be soldered to the board for thermal and mechanical performance. See manufacturer data for details regarding the exposed thermal pad dimensions.

FIGURE 1. Case outline.

Case X (2-Wire interface)

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DA1_P	17	AVDD	33	AGND	49	LVDD
2	DA1_M	18	AGND	34	INC_P	50	DC1_P
3	DA0_P	19	AVDD	35	INC_M	51	DC1_M
4	DA0_M	20	NC	36	AGND	52	DC0_P
5	CAP	21	CFG4	37	IND_P	53	DC0_M
6	RESET	22	VCM	38	IND_M	54	LGND
7	LVDD	23	AGND	39	AGND	55	FCLKP
8	AGND	24	CLKP	40	AVDD	56	FCLKM
9	AVDD	25	CLKM	41	PDN	57	DCLKP
10	AGND	26	AGND	42	SEN	58	DCLKM
11	INA_M	27	AVDD	43	SDATA	59	LGND
12	INA_P	28	CFG3	44	SCLK	60	DB1_P
13	AGND	29	CFG2	45	DD1_P	61	DB1_M
14	INB_M	30	CFG1	46	DD1_M	62	DB0_P
15	INB_P	31	AGND	47	DD0_P	63	DB0_M
16	AGND	32	AVDD	48	DD0_M	64	LVDD

Case X (1-Wire interface)

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	UNUSED	17	AVDD	33	AGND	49	LVDD
2	UNUSED	18	AGND	34	INC_P	50	DD_P
3	UNUSED	19	AVDD	35	INC_M	51	DD_M
4	UNUSED	20	NC	36	AGND	52	DC_P
5	CAP	21	CFG4	37	IND_P	53	DC_M
6	RESET	22	VCM	38	IND_M	54	LGND
7	LVDD	23	AGND	39	AGND	55	FCLKP
8	AGND	24	CLKP	40	AVDD	56	FCLKM
9	AVDD	25	CLKM	41	PDN	57	DCLKP
10	AGND	26	AGND	42	SEN	58	DCLKM
11	INA_M	27	AVDD	43	SDATA	59	LGND
12	INA_P	28	CFG3	44	SCLK	60	DB_P
13	AGND	29	CFG2	45	UNUSED	61	DB_M
14	INB_M	30	CFG1	46	UNUSED	62	DA_P
15	INB_P	31	AGND	47	UNUSED	63	DA_M
16	AGND	32	AVDD	48	UNUSED	64	LVDD

FIGURE 2. Terminal connections.

Pin Assignments (2-Wire interface)

Terminal		I/O	No. of pins	Description
Name	Number			
Supply and ground Pins				
AVDD	9, 17, 19, 27, 32, 40		6	Analog power supply
AGND	8,10, 13 16, 18, 23 26, 31, 33 36, 39		11	Analog ground
LVDD	7, 49, 64		3	Digital power supply
LGND	54, 59		2	Digital ground
Input pins				
CLKP, CLKM	24, 25	I	2	Differential input clock pair
INA_P, INA_M	12, 11	I	2	Differential input signal pair, channel A. If unused, the pins should be tied to VCM. Do not float
INB_P, INB_M	15, 14	I	2	Differential input signal pair, channel B. If unused, the pins should be tied to VCM. Do not float
INC_P, INC_M	34, 35	I	2	Differential input signal pair, channel C. If unused, the pins should be tied to VCM. Do not float
IND_P, IND_M	37, 38	I	2	Differential input signal pair, channel D. If unused, the pins should be tied to VCM. Do not float
CAP	5	I	1	Connect 2-nF capacitor from pin to ground
SCLK	44	I	1	This pin functions as serial interface clock input when RESET is low. When RESET is ***high***, it controls DESKEW, SYNC and global POWER DOWN modes (along with SDATA). Refer to manufacturer data for description. This pin has an internal pull-down resistor
SDATA	43	I	1	This pin functions as serial interface data input when RESET is low. When RESET is ***high***, it controls DESKEW, SYNC and global POWER DOWN modes (along with SCLK). Refer to manufacturer data for description. This pin has an internal pull-down resistor.
SEN	42	I	1	This pin functions as serial interface enable input when RESET is low. When RESET is ***high***, it controls coarse gain and internal/external reference modes. Refer to manufacturer data for description. This pin has an internal pull-up resistor.
RESET	6	I	1	Serial interface reset input. When using the serial interface mode, the user MUST initialize internal registers through hardware RESET by applying a high-going pulse on this pin or by using software reset option. Refer to the Serial Interface section in manufacturer data. In parallel interface mode, tie RESET permanently ***high***. (SCLK, SDATA and SEN function as parallel control pins in this mode). The pin has an internal pull-down resistor to ground.
PDN	41	I	1	Global power down control pin.
CFG1	30	I	1	Parallel input pin. It controls 1-wire or 2-wire interface and DDR or SDR bit clock selection. Refer to manufacturer data for description. Tie to AVDD for 2-wire interface with DDR bit clock.

FIGURE 3. Terminal description (2 wire interface).

Pin Assignments (2-Wire interface) – Continued.

Terminal		I/O	No. of pins	Description
Name	Number			
Input pins- Continued				
CFG2	29	I	1	Parallel input pin. It controls 14x or 16x serialization and SDR bit clock capture edge. Refer to manufacturer data for description. For 14x serialization with DDR bit clock, tie to ground or AVDD.
CFG3	28	I	1	RESERVED pin - Tie to ground.
CFG4	21	I	1	Parallel input pin. It controls data format and MSB or LSB first modes. Refer to manufacturer data for description
VCM	22	I/O	1	Internal reference mode – common-mode voltage output. External reference mode – reference input. The voltage forced on this pin sets the internal reference.
Output pins				
DA0_P, DA0_M	3, 4	O	2	Channel A differential LVDS data output pair, wire 0
DA1_P, DA1_M	1, 2	O	2	Channel A differential LVDS data output pair, wire 1
DB0_P, DB0_M	62, 63	O	2	Channel B differential LVDS data output pair, wire 0
DB1_P, DB1_M	60, 61	O	2	Channel B differential LVDS data output pair, wire 1
DC0_P, DC0_M	52, 53	O	2	Channel C differential LVDS data output pair, wire 0
DC1_P, DC1_M	50, 51	O	2	Channel C differential LVDS data output pair, wire 1
DD0_P, DD0_M	47, 48	O	2	Channel D differential LVDS data output pair, wire 0
DD1_P, DD1_M	45, 46	O	2	Channel D differential LVDS data output pair, wire 1
DCLKP, DCLKM	57, 58	O	2	Differential bit clock output pair
FCLKP, FCLKM	55, 56	O	2	Differential frame clock output pair
NC	20		1	Do Not Connect
PAD	0		1	Connect to ground plane using multiple vias. Refer to Board Design consideration in manufacturer data section.

FIGURE 3. Terminal description (2 wire interface) - Continued.

Pin Assignments (1-Wire interface)

Terminal		I/O	No. of pins	Description
Name	Number			
Supply and ground Pins				
AVDD	9, 17, 19, 27, 32, 40		6	Analog power supply
AGND	8,10, 13 16, 18, 23 26, 31, 33 36, 39		11	Analog ground
LVDD	7, 49, 64		3	Digital power supply
LGND	54, 59		2	Digital ground
Input pins				
CLKP, CLKM	24, 25	I	2	Differential input clock pair
INA_P, INA_M	12, 11	I	2	Differential input signal pair, channel A. If unused, the pins should be tied to VCM. Do not float
INB_P, INB_M	15, 14	I	2	Differential input signal pair, channel B. If unused, the pins should be tied to VCM. Do not float
INC_P, INC_M	34, 35	I	2	Differential input signal pair, channel C. If unused, the pins should be tied to VCM. Do not float
IND_P, IND_M	37, 38	I	2	Differential input signal pair, channel D. If unused, the pins should be tied to VCM. Do not float
CAP	5	I	1	Connect 2-nF capacitor from pin to ground
SCLK	44	I	1	This pin functions as serial interface clock input when RESET is low. When RESET is ***high***, it controls DESKEW, SYNC and global POWER DOWN modes (along with SDATA). Refer to manufacturer data for description. This pin has an internal pull-down resistor
SDATA	43	I	1	This pin functions as serial interface data input when RESET is low. When RESET is ***high***, it controls DESKEW, SYNC and global POWER DOWN modes (along with SCLK). Refer to manufacturer data for description. This pin has an internal pull-down resistor
SEN	42	I	1	This pin functions as serial interface enable input when RESET is low. When RESET is ***high***, it controls coarse gain and internal/external reference modes. Refer to manufacturer data for description. This pin has an internal pull-up resistor.
RESET	6	I	1	Serial interface reset input. When using the serial interface mode, the user MUST initialize internal registers through hardware RESET by applying a high-going pulse on this pin or by using software reset option. Refer to the Serial Interface section in manufacturer data. In parallel interface mode, tie RESET permanently ***high***. (SCLK, SDATA and SEN function as parallel control pins in this mode). The pin has an internal pull-down resistor to ground.
PDN	41	I	1	Global power down control pin.
CFG1	30	I	1	Parallel input pin. It controls 1-wire or 2-wire interface and DDR or SDR bit clock selection. Refer to manufacturer data for description. Tie to AVDD for 2-wire interface with DDR bit clock.

FIGURE 3. Terminal description (1 wire interface) - Continued.

Pin Assignments (1-Wire interface) – Continued.

Terminal		I/O	No. of pins	Description
Name	Number			
Input pins- Continued				
CFG2	29	I	1	Parallel input pin. It controls 14x or 16x serialization and SDR bit clock capture edge. Refer to manufacturer data for description. For 14x serialization with DDR bit clock, tie to ground or AVDD.
CFG3	28	I	1	RESERVED pin - Tie to ground.
CFG4	21	I	1	Parallel input pin. It controls data format and MSB or LSB first modes. Refer to manufacturer data for description
VCM	22	I/O	1	Internal reference mode – common-mode voltage output. External reference mode – reference input. The voltage forced on this pin sets the internal reference.
Output pins				
DA_P, DA_M	62, 63	O	2	Channel A differential LVDS data output pair.
DB_P, DB_M	60, 61	O	2	Channel B differential LVDS data output pair.
DC_P, DC_M	52, 53	O	2	Channel C differential LVDS data output pair.
DD_P, DD_M	50, 51	O	2	Channel D differential LVDS data output pair.
DCLKP, DCLKM	57, 58	O	2	Differential bit clock output pair
FCLKP, FCLKM	55, 56	O	2	Differential frame clock output pair
UNSUSED	1-4, 45-48			These pins are unused in the 1-wire interface. Do not connect
NC	20		1	Do Not Connect
PAD	0		1	Connect to ground plane using multiple vias. Refer to Board Design consideration in manufacturer data section.

FIGURE 3. Terminal description (1 wire interface) - Continued.

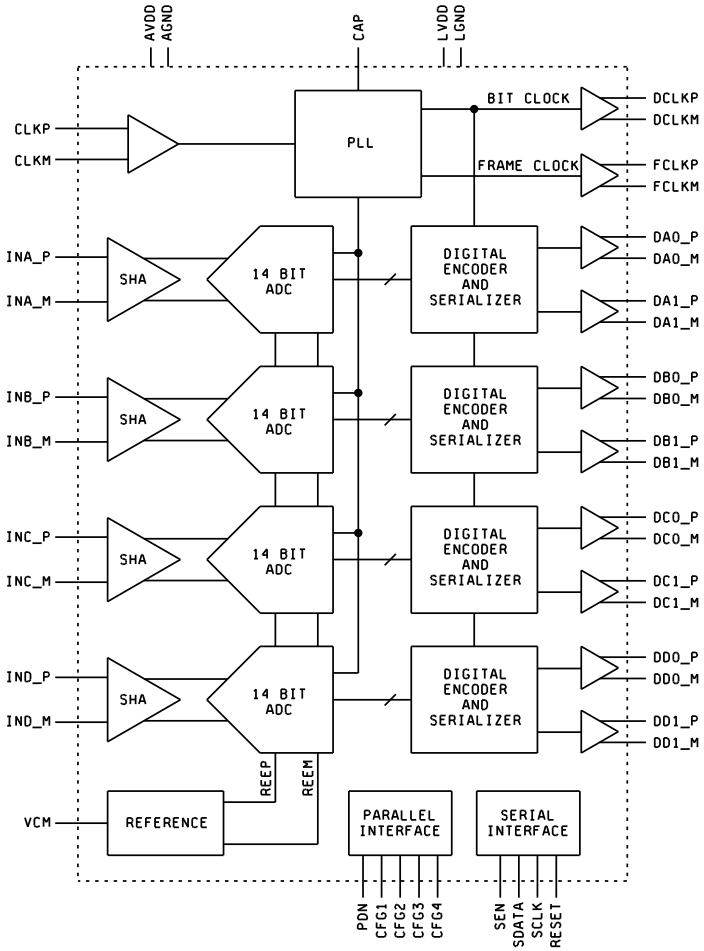


FIGURE 4. Functional block diagram.

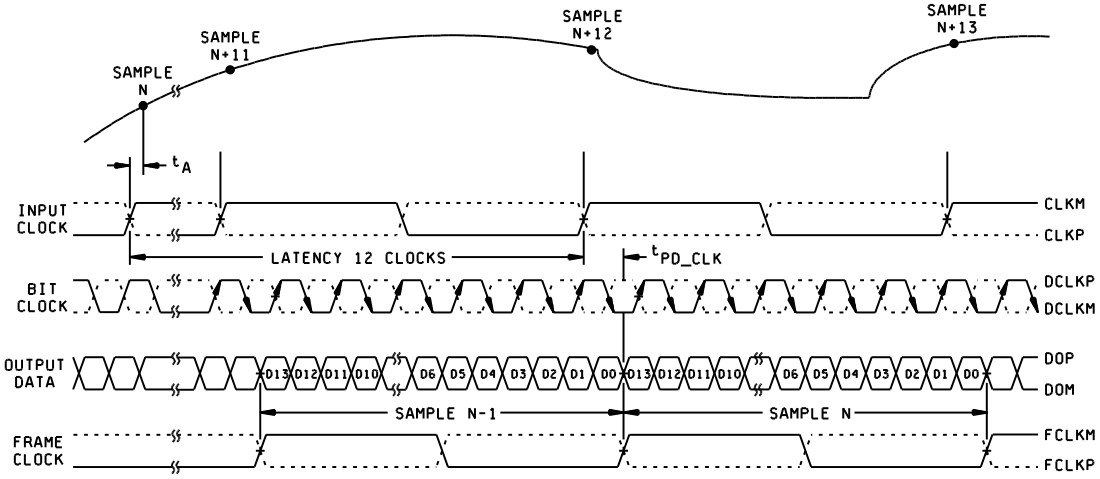


FIGURE 5. Latency.

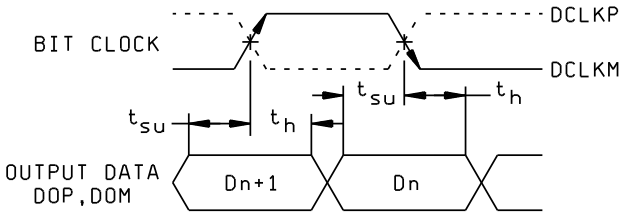


FIGURE 6. LVDS timing.

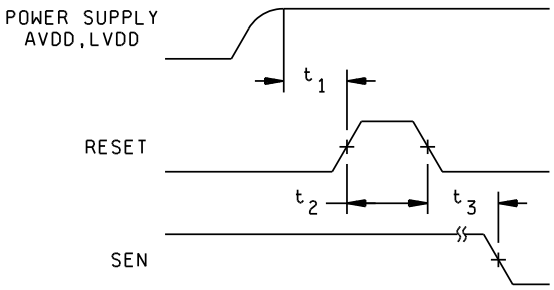


FIGURE 7. Reset timing.

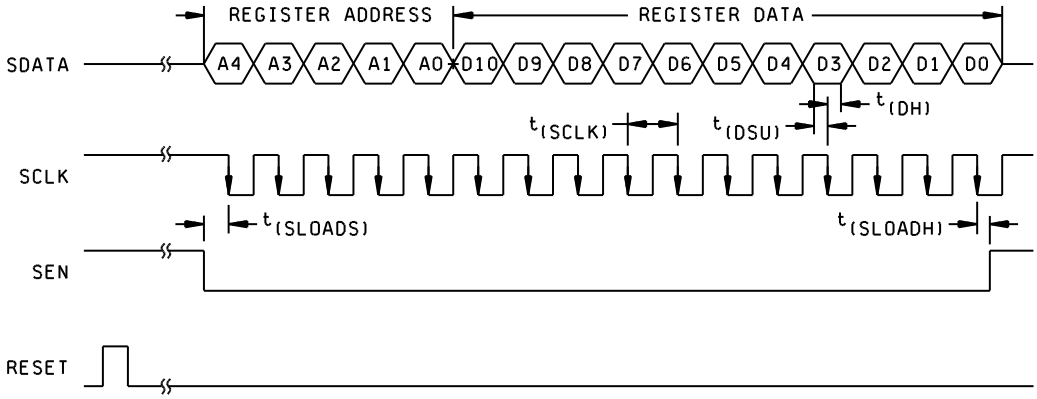


FIGURE 8. Serial interface timing.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/08628-01XE	01295	ADS6445MRGCTEP	6445EP
V62/08628-02XE	01295	ADS6444MRGCTEP	6444EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243