REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Make change to note 2 as specified under paragraph 6.3. Update document paragraphs to current requirements. - ro	15-05-14	C. SAFFLE
B	Add JEDEC references to section 2. Make change to the minimum “c” dimension and make changes to notes 2, 3 as specified under figure 1. Update document paragraphs to current requirements. - ro	21-01-13	J. ESCHMEYER

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV	B	B	B																		
PAGE	18	19	20																		

REV STATUS OF PAGES	**REV**	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 08-07-29	**CHECKED BY** RAJESH PITHADIA	**TITLE** MICROCIRCUIT, DIGITAL, HIGH SPEED ISOLATORS, MONOLITHIC SILICON
	APPROVED BY ROBERT M. HEBER	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/08627**
	REV **B**	**PAGE** 1 **OF** 20

AMSC N/A

5962-V094-20

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance high speed isolator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/08627	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ISO721M-EP	High speed isolator
02	ISO722M-EP	High speed isolator

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MS-012-AA	Plastic gullwing lead surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC1}, V_{CC2}) ..... -0.5 V to 6 V 2/
Voltage at IN, OUT, or $\overline{EN}$ terminal ..... -0.5 V to 6 V
Output current (I_O) ..... ±15 mA
Electrostatic discharge (ESD):
  Human body model (HBM) all pins ..... ±2 kV
  Charged device model (CDM) all pins ..... ±1 kV
Maximum junction temperature (T_J) ..... +170°C
Storage temperature range (T_{STG}) ..... -65°C to +150°C

1.4 Recommended operating conditions. 3/

Supply voltage:
  (V_{CC1}) ..... 4.5 V to 5.5 V
  (V_{CC2}) ..... 3 V to 3.6 V
High level output current (I_{OH}) ..... 4 mA maximum
Low level output current (I_{OL}) ..... -4 mA minimum
High level input voltage (V_{IH}) (IN, $\overline{EN}$ pins) ..... 0.7 V_{CC} to V_{CC}
Low level input voltage (V_{IL}) (IN, $\overline{EN}$ pins) ..... 0 V to 0.3 V_{CC}
Input pulse width (t_{ui}) ..... 6.67 ns minimum
Junction temperature (T_J) ..... +150°C
External magnetic field intensity (H) per IEC 61000-4-8 and IEC 61000-4-9 ..... 1000A/m
Operating free-air temperature range (T_A) ..... -55°C to +125°C

1.5 Thermal characteristics. Specified over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Test conditions	Min	Max	Unit
Junction to air	θ_{JA}	Low – K thermal resistance 4/	263 typical		°C/W
		High – K thermal resistance 4/	125 typical		°C/W
Junction to board thermal resistance	θ_{JB}		44 typical		°C/W
Junction to case thermal resistance	θ_{JC}		75 typical		°C/W
Power dissipation	P_D	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, input a 150 Mbps 50% duty cycle square wave		195	mW

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ All voltage values, except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.
3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
4/ Tested in accordance with the low – K or high – K thermal metric definition of EIA / JESD51-3 for leaded surface mount packages.

2. APPLICABLE DOCUMENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION (IEC)

IEC 60747-5-2	–	Discrete semiconductor devices and integrated circuits – Part 5-2: Optoelectronic devices – Essential rating and characteristics
IEC 61000-4-8	–	Electromagnetic compatibility (EMC) – Part 4-8: Testing and measurement techniques – Power frequency magnetic field immunity test
IEC 61000-4-9	–	Electromagnetic compatibility (EMC) – Part 4-9: Testing and measurement techniques – Pulse magnetic field immunity test

(Copies of these documents are available online at http://www.iec.ch.)

JEDEC Solid State Technology Association

JESD22-C101	–	Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronics Components
JESD22-A114	–	Electrostatic Discharge Sensitivity Testing Human Body Model (HBM)
JEDEC 51-3	–	Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Timing waveforms and test circuits. The timing waveforms and test circuits shall be as shown in figures 4, 5, 6, 7, 8, and 9.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions V_{CC1} and V_{CC2} at 5 V operation	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
V_{CC1} supply current	I_{CC1}	Quiescent, V_I = V_{CC} or 0 V, no load	-55°C to +125°C	All		1	mA
		25 Mbps, V_I = V_{CC} or 0 V, no load				4	
V_{CC2} supply current	I_{CC2}	Quiescent, V_I = V_{CC} or 0 V, no load	-55°C to +125°C	All		12	mA
		25 Mbps, V_I = V_{CC} or 0 V, no load				14	
High level output voltage	V_{OH}	I_{OH} = -4 mA, see figure 4	-55°C to +125°C	All	V_{CC} – 0.8		V
		I_{OH} = -20 μA, see figure 4			V_{CC} – 0.1		
Low level output voltage	V_{OL}	I_{OH} = 4 mA, see figure 4	-55°C to +125°C	All		0.4	V
		I_{OH} = 20 μA, see figure 4				0.1	
Input voltage hysteresis	$V_{I(HYS)}$		+25°C	All	150 typical		mV
High level input current	I_{IH}	IN at 2 V	-55°C to +125°C	All		10	μA
Low level input current	I_{IL}	IN at 0.8 V	-55°C to +125°C	All	-10		μA
High impedance output current	I_{OZ}	$\overline{EN}$, IN at V_{CC}	+25°C	02	1 typical		μA
Input capacitance to ground	C_I	IN at V_{CC}, V_I = 0.4 sin (4E6πt)	+25°C	All	1 typical		pF
Common mode transient immunity	CMTI	V_I = V_{CC} or 0 V, see figure 8	-55°C to +125°C	All	25		kV/μs

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued. 1/

Test	Symbol	Conditions V_{CC1} and V_{CC2} at 5 V operation	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Propagation delay, low to high level output	t_{PLH}	$\overline{EN}$ at 0 V, see figure 4	-55°C to +125°C	01	2	16	ns
Propagation delay, high to low level output	t_{PHL}	$\overline{EN}$ at 0 V, see figure 4	-55°C to +125°C	01	2	16	ns
Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$	$t_{sk(p)}$	$\overline{EN}$ at 0 V, see figure 4	-55°C to +125°C	01		1	ns
Part to part skew	$t_{sk(pp)}$	2/	-55°C to +125°C	All		3	ns
Output signal rise time	t_r	$\overline{EN}$ at 0 V, see figure 4	+25°C	All	1 typical		ns
Output signal fall time	t_f	$\overline{EN}$ at 0 V, see figure 4	+25°C	All	1 typical		ns
Sleep mode propagation delay, high level to high impedance output	t_{PHZ}	See figure 5	+25°C	02	8 typical		ns
Sleep mode propagation delay, high impedance to high level output	t_{PZH}	See figure 5	+25°C	02	4 typical		µs
Sleep mode propagation delay, low level to high impedance output	t_{PLZ}	See figure 6	+25°C	02	8 typical		ns
Sleep mode propagation delay, high impedance to low level output	t_{PZL}	See figure 6	+25°C	02	5 typical		µs
Failsafe output delay time from input power loss	t_{fs}	See figure 7	+25°C	All	3 typical		µs
Peak to peak eye pattern jitter	$t_{jit(PP)}$	150 Mbps NRZ data input, see figure 9	+25°C	All	1 typical		ns
		150 Mbps unrestricted bit run length data input, see figure 9			2 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions V_{CC1} at 5 V, V_{CC2} at 3.3 V operation	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
V_{CC1} supply current	I_{CC1}	Quiescent, V_I = V_{CC} or 0 V, no load	-55°C to +125°C	All		1	mA
		25 Mbps, V_I = V_{CC} or 0 V, no load				4	
V_{CC2} supply current	I_{CC2}	Quiescent, V_I = V_{CC} or 0 V, no load	-55°C to +125°C	All		6.5	mA
		25 Mbps, V_I = V_{CC} or 0 V, no load				7.5	
High level output voltage	V_{OH}	I_{OH} = -4 mA, see figure 4	-55°C to +125°C	All	V_{CC} – 0.4		V
		I_{OH} = -20 μA, see figure 4			V_{CC} – 0.1		
Low level output voltage	V_{OL}	I_{OH} = 4 mA, see figure 4	-55°C to +125°C	All		0.4	V
		I_{OH} = 20 μA, see figure 4				0.1	
Input voltage hysteresis	$V_{I(HYS)}$		+25°C	All	150 typical		mV
High level input current	I_{IH}	IN at 2 V	-55°C to +125°C	All		10	μA
Low level input current	I_{IL}	IN at 0.8 V	-55°C to +125°C	All	-10		μA
High impedance output current	I_{OZ}	$\overline{EN}$, IN at V_{CC}	+25°C	02	1 typical		μA
Input capacitance to ground	C_I	IN at V_{CC}, V_I = 0.4 sin (4E6πt)	+25°C	All	1 typical		pF
Common mode transient immunity	CMTI	V_I = V_{CC} or 0 V, see figure 8	-55°C to +125°C	All	25		kV/μs

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued. 1/

Test	Symbol	Conditions V_{CC1} at 5 V, V_{CC2} at 3.3 V operation	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Propagation delay, low to high level output	t_{PLH}	$\overline{EN}$ at 0 V, see figure 4	-55°C to +125°C	01	3	20	ns
Propagation delay, high to low level output	t_{PHL}	$\overline{EN}$ at 0 V, see figure 4	-55°C to +125°C	01	3	20	ns
Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$	$t_{sk(p)}$	$\overline{EN}$ at 0 V, see figure 4	-55°C to +125°C	01		1	ns
Part to part skew	$t_{sk(pp)}$	2/	-55°C to +125°C	All		5	ns
Output signal rise time	t_r	$\overline{EN}$ at 0 V, see figure 4	+25°C	All	2 typical		ns
Output signal fall time	t_f	$\overline{EN}$ at 0 V, see figure 4	+25°C	All	2 typical		ns
Sleep mode propagation delay, high level to high impedance output	t_{PHZ}	See figure 5	+25°C	02	11 typical		ns
Sleep mode propagation delay, high impedance to high level output	t_{PZH}	See figure 5	+25°C	02	6 typical		µs
Sleep mode propagation delay, low level to high impedance output	t_{PLZ}	See figure 6	+25°C	02	13 typical		ns
Sleep mode propagation delay, high impedance to low level output	t_{PZL}	See figure 6	+25°C	02	6 typical		µs
Failsafe output delay time from input power loss	t_{fs}	See figure 7	+25°C	All	3 typical		µs
Peak to peak eye pattern jitter	$t_{jit(PP)}$	150 Mbps NRZ data input, see figure 9	+25°C	All	1 typical		ns
		150 Mbps unrestricted bit run length data input, see figure 9			2 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions V_{CC1} at 3.3 V, V_{CC2} at 5 V operation	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
V_{CC1} supply current	I_{CC1}	Quiescent, V_I = V_{CC} or 0 V, no load	-55°C to +125°C	All		0.5	mA
		25 Mbps, V_I = V_{CC} or 0 V, no load				2	
V_{CC2} supply current	I_{CC2}	Quiescent, V_I = V_{CC} or 0 V, no load	-55°C to +125°C	All		12	mA
		25 Mbps, V_I = V_{CC} or 0 V, no load				14	
High level output voltage	V_{OH}	I_{OH} = -4 mA, see figure 4	-55°C to +125°C	All	V_{CC} – 0.8		V
		I_{OH} = -20 μA, see figure 4			V_{CC} – 0.1		
Low level output voltage	V_{OL}	I_{OH} = 4 mA, see figure 4	-55°C to +125°C	All		0.4	V
		I_{OH} = 20 μA, see figure 4				0.1	
Input voltage hysteresis	$V_{I(HYS)}$		+25°C	All	150 typical		mV
High level input current	I_{IH}	IN at 2 V	-55°C to +125°C	All		10	μA
Low level input current	I_{IL}	IN at 0.8 V	-55°C to +125°C	All	-10		μA
High impedance output current	I_{OZ}	$\overline{EN}$, IN at V_{CC}	+25°C	02	1 typical		μA
Input capacitance to ground	C_I	IN at V_{CC}, V_I = 0.4 sin (4E6πt)	+25°C	All	1 typical		pF
Common mode transient immunity	CMTI	V_I = V_{CC} or 0 V, see figure 8	-55°C to +125°C	All	25		kV/μs

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued. 1/

Test	Symbol	Conditions V_{CC1} at 3.3 V, V_{CC2} at 5 V operation	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Propagation delay, low to high level output	t_{PLH}	$\overline{EN}$ at 0 V, see figure 4	-55°C to +125°C	01	3	21	ns
Propagation delay, high to low level output	t_{PHL}	$\overline{EN}$ at 0 V, see figure 4	-55°C to +125°C	01	3	21	ns
Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$	$t_{sk(p)}$	$\overline{EN}$ at 0 V, see figure 4	-55°C to +125°C	01		1	ns
Part to part skew	$t_{sk(pp)}$	2/	-55°C to +125°C	All		5	ns
Output signal rise time	t_r	$\overline{EN}$ at 0 V, see figure 4	+25°C	All	1 typical		ns
Output signal fall time	t_f	$\overline{EN}$ at 0 V, see figure 4	+25°C	All	1 typical		ns
Sleep mode propagation delay, high level to high impedance output	t_{PHZ}	See figure 5	+25°C	02	9 typical		ns
Sleep mode propagation delay, high impedance to high level output	t_{PZH}	See figure 5	+25°C	02	5 typical		µs
Sleep mode propagation delay, low level to high impedance output	t_{PLZ}	See figure 6	+25°C	02	9 typical		ns
Sleep mode propagation delay, high impedance to low level output	t_{PZL}	See figure 6	+25°C	02	5 typical		µs
Failsafe output delay time from input power loss	t_{fs}	See figure 7	+25°C	All	3 typical		µs
Peak to peak eye pattern jitter	$t_{jit(PP)}$	150 Mbps NRZ data input, see figure 9	+25°C	All	1 typical		ns
		150 Mbps unrestricted bit run length data input, see figure 9			2 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued. 1/

Test	Symbol	Conditions V_{CC1} and V_{CC2} at 3.3 V operation	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
V_{CC1} supply current	I_{CC1}	Quiescent, V_I = V_{CC} or 0 V, no load	-55°C to +125°C	All		0.5	mA
		25 Mbps, V_I = V_{CC} or 0 V, no load				2	
V_{CC2} supply current	I_{CC2}	Quiescent, V_I = V_{CC} or 0 V, no load	-55°C to +125°C	All		6.5	mA
		25 Mbps, V_I = V_{CC} or 0 V, no load				7.5	
High level output voltage	V_{OH}	I_{OH} = -4 mA, see figure 4	-55°C to +125°C	All	V_{CC} – 0.4		V
		I_{OH} = -20 μA, see figure 4			V_{CC} – 0.1		
Low level output voltage	V_{OL}	I_{OH} = 4 mA, see figure 4	-55°C to +125°C	All		0.4	V
		I_{OH} = 20 μA, see figure 4				0.1	
Input voltage hysteresis	$V_{I(HYS)}$		+25°C	All	150 typical		mV
High level input current	I_{IH}	IN at 2 V	-55°C to +125°C	All		10	μA
Low level input current	I_{IL}	IN at 0.8 V	-55°C to +125°C	All	-10		μA
High impedance output current	I_{OZ}	$\overline{EN}$, IN at V_{CC}	+25°C	02	1 typical		μA
Input capacitance to ground	C_I	IN at V_{CC}, V_I = 0.4 sin (4E6πt)	+25°C	All	1 typical		pF
Common mode transient immunity	CMTI	V_I = V_{CC} or 0 V, see figure 8	-55°C to +125°C	All	25		kV/μs

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued. 1/

Test	Symbol	Conditions V_{CC1} and V_{CC2} at 3.3 V operation	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Propagation delay, low to high level output	t_{PLH}	$\overline{EN}$ at 0 V, see figure 4	-55°C to +125°C	01	3	25	ns
Propagation delay, high to low level output	t_{PHL}	$\overline{EN}$ at 0 V, see figure 4	-55°C to +125°C	01	3	25	ns
Pulse skew $\lvert t_{PHL} - t_{PLH} \rvert$	$t_{sk(p)}$	$\overline{EN}$ at 0 V, see figure 4	-55°C to +125°C	01		1	ns
Part to part skew	$t_{sk(pp)}$	2/	-55°C to +125°C	All		5	ns
Output signal rise time	t_r	$\overline{EN}$ at 0 V, see figure 4	+25°C	All	2 typical		ns
Output signal fall time	t_f	$\overline{EN}$ at 0 V, see figure 4	+25°C	All	2 typical		ns
Sleep mode propagation delay, high level to high impedance output	t_{PHZ}	See figure 5	+25°C	02	13 typical		ns
Sleep mode propagation delay, high impedance to high level output	t_{PZH}	See figure 5	+25°C	02	6 typical		µs
Sleep mode propagation delay, low level to high impedance output	t_{PLZ}	See figure 6	+25°C	02	13 typical		ns
Sleep mode propagation delay, high impedance to low level output	t_{PZL}	See figure 6	+25°C	02	6 typical		µs
Failsafe output delay time from input power loss	t_{fs}	See figure 7	+25°C	All	3 typical		µs
Peak to peak eye pattern jitter	$t_{jit(PP)}$	150 Mbps NRZ data input, see figure 9	+25°C	All	1 typical		ns
		150 Mbps unrestricted bit run length data input, see figure 9			2 typical		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ $t_{sk(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

Case X

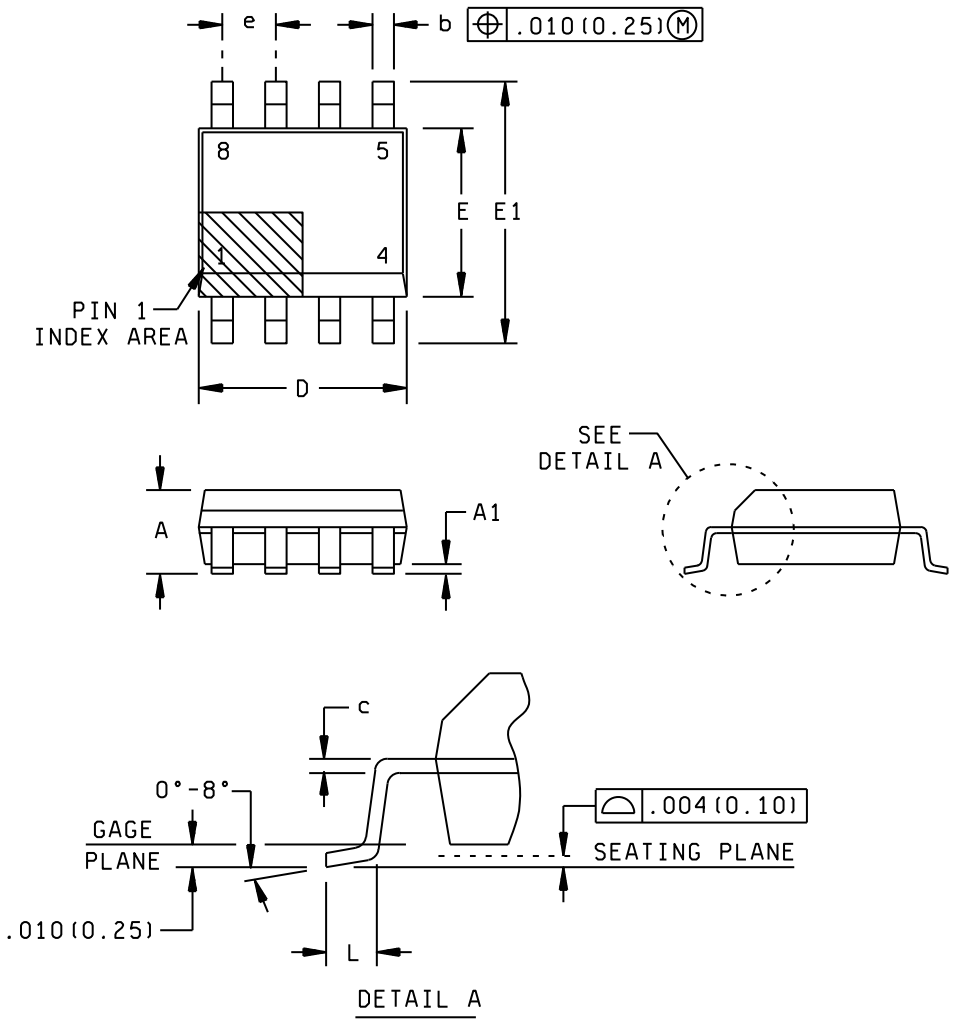


FIGURE 1. Case outline.

Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.069	---	1.75
A1	0.004	0.010	0.10	0.25
b	0.012	0.020	0.31	0.51
c	0.005	0.010	0.13	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
E1	0.228	0.244	5.80	6.20
e	0.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27
n	8		8	

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. Dimension D body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 inch (0.15 mm) per side.
3. Dimension E body width does not include interlead flash..
4. Falls within JEDEC MS-012-AA.

FIGURE 1. Case outline – Continued.

Device types	01	02
Case outline	X	
Terminal number	Terminal symbol	
1	V_{CC1}	V_{CC1}
2	IN	IN
3	V_{CC1}	V_{CC1}
4	GND1	GND1
5	GND2	GND2
6	OUT	OUT
7	GND2	$\overline{EN}$
8	V_{CC2}	V_{CC2}

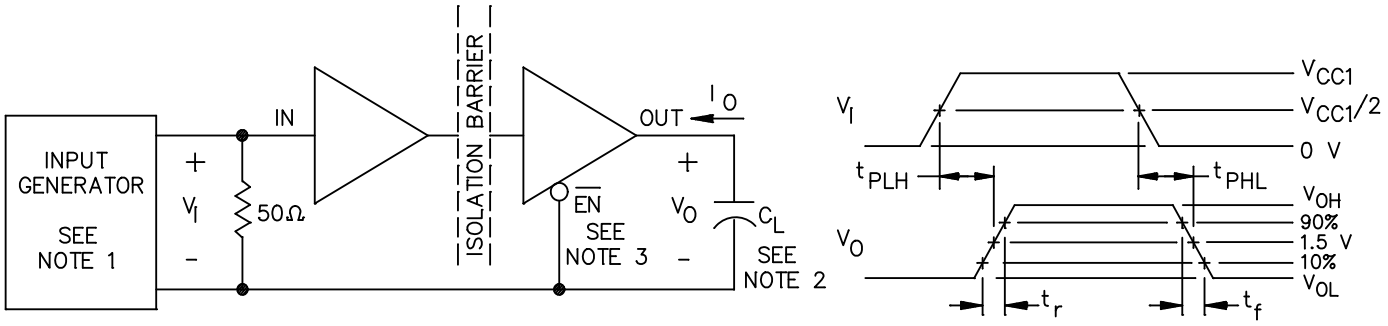
FIGURE 2. Terminal connections.

Device type 01 1/			
V_{CC1}	V_{CC2}	INPUT (IN)	OUTPUT (OUT)
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H

Device type 02 1/				
V_{CC1}	V_{CC2}	INPUT (IN)	OUTPUT ENABLE ($\overline{EN}$)	OUTPUT (OUT)
PU	PU	H	L or open	H
		L	L or open	L
		X	H	Z
		Open	L or open	H
PD	PU	X	L or open	H
PD	PU	X	H	Z

1/ PU = powered up ($V_{CC} \geq 3$ V); PD = powered down ($V_{CC} \leq 2.5$ V), X = irrelevant, H = high level, and L = low level.

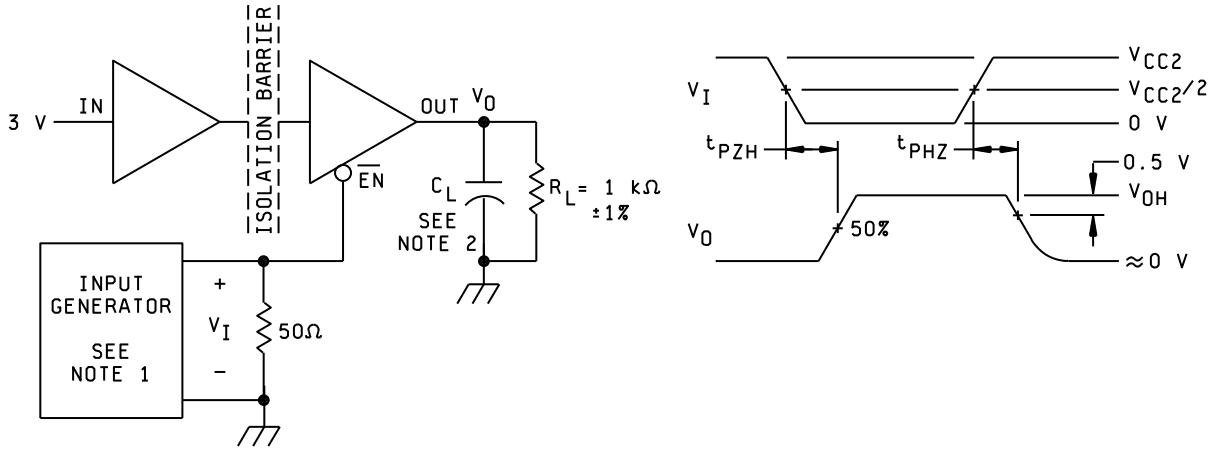
FIGURE 3. Truth tables.



NOTES:

1. The input pulse is supplied by a generator having the following characteristics:
   PRR ≤ 50 kHz, 50 % duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.
2. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.
3. The $\overline{EN}$ pin applies to device type 02 only.

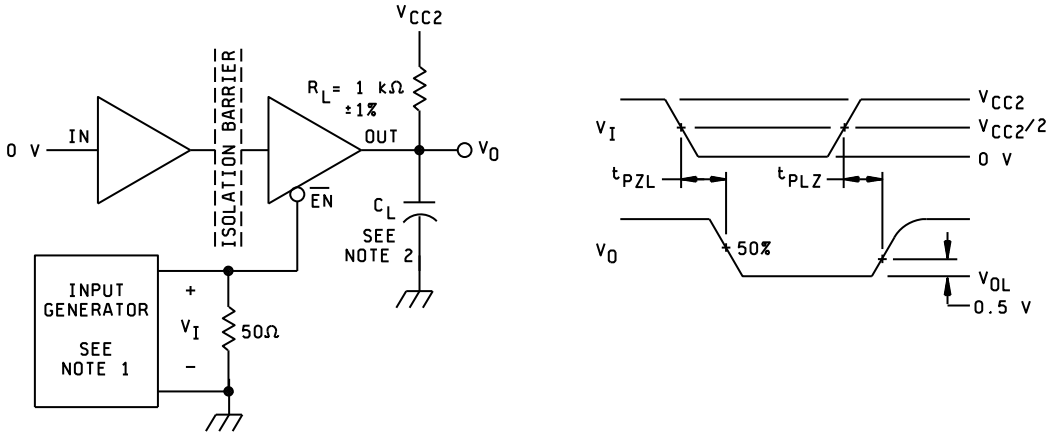
FIGURE 4. Switching characteristic test circuit and voltage waveforms.



NOTES:

1. The input pulse is supplied by a generator having the following characteristics:
   PRR ≤ 50 kHz, 50 % duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.
2. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

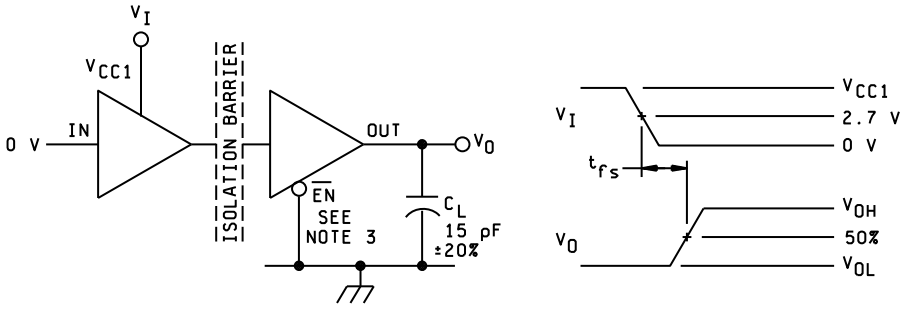
FIGURE 5. Sleep mode high level output test circuit and voltage waveforms for device type 02.



NOTES:

1. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50 % duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.
2. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

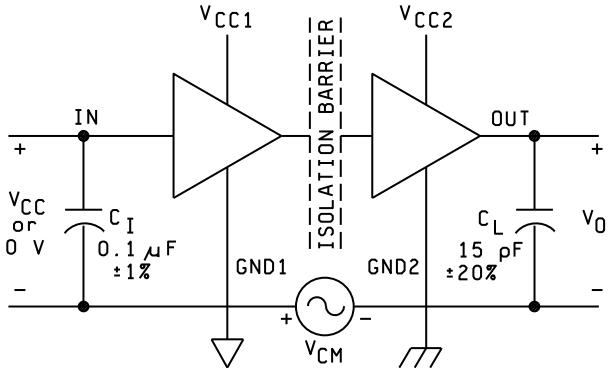
FIGURE 6. Sleep mode low level output test circuit and voltage waveforms for device type 02.



NOTES:

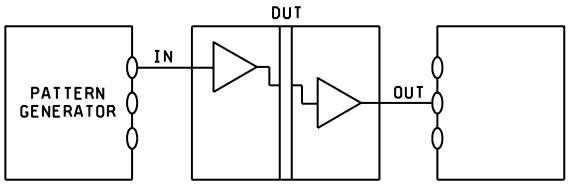
1. The V_I transition time is 100 ns.
2. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.
3. The $\overline{EN}$ pin applies to device type 02 only.

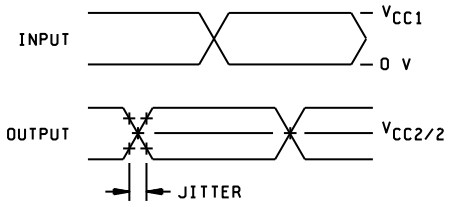
FIGURE 7. Failsafe delay time test circuit and voltage waveforms.



NOTE: Pass / fail criteria is no change in V_O.

FIGURE 8. Common mode transient immunity test circuit and voltage waveform.





NOTE: Bit pattern run length is $2^{16} - 1$. Transition time is 800 ps. Non return to zero (NRZ) data input has no more than five consecutive ones or zeros.

FIGURE 9. Peak to peak eye pattern jitter test circuit and voltage waveform.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/ 2/	Device manufacturer CAGE code	Output enabled	Input threshold	Noise filter	Top side marking	Vendor part number
V62/08627-01XE	01295	No	CMOS	No	721MEP	ISO721MMDREP
V62/08627-02XE	3/	Yes	CMOS	No	722MEP	ISO722MMDREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Package drawings, thermal data, and symbolization are available from the manufacturer.
3/ Not available from an approved source of supply.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243