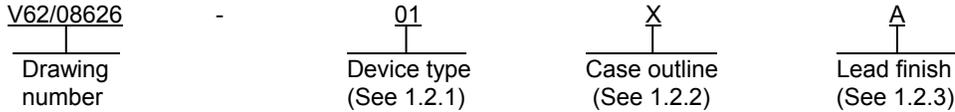


1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance ultralow-power NTSC/PAL/SECAM video decoder microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	TVP5150AM1-EP	Ultralow-power NTSC/PAL/SECAM video decoder

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>Package style</u>
X	32	Plastic quad flatpack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range:	
IO_DVDD to DGND	-0.5 V to 4.5 V
DVDD to DGND	-0.5 V to 2.3 V
PLL_AVDD to PLL_AGND	-0.5 V to 2.3 V
CH_AVDD to CH_AGND	-0.5 V to 2.3 V
Digital input voltage range, V _I to DGND	-0.5 V to 4.5 V
Input voltage range, XTAL1 to PLL_GND	-0.5 V to 2.3 V
Analog input voltage range A1 to CH_AGND	-0.2 V to 2.0 V
Digital output voltage range, V _O to DGND	-0.5 V to 4.5 V
Storage temperature range, T _{STG}	-65°C to 150°C

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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1.4 Recommended operating conditions.

Digital I/O supply voltage, IO_DVDD	3.0 V to 3.6 V
Digital supply voltage, DVDD	1.65 V to 1.95 V
Analog PLL supply voltage	1.65 V to 1.95 V
Analog core supply voltage, CH_AVDD	1.65 V to 1.95 V
Analog input voltage (ac-coupling necessary), V _{I(P-P)}	0 V to 0.75 V
Minimum digital input voltage high, V _{IH}	0.7 IO_DVDD V
Maximum digital input voltage low, V _{IL}	0.3 IO_DVDD V
Minimum XTAL input voltage high, V _{IH_XTAL}	0.7 PLL_AVDD V
Maximum XTAL input voltage low, V _{IL_XTAL}	0.3 PLL_AVDD V
Maximum high level output current, IOH	2 mA
Maximum low level output current, IOL	-2 mA
Maximum SCLK high level output current, I _{OH_SCLK}	4 mA
Maximum SCLK low level output current, I _{OL_SCLK}	-4 mA
Operating free air temperature	-55°C to 125°C

2. APPLICABLE DOCUMENTS

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industry Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or at <http://www.jedec.org>)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4-5.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	Limits		Unit
			Min	Max	
DC electrical characteristics 3/					
3.3 V I/O digital supply current	$I_{DD(I/O)}$	Color bar input 4/		10.0	mA
1.8 V digital supply current	$I_{DD(D)}$	Color bar input 4/		32.9	mA
1.8 V analog PLL supply current	$I_{DD(PLL)}$	Color bar input 4/		7.1	mA
1.8 V analog core supply current	$I_{DD(CH)}$	Color bar input 4/		36.0	mA
Total power dissipation, normal mode	P_{TOT}	Color bar input 4/		160	mW
Total power dissipation, power down mode 5/		Color bar input	1 TYP		mW
Input capacitance	C_i	By design	8 TYP		pF
Output voltage high	V_{OH}	$I_{OH} = 2$ mA	0.8 IO_DVDD		V
Output voltage low	V_{OL}	$I_{OL} = -2$ mA		0.22 IO_DVDD	V
SCLK output voltage high	V_{OH_SCLK}	$I_{OH} = 4$ mA	0.8 IO_DVDD		V
SCLK output voltage low	V_{OL_SCLK}	$I_{OL} = -4$ mA		0.22 IO_DVDD	V
High level input current 6/	I_{IH}	$V_i = V_{IH}$		± 28	μ A
Low level input current 6/	I_{iL}	$V_i = V_{iL}$		± 28	μ A
Analog electrical characteristics					
Input impedance, analog video inputs	Z_i	By design	500 TYP		k Ω
Input capacitance, analog video inputs	C_i	By design	10 TYP		pF
Input voltage range 7/	$V_{i(pp)}$	$C_{coupling} = 0.1$ μ F	0	0.75	V
Gain control maximum	ΔG		12 TYP		dB
Gain control minimum	ΔG		0 TYP		dB
DC differential nonlinearity	DNL	A/D only		± 1	LSB
DC integral nonlinearity	INL	A/D only		± 2.5	LSB
Frequency response	F_r	6 MHz, Specified by design		-3	dB
Signal to noise ratio	SNR	6 MHz, 1.0 V_{p-p}	50 TYP		dB
Noise spectrum	NS	50% flat field	50 TYP		dB
Differential phase	DP		1.5 TYP		$^\circ$
Differential gain	DG		0.5 TYP		%

See footnotes at end of table.

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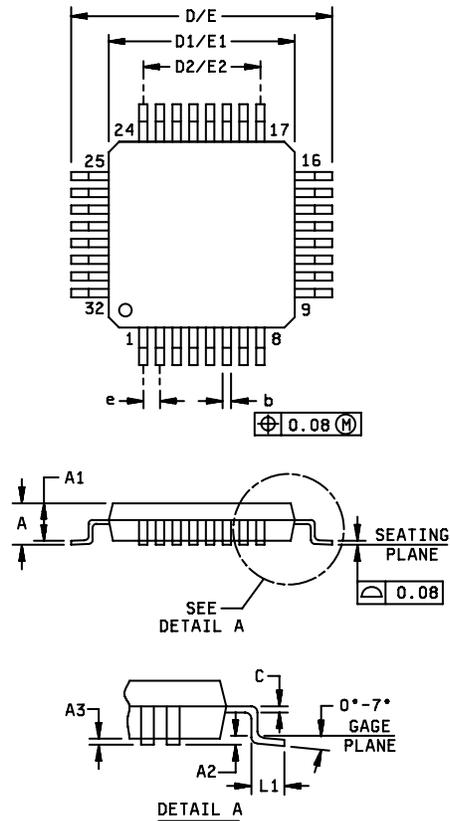
TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>2/</u> unless otherwise specified	Limits		Unit
			Min	Max	
Clocks, Video data, Sync timing <u>8/</u> See figure 4					
Duty cycle, PCLK			50 TYP		%
PCLK high time	t1	≥80%	16	22	ns
PCLK low time	t2	≤20%	16	22	
PCLK fall time	t3	80% to 20%	4 TYP		
PCLK rise time	t4	20% to 80%	4 TYP		
Output hold time	t5		2 TYP		
Output delay time	t6		3 TYP		
I²C host port timing <u>9/</u> See figure 5					
Bus free time between Stop and Start	t1		1.3		μs
Setup time for a (repeated) Start condition	t2		0.6		μs
Hold time (repeated) Start condition	t3		0.6		μs
Setup time for a Stop condition	t4		0.6		ns
Data setup time	t5		100		ns
Data hold time	t6		0	0.9	μs
Rise time, VC1(SDA) and VC0(SCL) signal	t7		250		ns
Fall time, VC1(SDA) and VC0(SCL) signal	t8		250 TYP		ns
Capacitive load for each bus line	Cb			400	pF
I ² C clock frequency	f _{I2C}			400	kHz

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ -55°C ≤ T_A ≤ 125°C, DVDD = 1.8 V, PLL_AVDD = 1.8 V, CH_AVDD = 1.8 V, IO_DVDD = 3.3 V; for Typical value T_A = 25°C unless otherwise noted.
- 3/ Measured with a load of 15 pF.
- 4/ For typical measurements only.
- 5/ Specified by device characterization.
- 6/ YOUT7 is a bidirectional terminal with an internal pull down resistor. This terminal may sink more than the specified current when in RESET mode.
- 7/ The 0.75 V maximum applies to the sync-chroma amplitude, not sync-white. The recommended termination resistor are 37.4 Ω, as seen in the manufacturer data book.
- 8/ Measured with a load of 15 pF. Specified by design.
- 9/ Specified by design for industrial temperature.

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Case X



Dimension					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	D/E	6.90	7.10
A1	0.95	1.05	D1/E1	4.95	5.05
A2	0.25 TYP		D2/E2	3.50 TYP	
A3	0.05	0.15	e	0.50 BSC	
b	0.17	0.23	L1	0.40	0.70
C	0.13 NOM				

NOTES:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.

FIGURE 1. Case outline.

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Case X							
Terminal number	Terminal symbol						
1	AIP1A	9	PCLK/SCLK	17	YOUT1	25	HSYNC
2	AIP1B	10	IO_DVDD	18	YOUT0	26	AVID
3	PLL_AGND	11	YOUT7/I2CSEL	19	DGND	27	AVIDINTREQ/GPCL/VBLK
4	PLL_AVDD	12	YOUT6	20	DVDD	28	PDN
5	XTAL1/OSC	13	YOUT5	21	SCL	29	REFP
6	XTAL2	14	YOUT4	22	SDA	30	REFM
7	AGND	15	YOUT3	23	FID/GLCO	31	CH_AGND
8	RESETB	16	YOUT2	24	VSYNC/PALI	32	CH_AVDD

FIGURE 2. Terminal connections.

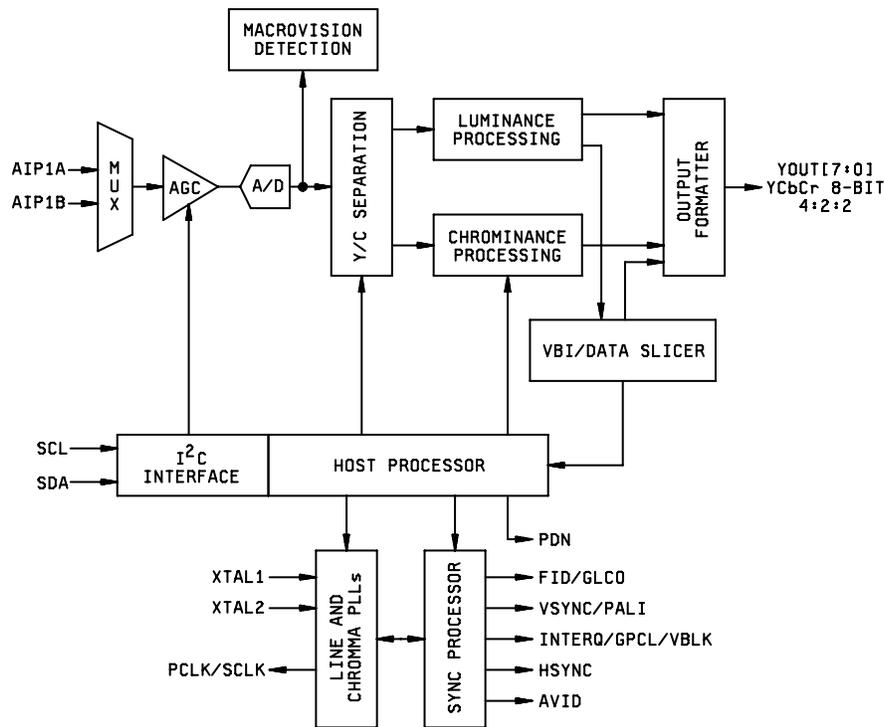
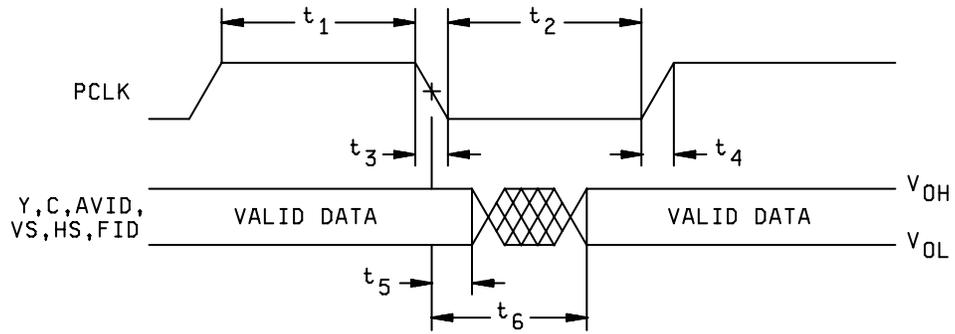


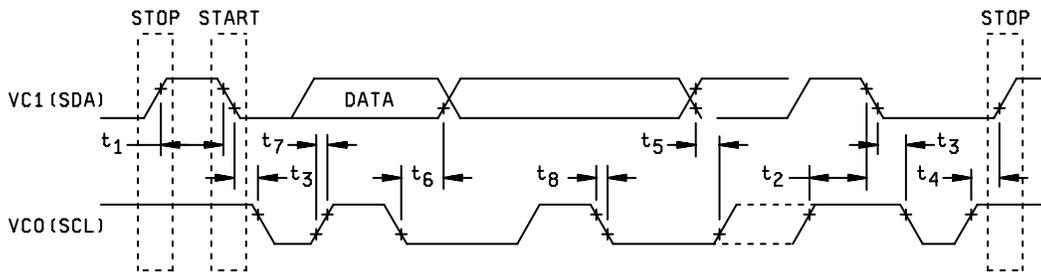
FIGURE 3. Functional block diagram.

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Clocks, Video data, and Sync Timing

FIGURE 4. Timing waveforms.



I²C Host port timing

FIGURE 5. Timing waveforms.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/08626-01XE	01295	TVP5150AM1MPBSREP	5150MEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

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