REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY MM DD 08-06-24	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL, IEEE-1394 LINK LAYER CONTROLLER, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/08625**
	REV	**PAGE** 1 **OF** 17

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance IEEE-1394 Link Layer controller microcircuit, with an extended operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/08625	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TSB12LV21B-EP	IEEE-1394 Link layer Controller

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	176	JEDEC MO-136	Plastic quad flat pack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range:
- V_{CC} ..... -0.5 V to +4.0 V
- V_{CCP} ..... -0.5 V to +6.0 V
- V_{CC5V} ..... -0.5 V to +6.0 V

Input voltage range for Universal PCI, (V_I) ..... -0.5 V to V_{CCP}+0.5 V
Input voltage range for 5 V tolerant TTL/LVCMOS, (V_I) ..... -0.5 V to V_{CCP}+0.5 V
Output voltage range for Universal PCI, (V_O) ..... -0.5 V to V_{CCP}+0.5 V
Output voltage range for 5 V tolerant TTL/LVCMOSI, (V_O) ..... -0.5 V to V_{CC5V}+0.5 V
Input clamp current (V_I < 0 or V_I > V_{CC}) (I_{IK}) ..... ±20 mA 3/
Output clamp current (V_O < 0 or V_O > V_{CC}) (I_{OK}) ..... ±20 mA 4/

1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Long term high temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See manufacturer data for more information on enhanced plastic package.
3/ Applies to external input and bidirectional buffers. For 5 V tolerant buffers, use $V_I > V_{CC5V}$. For Universal PCI, use $V_I > V_{CCP}$.
4/ Applies to external output and bidirectional buffers. For 5 V tolerant buffers, use $V_O > V_{CC5V}$. For Universal PCI, use $V_O > V_{CCP}$.

1.4 Recommended operating conditions. 5/

Core voltage (V_{CC}) ..... +3.0 V to +3.6 V
I/O voltage (V_{CCP}) ..... +3.0 V to +5.5 V
I/O voltage (V_{CC5V}) ..... +3.0 V to +5.5 V
Minimum high level input voltage (V_{IH}) ..... 2.0 V 6/
Maximum low level input voltage (V_{IL}) ..... 0.8 V 6/
Input voltage:
Universal PCI (V_I) ..... 0.0 V to V_{CCP}
5 V tolerant (V_I) ..... 0.0 V to V_{CC5V}
Output voltage, (V_O) ..... 0.0 V to V_{CC} 7/
Input transition times (t_r and t_f) ..... 0 ns to 6 ns
Operating free-air temperature range (T_A)..... -55°C to +125°C
Virtual junction temperature (Commercial and industrial) ..... 0°C to +115°C 8/

2. APPLICABLE DOCUMENTS

IEEE Standard 1394a - IEEE Standard for Higher Performance Serial Buses Allowing Gigabit Signaling.

(Applications for copies should be addressed to the Institute of Electrical and Electronic Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industry Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or at http://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

5/ Unused or floating pin (input or I/O) must be held high or low.
6/ Applies for external input and bidirectional buffers without hysteresis.
7/ Applies for external output buffers.
8/ These junction temperatures reflect simulation conditions. Customer is responsible for verifying the junction temperature. Absolute maximum junction temperature is 150°C.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as specified in figure 3.

3.5.4 PCI interface timing waveforms. The PCI interface timing waveforms shall be as specified in figure 4.

3.5.5 Phy_Link interface timing waveforms. The Phy_Link interface timing waveforms shall be as specified in figure 5.

3.5.6 Local bus timing waveforms. The local bus timing waveforms shall be as specified in figure 6.

3.5.7 Zoom Video IF timing waveforms (8 bit, divide-by-2 mode). The Zoom Video IF timing waveforms (8 bit, divide-by-2 mode) shall be as specified in figure 7.

3.5.8 Zoom Video IF timing waveforms (16 bit, divide-by-1 mode). The Zoom Video IF timing waveforms (16 bit, divide-by-1 mode) shall be as specified in figure 8.

3.5.9 Zoom Video IF timing waveforms (16 bit, divide-by-2 mode). The Zoom Video IF timing waveforms (16 bit, divide-by-2 mode) shall be as specified in figure 9.

TABLE I. Electrical performance characteristics. 1/

Test 1/			Symbol	Operation	Test condition 2/ unless otherwise noted	Limits Min	Limits Max	Unit
High level output voltage 3/	PCI		V_{OH}	3.3 V	I_{OH} = -0.5 mA	0.9 V_{CC}		V
				5 V	I_{OH} = -2 mA	2.4		
	TTL/LVCMOS 4/				I_{OH} = -18 mA	2.4		
	TTL/LVCMOS 4/				I_{OH} = -14 mA	2.4		
Low level output voltage	PCI		V_{OL}	3.3 V	I_{OL} = 1.5 mA		0.1 V_{CC}	V
				5 V	I_{OL} = 6 mA		0.5	
	TTL/LVCMOS 5/				I_{OL} = 18 mA		0.5	
	TTL/LVCMOS 5/				I_{OL} = 14 mA		0.5	
Low level input current	Input pins	Bushold	I_{IL}		V_I = 0.8 V		20	µA
		Others			V_I = GND		-1	
	I/O pins	Bushold			V_I = 0.8 V		400	
		Others			V_I = GND		-20	
High level input current	Input pins	Bushold	I_{IH}		V_I = 2 V		-20	µA
		Others			V_I = 5.5 V		20	
	I/O pins	Bushold			V_I = 2 V		-20	
		Others			V_I = 5.5 V		20	

Test	Symbol	Measured	Test condition 2/ unless otherwise noted	Limits Min	Limits Max	Unit
PCI interface switching characteristics (See figure 4)						
Setup time, pci_xx low or high to pci_clk high 6/	t_{su1}	40% to 40%		7		ns
Hold time, pci_clk high to pci_xx low or high, $\overline{\text{pci_gnt}}$ low or high 6/	t_{h1}	40% to 40%		0		
Delay time, pci_clk high to pci_xx low or high 6/	t_{d1}	40% to 40%		2	11	
Setup time, $\overline{\text{pci_gnt}}$ low or high to pci_clk high	t_{su2}	40% to 40%		10		
Delay time, pci_clk high to $\overline{\text{pci_int a}}$ low or high	t_{d2}	40% to 40%		2	13	

See notes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Measured	Test condition 2/ unless otherwise noted	Limits		Unit
				Min	Max	
PHY-LINK interface switching characteristics (See figure 5)						
Setup time, phy_xx low or high to phy_clk high 7/	t_{su3}	1.3 V to 1.3 V		4		ns
Hold time, phy_clk high to phy_xx, link_cyclein low or high	t_{h2}	1.3 V to 1.3 V		1		
Delay time, phy_clk high to phy_xx, phy_Ireq low or high 7/	t_{d3}	1.3 V to 1.3 V		3	11	
Setup time, phy_clk high to link_cyclein low or high	t_{su4}	1.3 V to 1.3 V		5		
Delay time, phy_clk high to link_cycleout low or high	t_{d4}	1.3 V to 1.3 V		3	13	
Local bus switching characteristics (See figure 6)						
Delay time, aux_clk high to aux_adr, aux_data 15-0 (write), $\overline{aux_oe}$ valid 8/	t_{d5}	1.3 V to 1.3 V		0	15	ns
Delay time, aux_clk high to $\overline{rom_cs}$, $\overline{ram_cs}$, $\overline{aux_cs}$ valid	t_{d6}	1.3 V to 1.3 V		0	20	
Delay time, $\overline{aux_we0}$, $\overline{aux_we1}$ high (deasserted) to aux_adr, aux_data15-0 (write), $\overline{aux_oe}$, $\overline{rom_cs}$, $\overline{ram_cs}$, $\overline{aux_cs}$ valid	t_{d7}	1.3 V to 1.3 V		0.5		
Delay time, aux_clk low to $\overline{aux_we0}$, $\overline{aux_we1}$ low (asserted)	t_{d8}	1.3 V to 1.3 V		0	10	
Delay time, aux_clk high to $\overline{aux_we0}$, $\overline{aux_we1}$ high (deasserted)	t_{d9}	1.3 V to 1.3 V		0	10	
Delay time, aux_clk high to gpio_data3-0 valid	t_{d10}	1.3 V to 1.3 V		2	15	
Setup time, aux_adr, adr_data15-0 (write), $\overline{aux_oe}$, $\overline{rom_cs}$, $\overline{ram_cs}$, $\overline{aux_cs}$ valid before $\overline{aux_we0}$, $\overline{aux_we1}$ low (asserted)	t_{su5}	1.3 V to 1.3 V		5		
Setup time, aux_data15-0 (read), $\overline{aux_rdy}$, gpio_data3-0 valid before aux_clk high	t_{su6}	1.3 V to 1.3 V		10		
Hold time, aux_data15-0 (read), $\overline{aux_rdy}$, gpio_data3-1 invalid after aux_clk high	t_{h3}	1.3 V to 1.3 V		0		

See notes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Measured	Test condition 2/ unless otherwise noted	Limits		Unit
				Min	Max	
Zoom video port switching characteristics, source clock = 30 ns with a 50% duty cycle						
Setup time, zv_vsync, zv_data_valid high before zv_pix_clk high	t_{su7}	1.3 V to 1.3 V	See figure 4	12		ns
Hold time, zv_hsync high zv_vsync, zv_data_valid low after zv_pix_clk low	t_{h4}	1.3 V to 1.3 V		14		
Setup time, aux_data7-0 valid before zv_pix_clk high or low	t_{su8}	1.3 V to 1.3 V		10		
Hold time, aux_data7-0 valid after zv_pix_clk high or low	t_{h5}	1.3 V to 1.3 V		14		
Delay time, zv_hsync low, zv_vsync, zv_data_valid high after zv_pix_clk low	t_{d11}	1.3 V to 1.3 V	See figure 5	-1	3	
Delay time, aux_data7-0 invalid after zv_pix_clk low	t_{d12}	1.3 V to 1.3 V		-1	5	
Setup time, zv_hsync low before zv_pix_clk high	t_{su9}	1.3 V to 1.3 V	See figure 6	25		
Hold time, zv_hsync high after zv_pix_clk high	t_{h6}	1.3 V to 1.3 V		14		
Setup time, zv_vsync low before zv_pix_clk high	t_{su10}	1.3 V to 1.3 V		10		
Setup time, aux_data7-0 valid, zv_data_valid high before zv_pix_clk high	t_{su11}	1.3 V to 1.3 V		25		
Hold time, aux_data7-0 valid, zv_data_valid low after zv_pix_clk high	t_{h7}	1.3 V to 1.3 V		14		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Over recommended operating conditions, unless otherwise noted.

3/ VOH is not tested on $\overline{\text{pci_serr}}$ (31) or $\overline{\text{pci_int a}}$ (166) due to open-drain output.

4/ All PHY-link pins, aux_clk(64), $\overline{\text{aux_we1}}$ (71), and $\overline{\text{aux_we0}}$ (73).

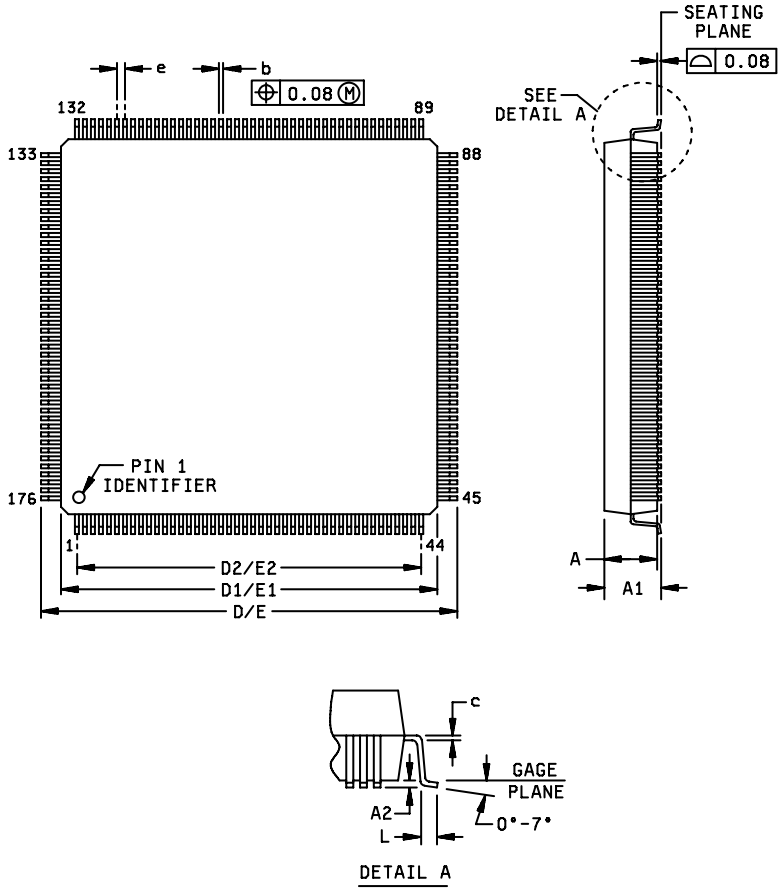
5/ All other TTL/VCMOS pins.

6/ In this case, pci_xx refers to the following signals; pci_ad31-0, , pci_par, $\overline{\text{pci_frame}}$, $\overline{\text{pci_irdy}}$, $\overline{\text{pci_trdy}}$, $\overline{\text{pci_devsel}}$, $\overline{\text{pci_stop}}$, $\overline{\text{pci_idsel}}$, $\overline{\text{pci_perr}}$, $\overline{\text{pci_serr}}$, $\overline{\text{pci_req}}$.

7/ In this case, phy_xx refers to the following bidirectional signals; phy_ctl1-0, phy_data7-0.

8/ These signals are asserted asynchronously when a ZOOM port transfer immediately preceeds the local bus transfer. In all cases, the setup time to aux_we1 and aux_we0 and the number of wait states remains the same.

Case X



Millimeters					
Symbol	Min	Max	Symbol	Min	Max
A	1.35	1.45	D/E	25.80	26.20
A1		1.60	D1/E1	23.80	24.20
A2	0.05		D2/E2	21.50 TYP	
b	0.17	0.27	e	0.50 BSC	
c	0.13 nom		L	0.45	0.75

Notes:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Fall within JEDEC MO-136

FIGURE 1. Case outlines.

Case outline X

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	3.3V_V_{CC}	31	$\overline{\text{pci_serr}}$	61	$\overline{\text{aux_int}}$	91	aux_data4
2	NC	32	pci_par	62	$\overline{\text{aux_rdy}}$	92	aux_data3
3	pci_ad25	33	3.3V_V_{CC}	63	5V_V_{CC}	93	3.3V_V_{CC}
4	pci_ad24	34	$\overline{\text{pci_cbe1}}$	64	aux_clk	94	aux_data2
5	$\overline{\text{pci_cbe3}}$	35	GND	65	GND	95	GND
6	GND	36	pci_ad15	66	$\overline{\text{aux_rst}}$	96	aux_data1
7	pci_idselz	37	pci_ad14	67	$\overline{\text{ram_cs}}$	97	aux_data0
8	3.3V_V_{CC}	38	pci_ad13	68	$\overline{\text{rom_cs}}$	98	aux_adr15
9	pci_ad23	39	pci_ad12	69	$\overline{\text{aux_cs}}$	99	aux_adr14
10	pci_ad22	40	5V_V_{CC}	70	3.3V_V_{CC}	100	3.3V_V_{CC}
11	pci_ad21	41	pci_ad11	71	$\overline{\text{aux_we1}}$	101	aux_adr13
12	5V_V_{CC}	42	3.3V_V_{CC}	72	GND	102	GND
13	pci_ad20	43	pci_ad10	73	$\overline{\text{aux_we0}}$	103	aux_adr12
14	GND	44	pci_ad9	74	$\overline{\text{aux_oe}}$	104	aux_adr11
15	pci_ad19	45	GND	75	3.3V_V_{CC}	105	aux_adr10
16	pci_ad18	46	NC	76	aux_data15	106	aux_adr9
17	pci_ad17	47	pci_ad8	77	aux_data14	107	3.3V_V_{CC}
18	pci_ad16	48	$\overline{\text{pci_cbe0}}$	78	aux_data13	108	aux_adr8
19	3.3V_V_{CC}	49	3.3V_V_{CC}	79	GND	109	5V_V_{CC}
20	$\overline{\text{pci_cbe2}}$	50	pci_ad7	80	aux_data12	110	aux_adr7
21	GND	51	GND	81	aux_data11	111	aux_adr6
22	$\overline{\text{pci_frame}}$	52	pci_ad6	82	aux_data10	112	aux_adr5
23	$\overline{\text{pci_irdy}}$	53	pci_ad5	83	aux_data9	113	aux_adr4
24	$\overline{\text{pci_trdy}}$	54	pci_ad4	84	5V_V_{CC}	114	GND
25	$\overline{\text{pci_devsel}}$	55	pci_ad3	85	aux_data8	115	aux_adr3
26	3.3V_V_{CC}	56	3.3V_V_{CC}	86	3.3V_V_{CC}	116	3.3V_V_{CC}
27	$\overline{\text{pci_stop}}$	57	pci_ad2	87	aux_data7	117	aux_adr2
28	GND	58	pci_ad1	88	aux_data6	118	aux_adr1
29	NC	59	pci_ad0	89	GND	119	aux_adr0
30	$\overline{\text{pci_perr}}$	60	5V_V_{CC}	90	aux_data5	120	NC

NC = No connection

FIGURE 2. Terminal connections.

Case outline X - Continued

Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
121	GND	135	5V_V_{CC}	149	phy_data3	163	$\overline{\text{pci_reset}}$
122	gpio_data3	136	3.3V_V_{CC}	150	GND	164	$\overline{\text{pci_gnt}}$
123	gpio_data2	137	link_cyclein	151	phy_data4	165	3.3V_V_{CC}
124	gpio_data1	138	3.3V_V_{CC}	152	phy_data5	166	$\overline{\text{pci_int a}}$
125	gpio_data0	139	link_cycleout	153	phy_data6	167	$\overline{\text{pci_req}}$
126	zv_pix_clk	140	test_out	154	phy_data7	168	GND
127	zv_vsync	141	GND	155	GND	169	pci_ad31
128	3.3V_V_{CC}	142	phy_ctl0	156	phy_clk50	170	pci_ad30
129	zv_ext_clk	143	phy_ctl1	157	3.3V_V_{CC}	171	pci_ad29
130	GND	144	phy_lreq	158	GND	172	3.3V_V_{CC}
131	zv_hsync	145	3.3V_V_{CC}	159	autoboot	173	pci_ad28
132	zv_data_valid	146	phy_data0	160	GND	174	pci_ad27
133	seeprom_clk	147	phy_data1	161	pci_clk	175	GND
134	seeprom_data	148	phy_data2	162	5V_V_{CC}	176	pci_ad26

NC = No connection

FIGURE 2. Terminal connections - Continued.

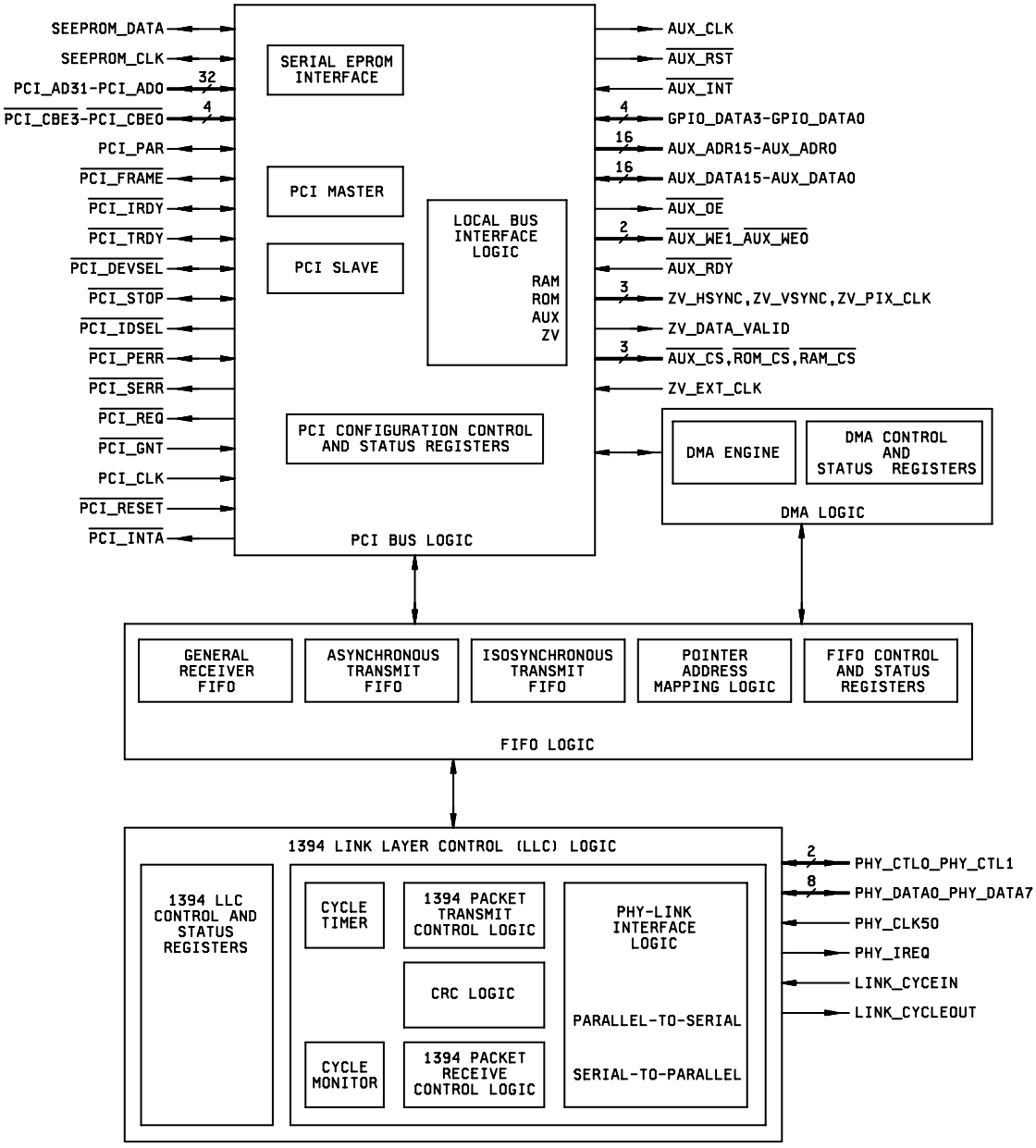
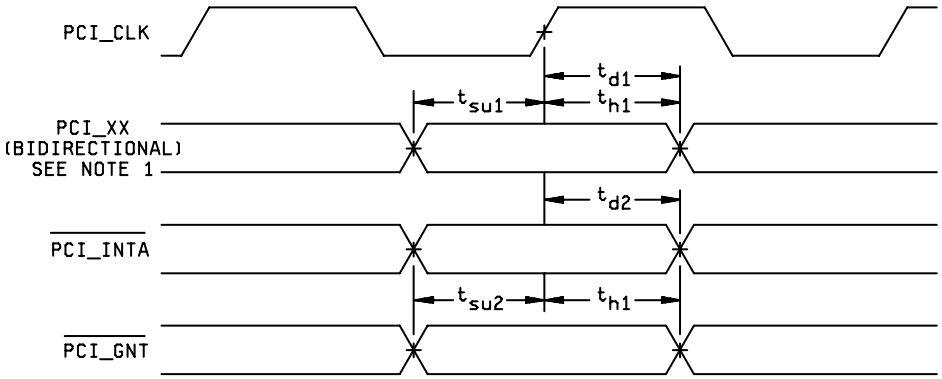


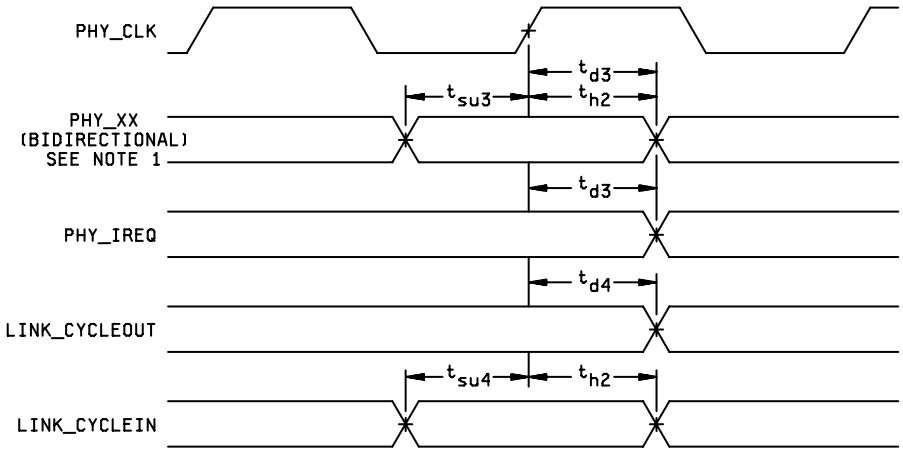
FIGURE 3. Block diagram.



NOTE:

1. In this case, pci_xx refers to the following signals; pci_ad31-0, , pci_par, $\overline{\text{pci_frame}}$, $\overline{\text{pci_irdy}}$, $\overline{\text{pci_trdy}}$, $\overline{\text{pci_devsel}}$, $\overline{\text{pci_stop}}$, $\overline{\text{pci_idsel}}$, $\overline{\text{pci_perr}}$, $\overline{\text{pci_serr}}$, $\overline{\text{pci_req}}$.

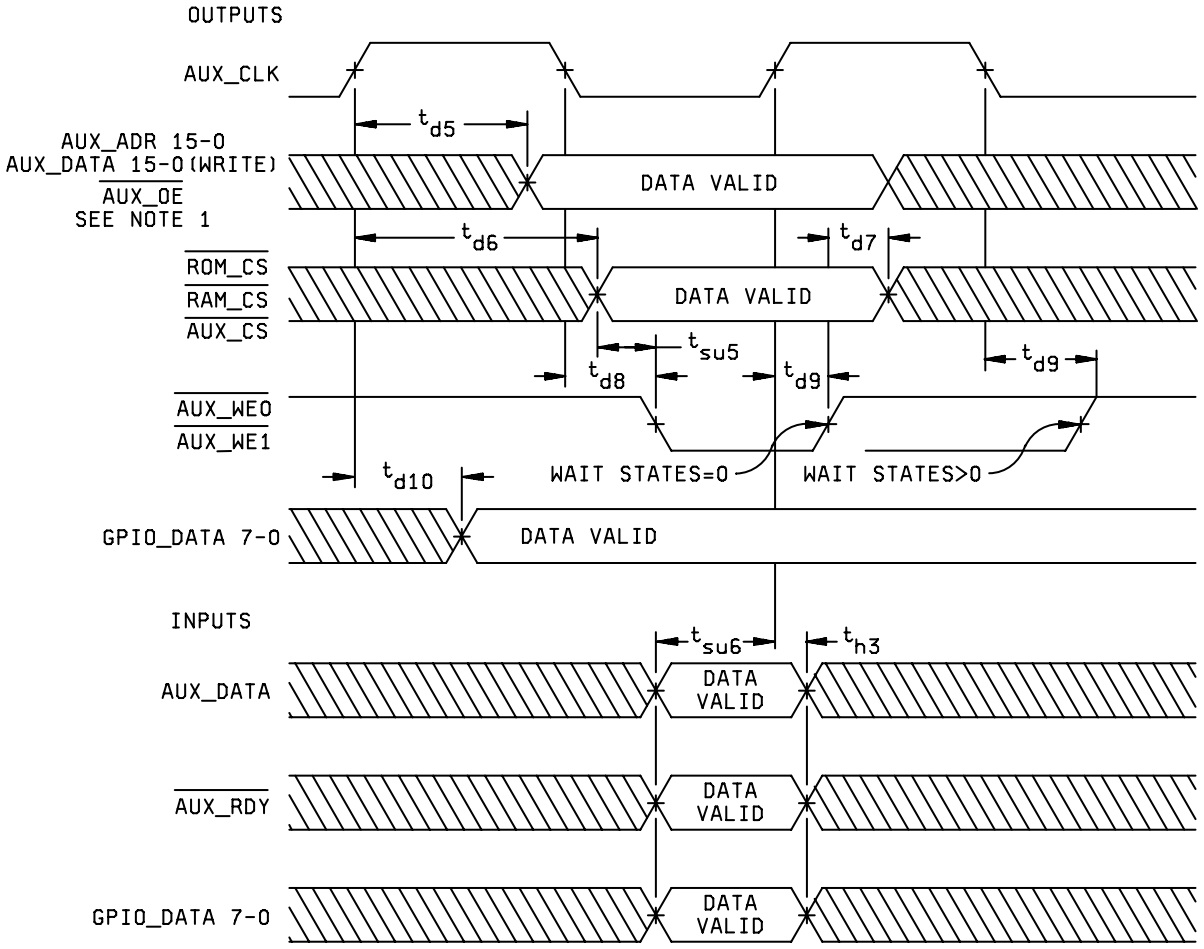
FIGURE 4. PCI interface timing waveforms.



NOTE:

1. In this case, phy_xx refers to the following bidirectional signals; phy_ctl1-0, phy_data7-0.

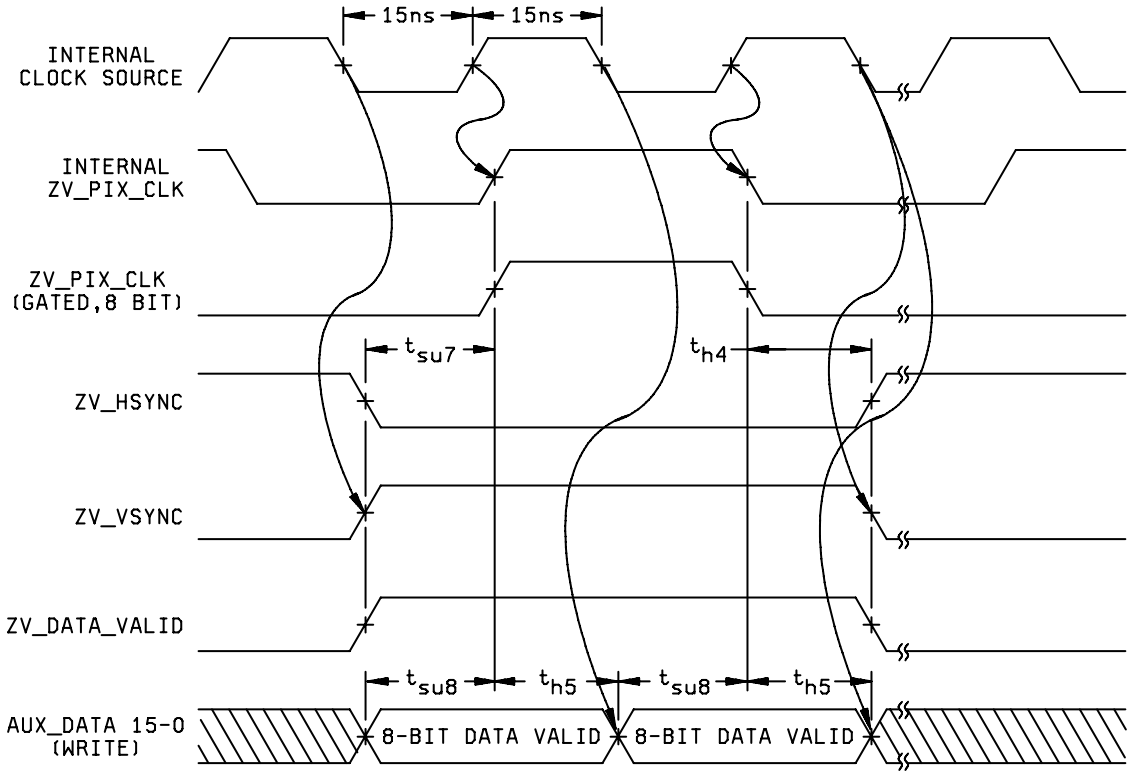
FIGURE 5. Phy-Lin interface timing waveforms.



NOTE:

1. These signals are asserted asynchronously when a ZOOM port transfer immediately preceeds the local bus transfer. In all cases, the setup time to $\overline{\text{aux_we}}$ and the number of wait states remains valid.

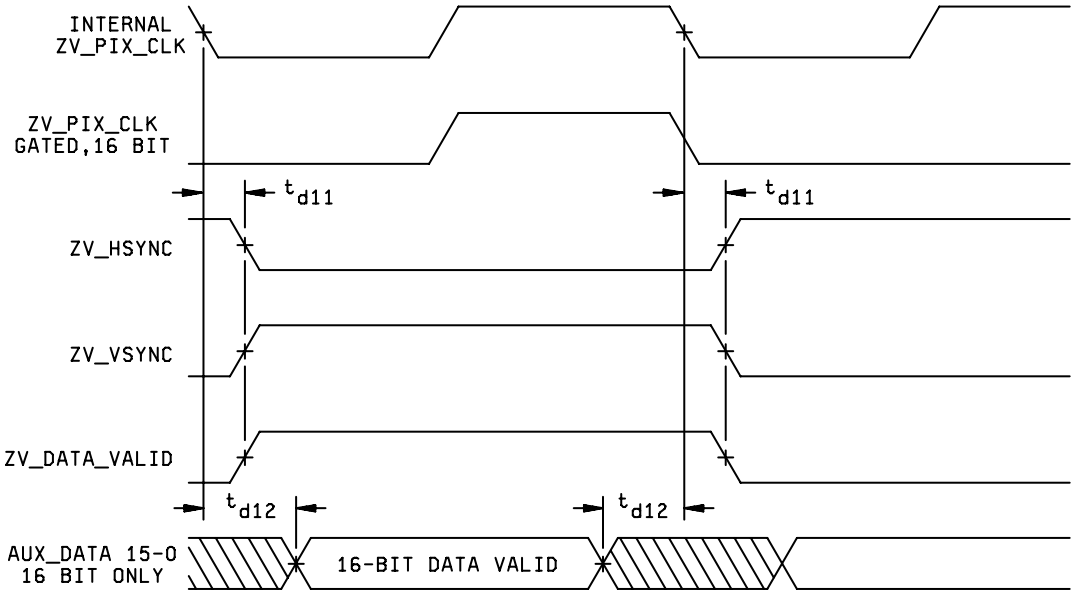
FIGURE 6 Local bus timing waveforms.



NOTE:

1. The data is in 8-bit mode and zv_pix_clk is in divide-by-2 mode.
2. The timing for these waveforms is for write access to zoom address space.
3. The aux_datax signal meets timing while the zv_data_valid signal is asserted. The aux_datax signal can be asynchronous to zv_pix_clk at other times.
4. The polarity of zv_pix_clk depends on the setting of the invert_zv_clk register bit. The polarity shown in this figure is with invert_zv_clk=0.
5. The timing for these waveforms is with a 30 ns source clock and a 50/50 duty cycle.

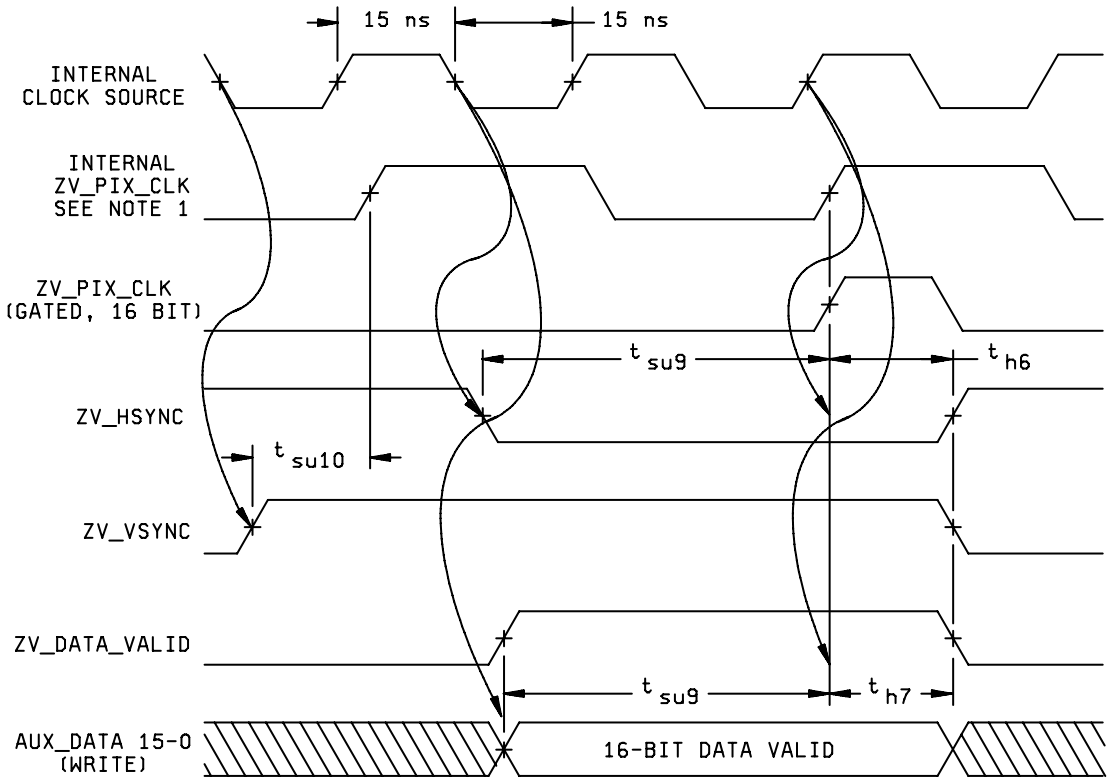
FIGURE 7 Zoom video IF timing waveforms (8 bit, divide-by-2 mode).



NOTE:

1. The data is in 16-bit mode and zv_pix_clk is in divide-by-1 mode.
2. The timing for these waveforms is for write access to zoom address space.
3. The aux_datax signal meets timing while the zv_data_valid signal is asserted. The aux_datax signal can be asynchronous to zv_pix_clk at other times.
4. The polarity of zv_pix_clk depends on the setting of the invert_zv_clk register bit. The polarity shown in this figure is with invert_zv_clk=0.

FIGURE 8 Zoom video IF timing waveforms (16 bit, divide-by-1 mode).



NOTE:

1. The data is in 16-bit mode and zv_pix_clk is in divide-by-2 mode.
2. The timing for these waveforms is for write access to zoom address space.
3. The aux_datax signal meets timing while the zv_data_valid signal is asserted. The aux_datax signal can be asynchronous to zv_pix_clk at other times.
4. The polarity of zv_pix_clk depends on the setting of the invert_zv_clk register bit. The polarity shown in this figure is with invert_zv_clk=0.
5. The timing for these waveforms is with a 30 ns source clock and a 50/50 duty cycle.

FIGURE 9 Zoom video IF timing waveforms (16 bit, divide-by-2 mode).

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/08625-01XE	01295	TSB12LV21BMPGFEP	12LV21BMPGFEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493