REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Add two columns and two footnotes under paragraph 6.3. Update document paragraphs to current requirements. - ro	16-07-07	C. SAFFLE

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** RAJESH PITHADIA	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 09-07-29	**CHECKED BY** RAJESH PITHADIA **APPROVED BY** CHARLES F. SAFFLE	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, 12 BIT, SERIAL, ANALOG-TO-DIGITAL CONVERTER WITH INTERNAL REFERENCE, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/08622**
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a 12-bit, serial, analog-to-digital converter with internal reference, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/08622	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TLV2556-EP	12-bit, serial, analog-to-digital converter with internal reference

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	MO-153	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC})	-0.5 V to 6.5 V
Input voltage range (V_{IN}) (any input)	-0.3 V to V_{CC} + 0.3 V
Output voltage range (V_{OUT})	-0.3 V to V_{CC} + 0.3 V
Positive reference voltage range (V_{REF+})	-0.3 V to V_{CC} + 0.3 V
Negative reference voltage range (V_{REF-})	-0.3 V to V_{CC} + 0.3 V
Peak input current (I_I) (any input)	±20 mA
Peak total input current (all inputs)	±30 mA
Operating virtual junction temperature range (T_J)	-55°C to 150°C
Operating free-air temperature range (T_A)	-55°C to 125°C
Storage temperature range (T_{STG})	-65°C to 150°C
Lead temperature (1.6 mm, at distance 1/16 inch from case for 10 seconds)	260°C

1.4 Recommended operating conditions. 3/

Supply voltage (V_{CC})	2.7 V min to 5.5 V max
SCLK frequency:	
V_{CC} = 4.5 V to 5.5 V, 16 bit I/O	0.01 MHz min to 15 MHz max
V_{CC} = 4.5 V to 5.5 V, 12 bit I/O	0.01 MHz min to 15 MHz max
V_{CC} = 4.5 V to 5.5 V, 8 bit I/O	0.01 MHz min to 15 MHz max
V_{CC} = 2.7 V to 3.6 V	0.01 MHz min to 10 MHz max
Tolerable clock jitter, I/O CLOCK, V_{CC} = 4.5 V to 5.5 V	0.38 ns max
Aperature jitter, V_{CC} = 4.5 V to 5.5 V	100 ps nominal
Analog input voltage : 4/	
V_{CC} = 4.5 V to 5.5 V	0 V min to (REF+) – (REF-) V max
V_{CC} = 3 V to 3.6 V	0 V min to (REF+) – (REF-) V max
V_{CC} = 2.7 V to 3 V	0 V min to (REF+) – (REF-) V max
High level control input voltage (V_{IH}):	
V_{CC} = 4.5 V to 5.5 V	2 V min
V_{CC} = 2.7 V to 3.6 V	2.1 V min
Low level control input voltage (V_{IH}):	
V_{CC} = 4.5 V to 5.5 V	0.8 V max
V_{CC} = 2.7 V to 3.6 V	0.6 V max
Operating free-air temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Unless otherwise specified, all voltage values are with respect to the GND terminal with REF- and GND wired together.
3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
4/ Analog input voltages greater than the voltage applied to REF+ convert as all ones (111111111111), while input voltages less than the voltage applied to REF- convert as all zeros (000000000000).

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -1.6 mA V_{CC} = 2.7 V, I_{OH} = -0.2 mA 30 pF	-55°C to +125°C	01	2.4		V
		V_{CC} = 4.5 V, I_{OH} = -20 µA V_{CC} = 2.7 V, I_{OH} = -20 µA 30 pF			V_{CC} – 0.1		
Low level output voltage	V_{OL}	V_{CC} = 5.5 V, I_{OL} = 1.6 mA V_{CC} = 3.6 V, I_{OL} = 0.8 mA 30 pF	-55°C to +125°C	01		0.4	V
		V_{CC} =5.5 V, I_{OL} = -20 µA V_{CC} = 3.6 V, I_{OL} = -20 µA 30 pF				0.1	
High impedance off state output current	I_{OZ}	V_{OUT} = V_{CC}, $\overline{CS}$ = V_{CC}	-55°C to +125°C	01		2.5	µA
		V_{OUT} = 0 V, $\overline{CS}$ = V_{CC}				-2.5	
Operating supply current	I_{CC}	$\overline{CS}$ at 0 V, external reference, V_{CC} = 5 V	-55°C to +125°C	01		1.2	mA
		$\overline{CS}$ at 0 V, external reference, V_{CC} = 2.7 V				0.9	
		$\overline{CS}$ at 0 V, internal reference, V_{CC} = 5 V				3	
		$\overline{CS}$ at 0 V, internal reference, V_{CC} = 2.7 V				2.4	
Software power down current	$I_{CC(SPD)}$	For all digital inputs, 0 V ≤ V_{IN} ≤ 0.5 V or V_{IN} ≥ V_{CC} – 0.5 V, SCLK = 0 V, external reference	-55°C to +125°C	01		10	µA
		For all digital inputs, 0 V ≤ V_{IN} ≤ 0.5 V or V_{IN} ≥ V_{CC} – 0.5 V, SCLK = 0 V, internal reference				10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Auto power down current	$I_{CC(APD)}$	For all digital inputs, 0 V ≤ V_{IN} ≤ 0.5 V or V_{IN} ≥ V_{CC} – 0.5 V, SCLK = 0 V, external reference	-55°C to +125°C	01		10	µA
		For all digital inputs, 0 V ≤ V_{IN} ≤ 0.5 V or V_{IN} ≥ V_{CC} – 0.5 V, SCLK = 0 V, internal reference				1800	
High level input current	I_{IH}	V_{IN} = V_{CC}	-55°C to +125°C	01		2.5	µA
Low level input current	I_{IL}	V_{IN} = 0 V	-55°C to +125°C	01		-2.5	µA
Selected channel leakage current	I_{IKG}	Selected channel at V_{CC}, Unselected channel at 0 V	-55°C to +125°C	01		1	µA
		Selected channel at 0 V, Unselected channel at V_{CC}				-1	
Internal oscillator frequency	$f_{(OSC)}$	V_{CC} = 4.5 V to 5.5 V	-55°C to +125°C	01	3.0		MHz
		V_{CC} = 2.7 V to 3.6 V			2.1		
Conversion time = 13.5 x $f_{(OSC)}$ + 25 ns	t_{conv}	V_{CC} = 4.5 V to 5.5 V	-55°C to +125°C	01		4.53	µs
		V_{CC} = 2.7 V to 3.6 V				6.46	
Internal oscillator frequency switch-over voltage			+25°C	01	3.9 typical		V
Analog input MUX 3/ impedance	Z_i	V_{CC} = 4.5 V	+25°C	01	600 typical		Ω
		V_{CC} = 2.7 V			500 typical		
Input capacitance	C_{IN}	Analog inputs	+25°C	01	45 typical		pF
		Control inputs			5 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
External reference section 4/							
Reference input voltage	REF-	V_{CC} = 4.5 V to 5.5 V	-55°C to +125°C	01	-0.1	0.1	V
		V_{CC} = 2.7 V to 3.6 V			-0.1	0.1	
Reference input voltage	REF+	V_{CC} = 4.5 V to 5.5 V	-55°C to +125°C	01	2	V_{CC}	V
		V_{CC} = 2.7 V to 3.6 V			2	V_{CC}	
External reference input voltage difference	(REF+) – (REF-)	V_{CC} = 4.5 V to 5.5 V	-55°C to +125°C	01	1.9	V_{CC}	V
		V_{CC} = 2.7 V to 3.6 V			1.9	V_{CC}	
External reference supply current		$\overline{CS}$ = 0 V, V_{CC} = 4.5 V to 5.5 V	-55°C to +125°C	01		1	mA
		$\overline{CS}$ = 0 V, V_{CC} = 2.7 V to 3.6 V				0.7	
Reference input impedance		V_{CC} = 5 V, static	+25°C	01	1 typical		MΩ
		V_{CC} = 5 V, during sampling/conversion			9 typical		kΩ
		V_{CC} = 2.7 V, static			1 typical		MΩ
		V_{CC} = 2.7 V, during sampling/conversion			9 typical		kΩ
Internal reference section 5/							
Reference input voltage	REF-	V_{CC} = 2.7 V to 5.5 V, REF- = Analog GND	+25°C	01	0 typical		V
Internal reference voltage difference	(REF+) – (REF-)	V_{CC} = 5.5 V, Internal 4.096-V V_{REF} selected	-55°C to +125°C	01	3.95	4.25	V
		V_{CC} = 5.5 V, Internal 2.048-V V_{REF} selected			1.94	2.15	
		V_{CC} = 2.7 V, Internal 2.048-V V_{REF} selected			1.94	2.15	
Internal reference start up time		V_{CC} = 5 V, with 10 μF load	+25°C	01	20 typical		ms
		V_{CC} = 2.7 V, with 10 μF load			20 typical		
Internal reference temperature coefficient		V_{CC} = 2.7 V to 5.5 V	+25°C	01	±50 typical		ppm/°C

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Operating characteristics.							
Integral nonlinearity error 6/	INL		-55°C to +125°C	01	-1	1	LSB
Differential nonlinearity error	DNL		-55°C to +125°C	01	-1	1	LSB
Offset error 7/ 8/	E_O		-55°C to +125°C	01	-2	2	mV
Gain error 7/ 8/	E_G		-55°C to +125°C	01	-3	3	mV
Total unadjusted error 9/	E_T		+25°C	01	±1.5 typical		LSB
Self test output code 10/		Address data input = 1011	+25°C	01	2048 typical		
		Address data input = 1100			0 typical		
		Address data input = 1101			4095 typical		
Timing characteristics.							
Pulse duration I/O CLOCK high or low 11/	t_{w1}	12/	-40°C to +85°C	01	26.7	100000	ns
Setup time DATA IN valid before I/O CLOCK rising edge 11/	t_{su1}	See figure 4 12/	-40°C to +85°C	01	12		ns
Hold time DATA IN valid after I/O CLOCK rising edge 11/	t_{h1}	See figure 4 12/	-40°C to +85°C	01	0		ns
Setup time $\overline{CS}$ low before 1st rising I/O CLOCK edge 11/ 13/	t_{su2}	See figure 5 12/	-40°C to +85°C	01	25		ns
Hold time $\overline{CS}$ pulse duration high time 11/	t_{h2}	See figure 5 12/	-40°C to +85°C	01	100		ns
Hold time $\overline{CS}$ low after last I/O CLOCK falling edge 11/	t_{h3}	See figure 5 12/	-40°C to +85°C	01	0		ns
Hold time DATA OUT valid after I/O CLOCK falling edge 11/	t_{h4}	See figure 6 12/	-40°C to +85°C	01	2		ns
Hold time $\overline{CS}$ high after EOC rising edge when $\overline{CS}$ is toggled 11/	t_{h5}	See figure 7 12/	-40°C to +85°C	01	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 12/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing characteristics - continued.							
Hold time $\overline{CS}$ high after $\overline{INT}$ falling edge 11/	t_{h6}	See figure 7 12/	-40°C to +85°C	01	0		ns
Hold time I/O CLOCK low after EOC rising edge or $\overline{INT}$ falling edge when $\overline{CS}$ is held low 11/	t_{h7}	See figure 8	-40°C to +85°C	01	10		ns
Delay time $\overline{CS}$ falling edge to DATA OUT valid (MSB or LSB) 11/	t_{d1}	Load = 25 pF, see figure 9	-40°C to +85°C	01		28	ns
		Load = 10 pF, see figure 9	-40°C to +85°C	01		20	
Delay time $\overline{CS}$ rising edge to DATA OUT high impedance 11/	t_{d2}	See figure 9	-40°C to +85°C	01		10	ns
Delay time I/O CLOCK falling edge to next DATA OUT bit valid 11/	t_{d3}	See figure 6	-40°C to +85°C	01	2	20	ns
Delay time last I/O CLOCK falling edge to EOC falling edge 11/	t_{d4}	See figure 10	-40°C to +85°C	01		55	ns
Delay time last I/O CLOCK falling edge to $\overline{CS}$ falling edge to abort conversion 11/	t_{d5}		-40°C to +85°C	01		1.5	µs
Delay time last I/O CLOCK falling edge to $\overline{INT}$ falling edge 11/	t_{d6}	See figure 10	-40°C to +85°C	01		MAX(t_{conv})	ns
Delay time EOC rising edge or $\overline{INT}$ falling edge to DATA OUT valid: MSB or LSB first 11/	t_{d7}	See figure 11	-40°C to +85°C	01		4	ns
Delay time I/O CLOCK high to $\overline{INT}$ rising edge when $\overline{CS}$ is held low 11/	t_{d9}	See figure 8	-40°C to +85°C	01	1	28	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 12/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing characteristics - continued.							
Transition time I/O CLOCK 11/ 13/	t_{t1}	See figure 6	-40°C to +85°C	01		1	µs
Transition time DATA OUT 11/	t_{t2}	See figure 6	-40°C to +85°C	01		5	ns
Transition time $\overline{INT}$/EOC, C_L = 7 pF 11/	t_{t3}	See figures 10 and 11	-40°C to +85°C	01		2.4	ns
Transition time DATA IN, $\overline{CS}$ 11/	t_{t4}		-40°C to +85°C	01		10	µs
Total cycle time (sample, conversion and delays) 11/ 13/	t_{cyc}		-40°C to +85°C	01		MAX(t_{conv}) + I/O period (8/12/16 CLKs)	µs
Channel acquisition time (sample), at 1 kΩ 11/ 13/	t_{sample}	Source impedance = 25 Ω	-40°C to +85°C	01	600		ns
		Source impedance = 100 Ω		01	650		
		Source impedance = 500 Ω		01	700		
		Source impedance = 1 kΩ		01	1000		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 14/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing characteristics - continued.							
Pulse duration I/O CLOCK high or low 11/	t_{w1}		-40°C to +85°C	01	40	100000	ns
Setup time DATA IN valid before I/O CLOCK rising edge 11/	t_{su1}	See figure 4	-40°C to +85°C	01	22		ns
Hold time DATA IN valid after I/O CLOCK rising edge 11/	t_{h1}	See figure 4	-40°C to +85°C	01	0		ns
Setup time $\overline{CS}$ low before 1st rising I/O CLOCK edge 11/ 13/	t_{su2}	See figure 5	-40°C to +85°C	01	33		ns
Hold time $\overline{CS}$ pulse duration high time 11/	t_{h2}	See figure 5	-40°C to +85°C	01	100		ns
Hold time $\overline{CS}$ low after last I/O CLOCK falling edge 11/	t_{h3}	See figure 5	-40°C to +85°C	01	0		ns
Hold time DATA OUT valid after I/O CLOCK falling edge 11/	t_{h4}	See figure 6	-40°C to +85°C	01	2		ns
Hold time $\overline{CS}$ high after EOC rising edge when $\overline{CS}$ is toggled 11/	t_{h5}	See figure 7	-40°C to +85°C	01	0		ns
Hold time $\overline{CS}$ high after $\overline{INT}$ falling edge 11/	t_{h6}	See figure 7	-40°C to +85°C	01	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 14/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing characteristics - continued.							
Hold time I/O CLOCK low after EOC rising edge or $\overline{INT}$ falling edge when $\overline{CS}$ is held low 11/	t_{h7}	See figure 8	-40°C to +85°C	01	10		ns
Delay time $\overline{CS}$ falling edge to DATA OUT valid (MSB or LSB) 11/	t_{d1}	Load = 25 pF, see figure 9	-40°C to +85°C	01		30	ns
		Load = 10 pF, see figure 9	-40°C to +85°C	01		22	
Delay time $\overline{CS}$ rising edge to DATA OUT high impedance 11/	t_{d2}	See figure 9	-40°C to +85°C	01		10	ns
Delay time I/O CLOCK falling edge to next DATA OUT bit valid 11/	t_{d3}	See figure 6	-40°C to +85°C	01	2	33	ns
Delay time last I/O CLOCK falling edge to EOC falling edge 11/	t_{d4}	See figure 10	-40°C to +85°C	01		75	ns
Delay time last I/O CLOCK falling edge to $\overline{CS}$ falling edge to abort conversion 11/	t_{d5}		-40°C to +85°C	01		1.5	µs
Delay time last I/O CLOCK falling edge to $\overline{INT}$ falling edge 11/	t_{d6}	See figure 10	-40°C to +85°C	01		MAX(t_{conv})	ns
Delay time EOC rising edge or $\overline{INT}$ falling edge to DATA OUT valid: MSB or LSB first 11/	t_{d7}	See figure 11	-40°C to +85°C	01		20	ns
Delay time I/O CLOCK high to $\overline{INT}$ rising edge when $\overline{CS}$ is held low 11/	t_{d9}	See figure 8	-40°C to +85°C	01	1	55	ns
Transition time I/O CLOCK 11/ 13/	t_{t1}	See figure 6	-40°C to +85°C	01		1	µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 14/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Timing characteristics - continued.							
Transition time DATA OUT 11/	t_{t2}	See figure 6	-40°C to +85°C	01		5	ns
Transition time $\overline{INT}$/EOC, C_L = 7 pF 11/	t_{t3}	See figures 10 and 11	-40°C to +85°C	01		4	ns
Transition time DATA IN, $\overline{CS}$ 11/	t_{t4}		-40°C to +85°C	01		10	µs
Total cycle time (sample, conversion and delays) 11/ 13/	t_{cyc}		-40°C to +85°C	01		MAX(t_{conv}) + I/O period (8/12/16 CLKs)	µs
Channel acquisition time (sample), at 1 kΩ 11/ 13/	t_{sample}	Source impedance = 25 Ω	-40°C to +85°C	01	800		ns
		Source impedance = 100 Ω		01	850		
		Source impedance = 500 Ω		01	1000		
		Source impedance = 1 kΩ		01	1600		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{REF+} = 5 V. SCLK frequency = 15 MHz when V_{CC} = 5 V, V_{REF+} = 2.5 V. SCLK frequency = 10 MHz when V_{CC} = 2.7 V. All typical values are at V_{CC} = 5 V.

3/ The switch resistance is very nonlinear and varies with input voltage and supply voltage.

4/ Add a 0.1 µF capacitor between REF+ and REF- pins when external reference is used.

5/ When an internal reference is used, the following conditions are required:
a. Add 0.1 µF and 10 µF capacitors between REF+ and REF- pins.
b. REF- must be connected to analog GND (the ground pin of the ADC).

TABLE I. Electrical performance characteristics - Continued.

6/ Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.

7/ Analog input voltages greater than the voltage applied to REF+ convert as all ones (111111111111), while input voltages less than the voltage applied to REF- convert as all zeros (000000000000).

8/ Gain error is the difference between the actual mid-step value and the nominal mid-step value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero. Offset error is the difference between the actual mid-step value and the nominal mid-step value at the offset point.

9/ Total unadjusted error comprises linearity, zero-scale, and full-scale errors.

10/ Both the input address and the output codes are expressed in positive logic.

11/ Timing parameters are not production tested.

12/ Unless otherwise specified, V_{REF+} = 5 V, SCLK frequency = 15 MHz, V_{CC} = 5 V, load = 25 pF.

13/ I/O CLOCK period = 8 x [1/(I/O CLOCK frequency)] or 12 x [1/(I/O CLOCK frequency)] or 16 x [1/(I/O CLOCK frequency)], depending on I/O format selected.

14/ Unless otherwise specified, V_{REF+} = 2.5 V, SCLK frequency = 10 MHz, V_{CC} = 2.7 V, load = 25 pF.

Case X

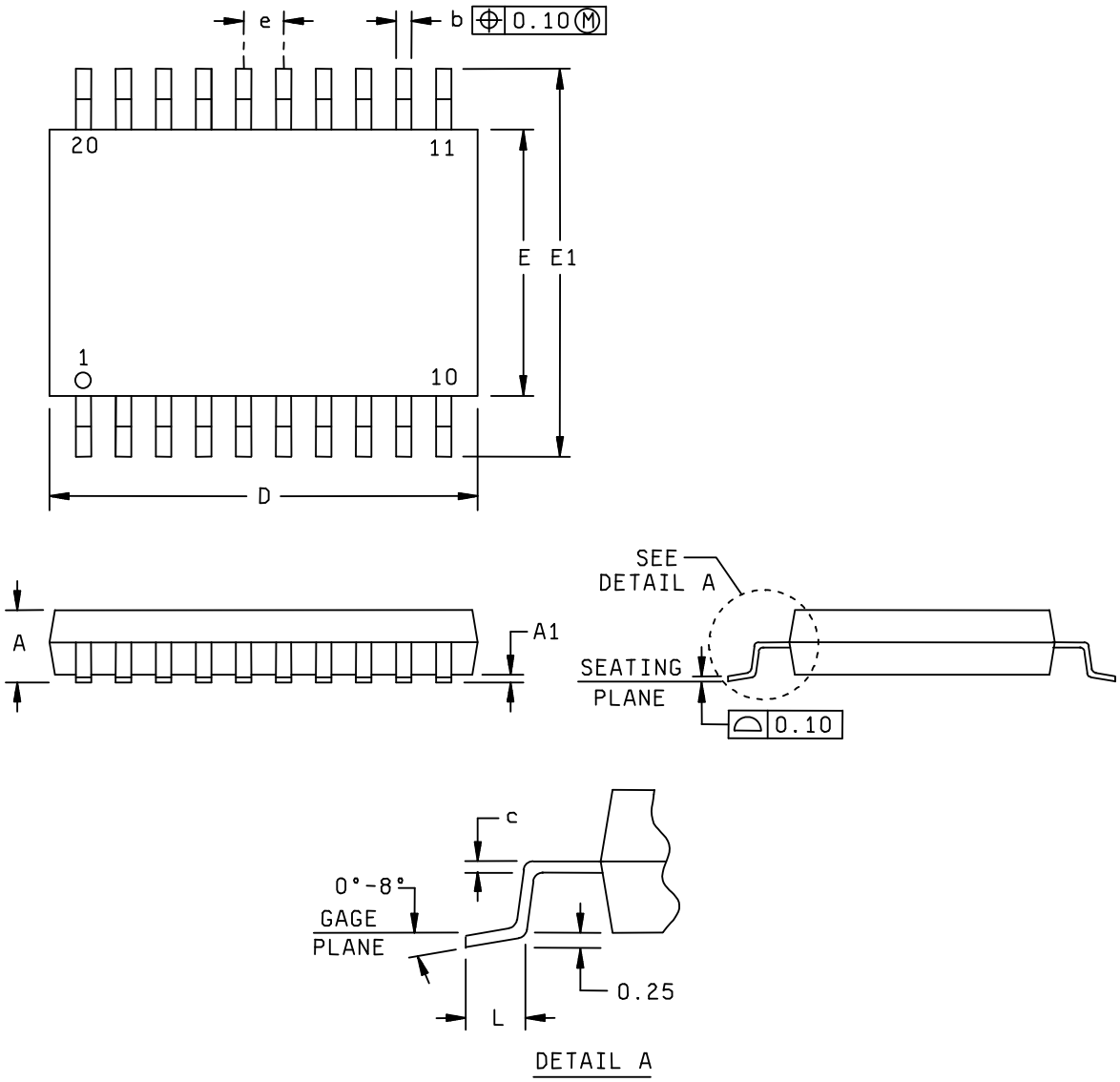

FIGURE 1. Case outlines.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE **A**	CODE IDENT NO. **16236**	DWG NO. **V62/08622**
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Case X – continued.

Symbol	Dimensions	
	Millimeters	
	Min	Max
A		1.20
A1	0.05	0.15
b	0.19	0.30
c	0.15 NOM	
D	6.40	6.60
E	4.30	4.50
E1	6.20	6.60
e	0.65 BSC	
L	0.50	0.75

NOTES:
1. All linear dimensions are in millimeters.
2. Body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. Falls within reference to JEDEC MO-153.

FIGURE 1. Case outline – continued.

Device type	01
Case outlines	X
Terminal number	Terminal symbol
1	AIN0
2	AIN1
3	AIN2
4	AIN3
5	AIN4
6	AIN5
7	AIN6
8	AIN7
9	AIN8
10	GND
11	AIN9
12	AIN10
13	REF-
14	REF+
15	$\overline{CS}$
16	DATA OUT
17	DATA IN
18	I/O CLOCK
19	$\overline{INT}$/EOC
20	V_{CC}

FIGURE 2. Terminal connections.

Terminal symbol	Terminal number	I/O	Description
AIN0-AIN10	1-9, 11, 12	I	Analog input. These 11 analog signal inputs are internally multiplexed.
$\overline{CS}$	15	I	Chip select. A high-to-low transition on $\overline{CS}$ resets the internal counters and controls and enables DATA OUT, DATA IN, and I/O CLOCK. A low-to-high transition disables DATA IN and I/O CLOCK within a setup time.
DATA IN	17	I	Serial data input. The 4 bit serial data can be used as address selects the desired analog input channel or test voltage to be converted next, or a command to activate other features. The input data is presented with the MSB (D7) first and is shifted in on the first four rising edges of the I/O CLOCK. After the four address/command bits are read into the command register CMR, I/O CLOCK clocks the remaining four bits of configuration in.
DATA OUT	16	O	The 3-state serial output for the A/D conversion result. DATA OUT is in the high impedance state when $\overline{CS}$ is high and active when $\overline{CS}$ is low. With a valid $\overline{CS}$, DATA OUT is removed from the high impedance state and is driven to the logic level corresponding to the MSB(most significant bit)/LSB(least significant bit) value of the previous conversion result. The next falling edge of I/O CLOCK drives DATA OUT to the logic level corresponding to the next MSB/LSB, and the remaining bits are shifted out in order.
$\overline{INT}$/EOC	19	O	Status output, used to indicate the end of conversion (EOC) or an interrupt ($\overline{INT}$) to host processor. Programmed as $\overline{INT}$ (interrupt): $\overline{INT}$ goes from a high to a low logic level after the conversion is complete and the data is ready for transfer. $\overline{INT}$ is cleared by a rising I/O CLOCK transition. Programmed as EOC: EOC goes from a high to a low logic level after the falling edge of the last I/O CLOCK and remains low until the conversion is complete and the data is ready for transfer.
GND	10		Ground. GND is the ground return terminal for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
I/O CLOCK	18	I	Input/output clock. I/O CLOCK receives the serial input and performs the following four functions: 1. It clocks the eight input data bits into the input data register on the first eight rising edges of I/O CLOCK with the multiplexer address available after the fourth rising edge. 2. On the fourth falling edge of I/O CLOCK, the analog input voltage on the selected multiplexer input begins charging the capacitor array and continues to do so until the last falling edge of I/O CLOCK. 3. The remaining 11 bits of the previous conversion data are shifted out on DATA OUT. Data changes on the falling edge of I/O CLOCK. 4. Control of the conversion is transferred to the internal state controller on the falling edge of the last I/O CLOCK.

FIGURE 2. Terminal connections – continued.

Terminal symbol	Terminal number	I/O	Description
REF+	14	I/O	Positive reference voltage. The upper reference voltage value (nominally V_{CC}) is applied to REF+. The maximum analog input voltage range is determined by the difference between the voltage applied to terminals REF+ and REF-. When the internal reference is used it is capable of driving a 10 kΩ, 10 pF load.
REF-	13	I/O	Negative reference voltage. The lower reference voltage value (nominally ground) is applied to REF-. This pin is connected to analog ground (GND of the ADC) when the internal reference is used.
V_{CC}	20		Positive supply voltage.

FIGURE 2. Terminal connections – continued.

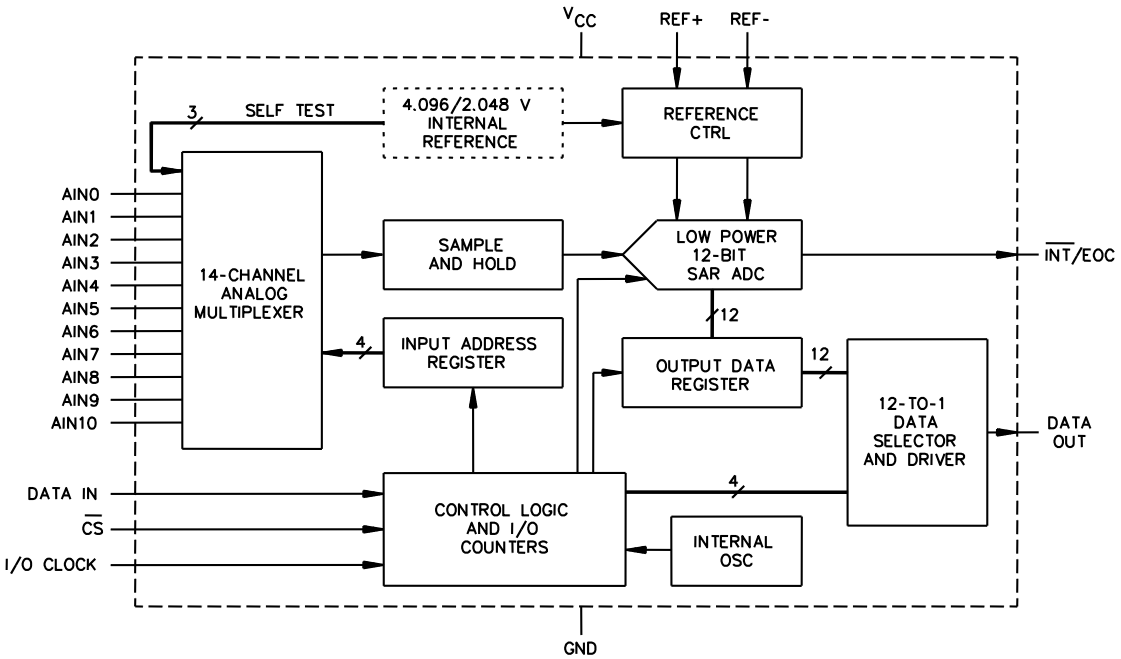

FIGURE 3. Block diagram.

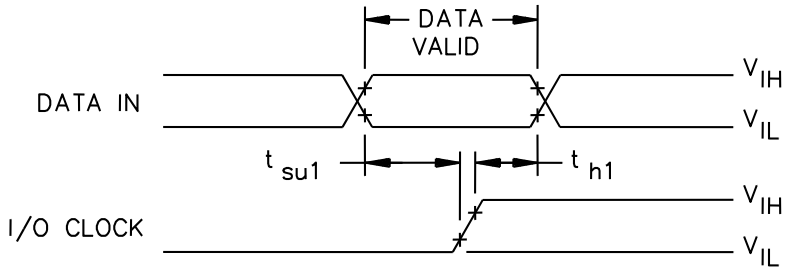

FIGURE 4. DATA IN and I/O CLOCK voltage waveforms.

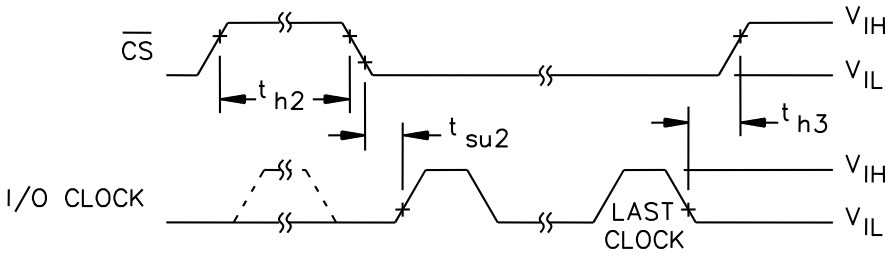

FIGURE 5. $\overline{CS}$ and I/O CLOCK voltage waveforms.

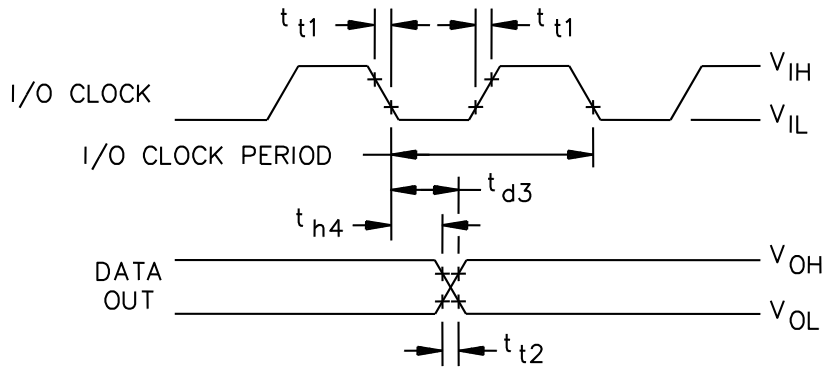

FIGURE 6. I/O CLOCK and DATA OUT voltage waveforms.

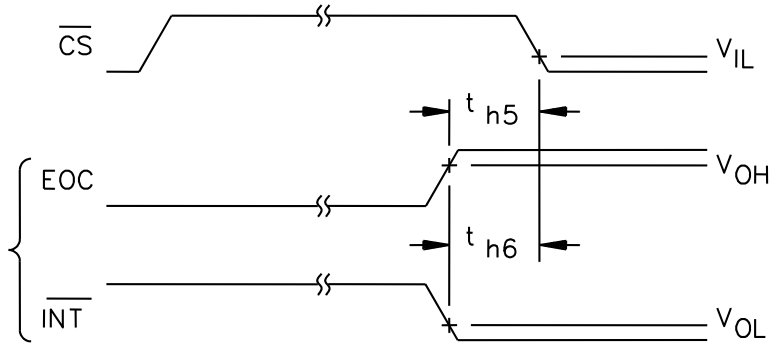

FIGURE 7. $\overline{CS}$ and EOC voltage waveforms.

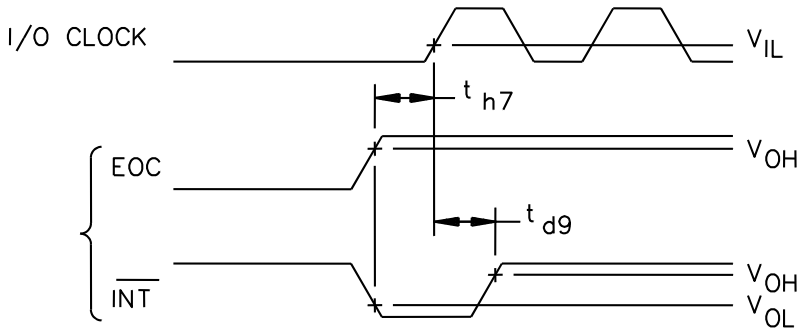

FIGURE 8. I/O CLOCK and EOC voltage waveforms.

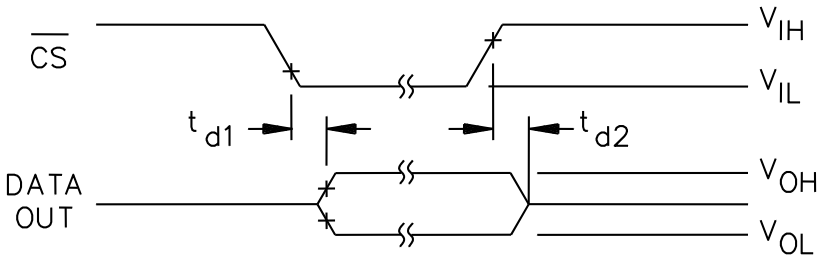

FIGURE 9. DATA OUT to Hi-Z voltage waveforms.

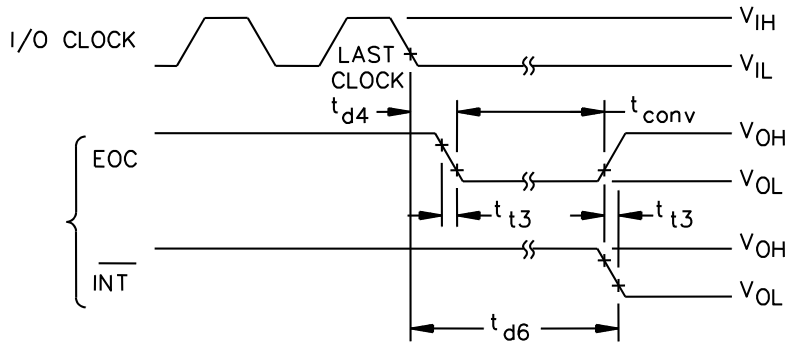

FIGURE 10. I/O CLOCK and EOC voltage waveforms.

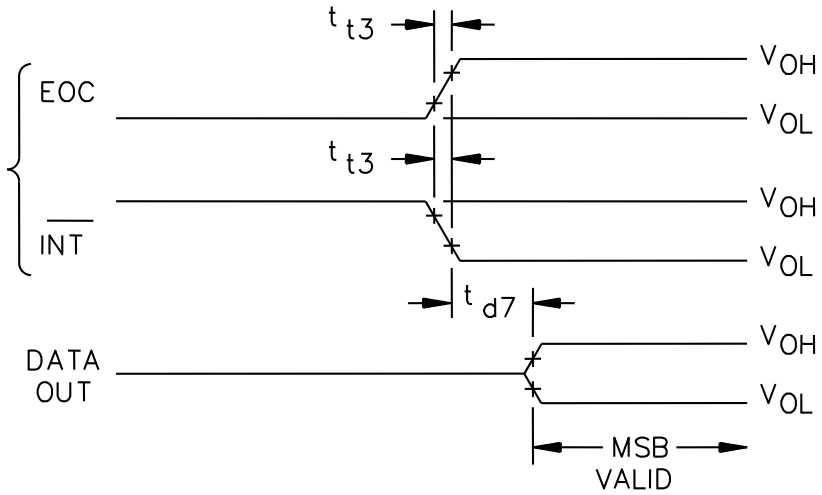

FIGURE 11. EOC and DATA OUT voltage waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Transportation mode and quantity 2/ 3/	Top side marking	Vendor part number
V62/08622-01XE	01295	Reel of 2000	TL2556EP	TLV2556MPWREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet, or from the manufacturer.

3/ Package drawings, thermal data, and symbolization are available from the manufacturer.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243