

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Delete dissipation rating table and replace with paragraph 1.5 thermal characteristics. Make changes to D/E dimensions and notes 3 and 4 under figure 1. Add top side marking, transportation and quantity columns and two footnotes to paragraph 6.3. Update document paragraphs to current requirements. - ro	15-05-27	C. SAFFLE
B	Update document paragraphs to current requirements. - ro	21-01-07	J. ESCHMEYER



CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	REV	B	B	B	B	B	B	B	B	B	B	B	B	B						
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PMIC N/A	PREPARED BY RAJESH PITHADIA	DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990
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Original date of drawing YY-MM-DD 09-07-27	CHECKED BY RAJESH PITHADIA	TITLE MICROCIRCUIT, LINEAR, DUAL, LOW DROPOUT VOLTAGE REGULATOR, MONOLITHIC SILICON
	APPROVED BY CHARLES F. SAFFLE	

SIZE A	CODE IDENT. NO. 16236	DWG NO. V62/08621
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual, low dropout, voltage regulator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/08621</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	TPS71202-EP	Dual, 250 mA output, ultra-low noise, high power supply rejection ratio, low-dropout, voltage regulator

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	10	See figure 1	Small outline, no leads

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

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1.3 Absolute maximum ratings. 1/

Input voltage range (VIN), IN pin	-0.3 V to 6 V
Input voltage range (VEN1, VEN2), EN1 and EN2 pins	-0.3 V to VIN + 0.3 V
Output voltage range (VOUT), OUT pins	-0.3 V to 6 V
Peak output current	Internally limited
Output short-circuit duration	Indefinite
Continuous total power dissipation (PD)	See 1.5 thermal characteristics
Junction temperature range (TJ)	-55°C to 150°C
Storage temperature range (TSTG)	-65°C to 150°C
Thermal resistance, junction to case (θJC):	
X package	48°C/W
Thermal resistance, junction to ambient (θJA):	
X package	52°C/W
Electrostatic discharge rating (ESD):	
Human Body Model (HBM)	2000 V
Charged Device Model (CDM)	500 V

1.4 Recommended operating conditions. 2/

Operating junction temperature range (TJ)	-55°C to +125°C
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1.5 Thermal characteristics.

Thermal metric 3/ 4/	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θJA	49.6	°C/W
Thermal resistance, junction-to-case (top)	θJC(TOP)	70.0	°C/W
Thermal resistance, junction-to-board	θJB	17.8	°C/W
Characterization parameter, junction-to-top	ψJT	0.6	°C/W
Characterization parameter, junction-to-board	ψJB	15.2	°C/W
Thermal resistance, junction-to-case (bottom)	θJC(BOTTOM)	5.2	°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

3/ See manufacturer for more information about traditional and new thermal metrics.

4/ See manufacturer for thermal estimates of this device based on printed circuit board (PCB) copper area.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T _J	Device type	Limits		Unit
					Min	Max	
Input voltage range 3/	V _{IN}		-55°C to +125°C	01	2.7	5.5	V
Internal reference (adjustable LDOs)	V _{FB}		-55°C to +125°C	01	1.200	1.250	V
Output voltage range (adjustable LDOs)	V _{OUT}		-55°C to +125°C	01	V _{FB}	5.5 - V _D O	V
Accuracy (nominal) 3/		I _{OUT} = 0 mA	+25°C		-1.5	+1.5	%
Accuracy (over V _{IN} , I _{OUT} , and temperature) 3/		V _{OUT} + 1.0 V ≤ V _{IN} ≤ 5.5 V, 0 μA ≤ I _{OUT} ≤ 250 mA	-55°C to +125°C		-3	+3	
Line regulation 3/	ΔV _{OUT} %/ ΔV _{IN}	V _{OUT} + 1.0 V ≤ V _{IN} ≤ 5.5 V	+25°C	01	0.05 typical		%/V
Load regulation	ΔV _{OUT} %/ ΔI _{OUT}	0 μA ≤ I _{OUT} ≤ 250 mA	+25°C	01	0.8 typical		%/mA
Dropout voltage (V _{IN} = V _{OUT(nom)} – 0.1 V)	V _D O	I _{OUT1} = I _{OUT2} = 250 mA	-55°C to +125°C	01		315	mV
Output current limit	I _{CL}	V _{OUT} = 0.9 x V _{OUT(nom)}	-55°C to +125°C	01	400	800	mA
Ground pin current	I _{IGND}	One LDO enabled, I _{OUT} = 1 mA (enabled channel)	-55°C to +125°C	01		250	μA
		Both LDOs enabled, I _{OUT1} = I _{OUT2} = 1 mA to 250 mA				600	
Shutdown current 4/	I _{SHDN}	V _{EN} ≤ 0.4 V, 0 V ≤ V _{IN} ≤ 5.5 V	-55°C to +125°C	01		2.0	μA
FB pin current	I _{FB}		-55°C to +125°C	01		1.50	μA
Output noise voltage, BW = 10 Hz to 100 kHz	V _n	No CNR, I _{OUT} = 250 mA	+25°C	01	80.0 x V _{OUT} typical		μV _{rms}
		CNR = 0.01 μF, I _{OUT} = 250 mA			11.8 x V _{OUT} typical		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _J	Device type	Limits		Unit
					Min	Max	
Power supply rejection ratio (ripple rejection)	PSRR	f = 100 Hz, I _{OUT} = 250 mA	+25°C	01	65 typical		dB
		f = 10 kHz, I _{OUT} = 250 mA			65 typical		
Startup time	t _{STR}	V _{OUT} = 2.85 V, R _L = 30 Ω, CNR = 0.001 μF	+25°C	01	60 typical		μs
Enable threshold high (EN1, EN2)	V _{IH}		-55°C to +125°C	01	1.2	V _{IN}	V
Enable threshold low (EN1, EN2)	V _{IL}		-55°C to +125°C	01	0	0.4	V
Enable pin current (EN1, EN2)	I _{EN}	V _{IN} = V _{EN} = 5.5 V	-55°C to +125°C	01	-1	1	μA
Thermal shutdown temperature	T _{SD}	Shutdown, temperature increasing	+25°C	01	+160 typical		°C
		Reset, temperature decreasing			+140 typical		
Undervoltage lockout threshold	UVLO	V _{IN} rising	-55°C to +125°C	01	2.25	2.65	V
Undervoltage lockout hysteresis		V _{IN} falling	+25°C		100 typical		mV

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ V_{IN} = highest (V_{OUT(nom)} + 1 V) or 2.7 V (whichever is greater), I_{OUT} = 1 mA, V_{EN1, 2} = 1.2 V, C_{OUT} = 10 μF, CNR = 0.01 μF, and adjustable LDOs are tested at V_{OUT} = 3.0 V, unless otherwise specified.

3/ Minimum V_{IN} = (V_{OUT} + V_{DO}) or 2.7 V, whichever is greater.

4/ For the adjustable version, this applies only after V_{IN} is applied; then V_{EN} transitions from high to low.

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Case X

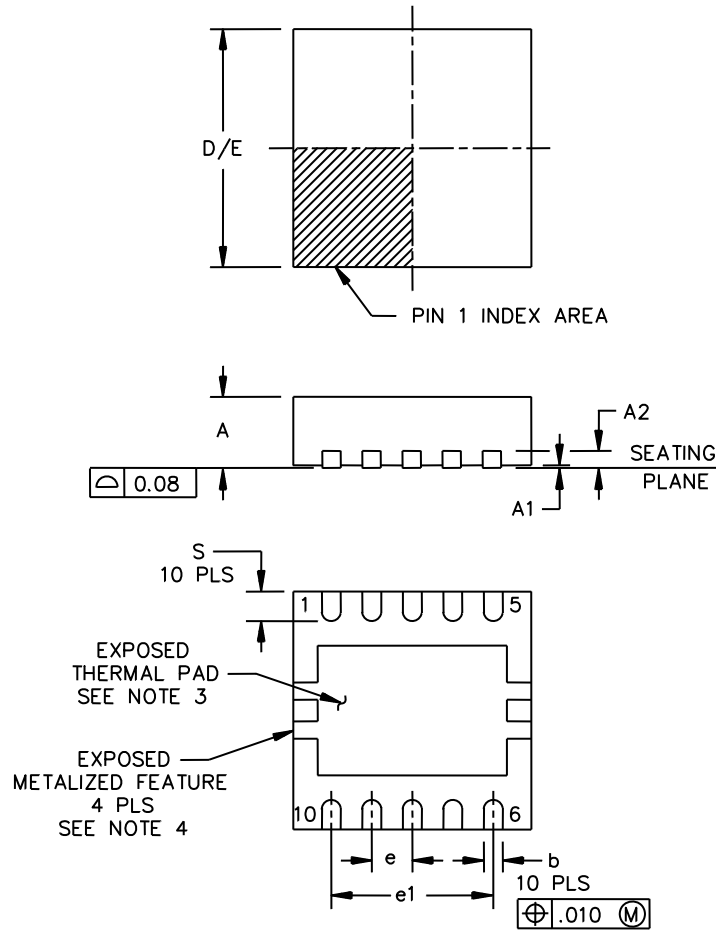


FIGURE 1. Case outline.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/08621</p>
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Case X – continued.

Symbol	Dimensions	
	Millimeters	
	Min	Max
A	0.80	1.00
A1	0.00	0.05
A2	0.20 REF	
b	0.18	0.30
D/E	2.90	3.10
e	0.50 BSC	
e1	2.00 BSC	
S	0.30	0.50

NOTES:

1. All linear dimensions are in millimeters.
2. Small outline, no-lead (SON) package configuration.
3. The package thermal pad must be soldered to the board for thermal and mechanical performance.
4. See product data sheet for details regarding the exposed thermal pad dimensions.

FIGURE 1. Case outline – Continued.

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Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	IN	Unregulated input supply. A small 0.1 μ F capacitor should be connected from IN to GND.
2	NC	No connection.
3	OUT1	Output of the regulator. A small 2.2 μ F ceramic capacitor is required from this pin to ground to assure stability.
4	OUT2	Same as OUT1 but for LDO2.
5, Pad	GND	Ground.
6	NR	Noise reduction pin; connect an external bypass capacitor to reduce LDO output noise.
7	FB2	Feedback for channel 2.
8	EN2	Same as EN1 but controls LDO2.
9	FB1	Feedback for channel 1.
10	EN1	Driving the enable pin (EN) high turns on LDO1. Driving this pin low puts LDO1 into shutdown mode, reducing operating current. The enable pin should be connected to IN if not used.

FIGURE 2. Terminal connections.

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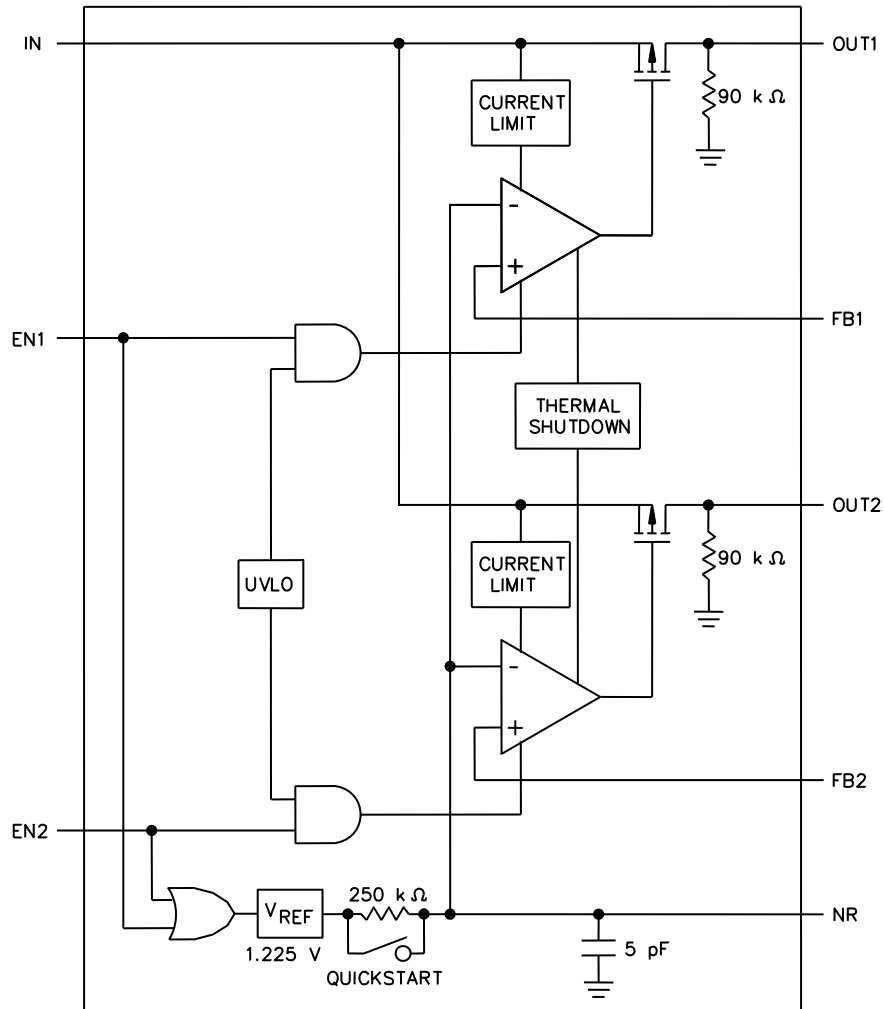


FIGURE 3. Block diagram.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/08621</p>
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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/ 2/</u>	Device manufacturer CAGE code	Transportation and quantity <u>3/</u>	Top side marking	Vendor part number
V62/08621-01XE	01295	Reel of 250	CVQ	TPS71202MDRCTEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet.

3/ Package drawings, thermal data, and symbolization are available from the manufacturer.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243

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