REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update document paragraphs to current requirements. - jwc	15-06-24	Thomas M. Hess

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**		A	A	A	A	A	A	A	A	A	A	A								
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PMIC N/A	**PREPARED BY** Muhammad A. Akbar	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO 43218 - 3990**
Original date of drawing YY - MM - DD 09-08-10	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, DIGITAL, SINGLE POSITIVE EDGE TRIGGRERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/08617**
	REV A	PAGE 1 OF 11

AMSC N/A

5962-V060-15

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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance single positive edge triggered D-type flip-flop with clear and preset microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/08617	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74LVC2G74-EP	Single positive edge triggered D-type flip-flop with clear and preset.

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	8	MO-187	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.5 V to +6.5 V
Input voltage range (V_i) ..... -0.5 V to +6.5 V 2/
Voltage range applied to any output in high-impedance or power-off state (V_O) ..... -0.5 V to +6.5 V 2/
Voltage range applied to any output in the high or low state (V_O) ..... -0.5 V to V_{CC}+0.5 V 2/ 3/
Maximum input clamp current (I_{IK}) ($V_I < 0$) ..... -50 mA
Maximum output clamp current (I_{OK}) ($V_I < 0$) ..... -50 mA
Maximum continuous output current (I_O) ..... ±50 mA
Maximum continuous current through V_{CC} or GND ..... ±100 mA
Maximum package thermal impedance (θ_{JA}) (case outline X) ..... 227°C/W 4/
Storage temperature range (T_{STG}) ..... -65°C to 150°C

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input and output negative voltage ratings may be exceeded if the input and output current rating are observed.
3/ The value of V_{CC} is provided in the recommended operating condition table.
4/ The package thermal impedance is calculated in accordance with JESD 51-7.

1.4 Recommended operating conditions. 5/ 6/

Supply voltage (V_{CC}):
- For operating ..... 1.65 V to 5.5 V
- For data retention only ..... 1.5 V

Minimum high level input voltage (V_{IH}):
- V_{CC} = 1.65 V to 1.95 V ..... 0.65 x V_{CC} V
- V_{CC} = 2.3 V to 2.7 V ..... 1.7 V
- V_{CC} = 3.0 V to 3.6 V ..... 2.0 V
- V_{CC} = 4.5 V to 5.5 V ..... 0.7 x V_{CC} V

Maximum low level input voltage (V_{IL}):
- V_{CC} = 1.65 V to 1.95 V ..... 0.35 x V_{CC} V
- V_{CC} = 2.3 V to 2.7 V ..... 0.7 V
- V_{CC} = 3.0 V to 3.6 V ..... 0.8 V
- V_{CC} = 4.5 V to 5.5 V ..... 0.3 x V_{CC} V

Input voltage (V_I) ..... 0 V to 5.5 V

Output voltage (V_O) ..... 0 V to 5.5 V

Maximum high- level output current (I_{OH}):
- V_{CC} = 1.65 V ..... -4 mA
- V_{CC} = 2.3 V ..... -8 mA
- V_{CC} = 3.0 V ..... -16 mA
- V_{CC} = 4.5 V ..... -24 mA

Maximum low level output current (I_{OL}):
- V_{CC} = 1.65 V ..... +4 mA
- V_{CC} = 2.3 V ..... +8 mA
- V_{CC} = 3.0 V ..... +16 mA
- V_{CC} = 4.5 V ..... +24 mA

Maximum input transition rise or fall time rate ($\Delta t/\Delta v$) :
- V_{CC} = 1.8 V ± 0.15 V ..... 20 ns/V
- V_{CC} = 2.5 V ± 0.20 V ..... 20 ns/V
- V_{CC} = 3.3 V ± 0.3 V ..... 10 ns/V
- V_{CC} = 5.0 V ± 0.5 V ..... 5 ns/V

Operating free-air temperature range (T_A) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
JEDEC STD 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and /or distributor maintain no responsibility or liability for product used beyond the stated limits.

6/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function table or truth table. The Function table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Load circuit and timing waveforms. The load circuit and timing waveforms shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	V_{CC}	Limits		Unit
				Min	Max	
Maximum output high level voltage	V_{OH}	I_{OH}= -100 µA	1.65 V to 5.5 V	V_{CC}-0.1		V
		I_{OH}= -4 mA	1.65 V	1.2		
		I_{OH}= -8 mA	2.3 V	1.9		
		I_{OH}= -16 mA	3.0 V	2.4		
		I_{OH}= -24 mA	3.0 V	2.3		
		I_{OH}= -24 mA	4.5 V	3.8		
Maximum output low level voltage	V_{OL}	I_{OL}= +100 µA	1.65 V to 5.5 V		0.1	V
		I_{OL}= +4 mA	1.65 V		0.45	
		I_{OL}= +8 mA	2.3 V		0.3	
		I_{OL}= +16 mA	3.0 V		0.4	
		I_{OL}= +24 mA	3.0 V		0.55	
		I_{OL}= +24 mA	4.5 V		0.55	
Input current (data or control inputs)	I_I	V_I = 5.5 V or GND	0 V to 5.5 V		±5	µA
Offset current	I_{off}	V_I or V_0 = 5.5 V	0 V		±10	µA
Supply current	I_{CC}	V_I = 5.5 V or GND I_0 = 0	1.65 V to 5.5 V		10	µA
Incremental supply current (control inputs)	ΔI_{CC}	One input at V_{CC} - 0.6 V, other inputs at V_{CC} or GND	3 V to 5.5 V		500	µA
Input capacitance (control inputs)	C_I	V_I = V_{CC} or 0 V	3.3 V	5.0 Typ		pF
Power dissipation capacitance	C_{pd}	f = 10 MHz; T_A = 25°C	3.3 V	37 Typ		pF
		f = 10 MHz; T_A = 25°C	5.0 V	40 Typ		

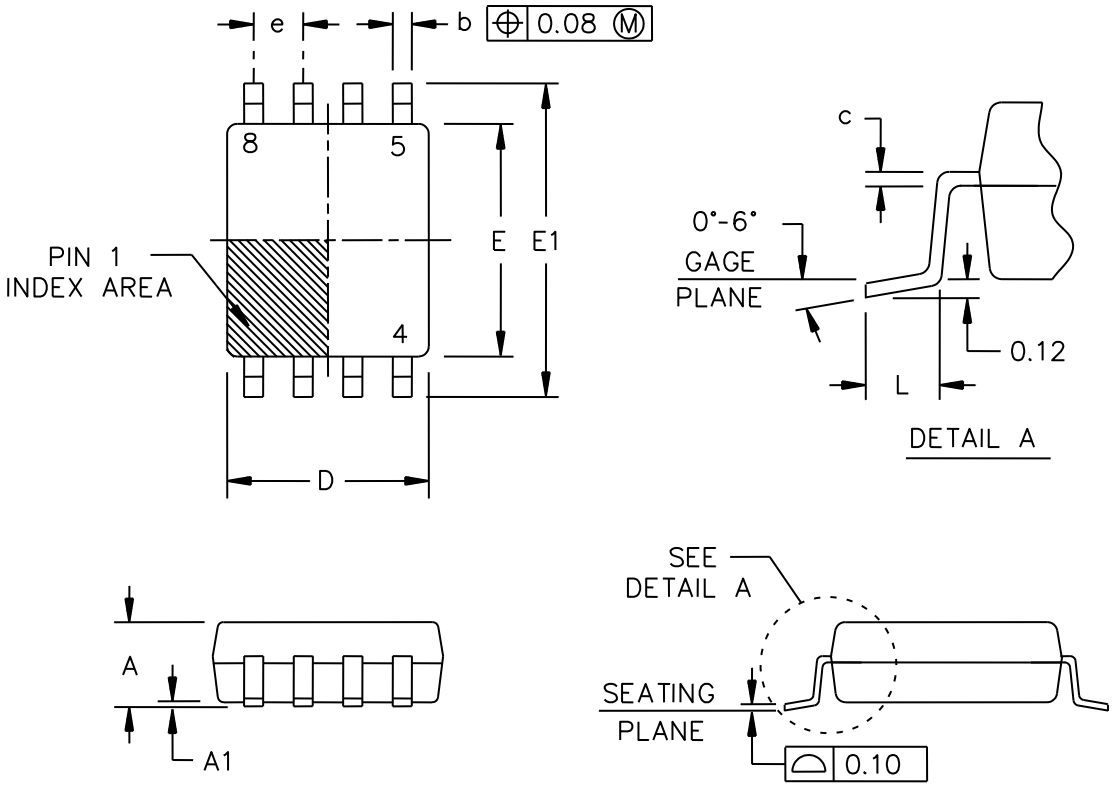
TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	V_{CC}	Limits		Unit
				Min	Max	
Timing requirements						
Clock frequency	f_{clock}		3.3 V ± 0.3 V		175	MHz
			5.0 V ± 0.5 V		200	
Pulse duration	t_w	CLK	3.3 V ± 0.3 V	2.7		ns
			5.0 V ± 0.5 V	2.0		
		$\overline{PRE}$ or $\overline{CLR}$ low	3.3 V ± 0.3 V	1.7		ns
			5.0 V ± 0.5 V	2.0		
Setup time, before CLK ↑	t_{SU}	data	3.3 V ± 0.3 V	1.3		ns
			5.0 V ± 0.5 V	1.1		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	3.3 V ± 0.3 V	1.2		ns
			5.0 V ± 0.5 V	1.2		
Hold time, data after CLK ↑	t_h		3.3 V ± 0.3 V	1.2		ns
			5.0 V ± 0.5 V	0.5		
Switching Characteristics						
Maximum operating frequency	f_{max}		3.3 V ± 0.3 V	175		MHz
			5.0 V ± 0.5 V	200		
Propagation delay time	t_{pd}	From input CLK to output Q	3.3 V ± 0.3 V	2.2	7.9	ns
			5.0 V ± 0.5 V	1.4	6.1	
		From input CLK to output $\overline{Q}$	3.3 V ± 0.3 V	2.6	8.2	ns
			5.0 V ± 0.5 V	1.6	6.4	
		From input $\overline{PRE}$ or $\overline{CLR}$ To output Q or $\overline{Q}$	3.3 V ± 0.3 V	1.7	7.9	ns
			5.0 V ± 0.5 V	1.6	6.1	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design

2/ Over recommended operating free-air temperature range (unless otherwise noted)

Case X



Dimension					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.60	0.90	E	2.20	2.40
A1	0.00	0.10	E1	3.00	3.20
b	0.17	0.25	e	0.50 NOM	
c	0.13 NOM		L	0.20	0.35
D	1.90	2.10			

NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion not to exceed 0.15 mm (0.006 inches) per side.
4. Falls within JEDEC MO-187 variation CA.

FIGURE 1. Case outline

Case X

Terminal number	Terminal symbol
1	CLK
2	D
3	$\overline{Q}$
4	GND
5	Q
6	$\overline{CLR}$
7	$\overline{PRE}$
8	V_{CC}

FIGURE 2. Terminal connections.

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H 1/	H 1/
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q0}$

H = High voltage level
L = Low voltage level
X = Don't care
1/ This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive(high) level.

FIGURE 3. Function table.

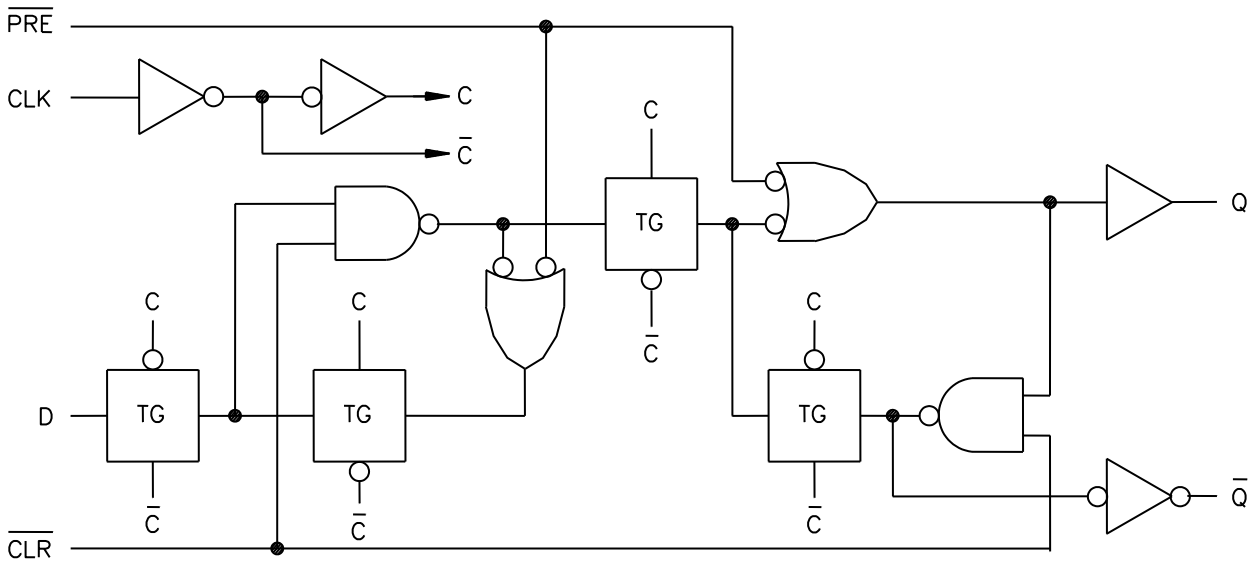
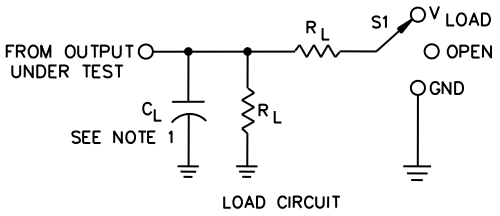
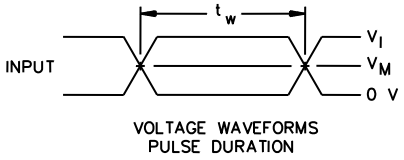


FIGURE 4. Logic diagram.

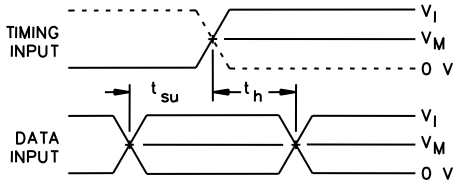


TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

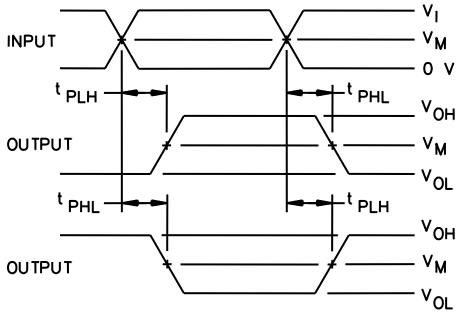
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ±0.15 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2xV_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ±0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2xV_{CC}$	30 pF	500Ω	0.15 V
3.3 V ±0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500Ω	0.3 V
5 V ±0.5 V	V_{CC}	≤ 2.5 ns	$V_{CC}/2$	$2xV_{CC}$	50 pF	500Ω	0.3 V



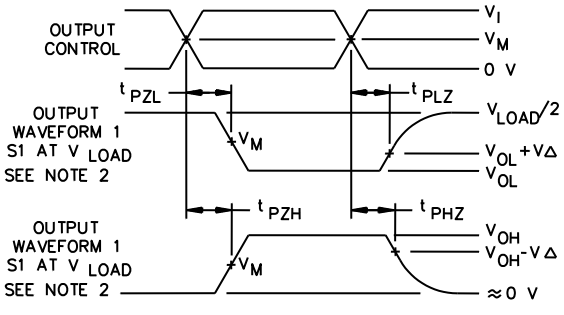
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW AND HIGH-LEVEL ENABLING

NOTES:
1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators have the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
4. The outputs are measured one at a time with one input transition per measurement.
5. t_{PLZ} and t_{PZL} are the same as t_{dis}.
6. t_{PZL} and t_{PZH} are the same as t_{en}
7. t_{PLH} and t_{PHL} are the same as t_{pd}
8. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 2 (2,000V human body model) minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side Marking
V62/08617-01XE	01295	SN74LVC2G74MDCUTEP	CHB

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493