

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update document paragraphs to current requirements. - jwc	15-05-28	Thomas M. Hess

CURRENT DESIGN ACTIVITY CAGE CODE 16236  
HAS CHANGED NAMES TO:  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990



Prepared in accordance with ASME Y14.24

Vendor item drawing

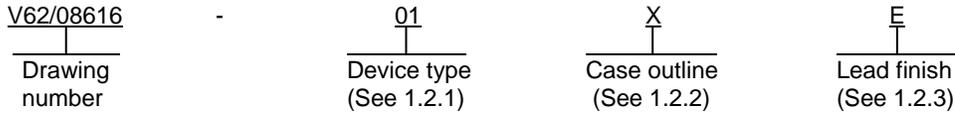
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REV STATUS OF PAGES	REV	A	A	A	A	A	A	A	A	A	A									
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PMIC N/A	PREPARED BY Muhammad A. Akbar	DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218 - 3990	
Original date of drawing YY - MM - DD  09-07-17	CHECKED BY Phu H. Nguyen	TITLE MICROCIRCUIT, DIGITAL, DUAL BUFFER / DRIVER WITH OPEN-DRAIN OUTPUTS; MONOLITHIC SILICON	
	APPROVED BY Thomas M. Hess		
	SIZE A	CODE IDENT. NO. 16236	DWG NO. <b>V62/08616</b>
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual buffer/driver with open-drain outputs microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74LVC2G07-EP	Dual buffer/driver with open drain outputs

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	6	MO-203	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. <sup>1/</sup>

Supply voltage range ( $V_{CC}$ ) .....	-0.5 V to +6.5 V
Input voltage range ( $V_i$ ) .....	-0.5 V to +6.5 V <sup>2/</sup>
Voltage range applied to any output in high-impedance or power-off state ( $V_O$ ) .....	-0.5 V to +6.5 V <sup>2/</sup>
Voltage range applied to any output in the high or low state ( $V_O$ ) .....	-0.5 V to +6.5 V <sup>2/ 3/</sup>
Maximum input clamp current ( $I_{IK}$ ) ( $V_i < 0$ ) .....	-50 mA
Maximum output clamp current ( $I_{OK}$ ) ( $V_i < 0$ ) .....	-50 mA
Maximum continuous output current ( $I_O$ ) .....	±50 mA
Maximum continuous current through $V_{CC}$ or GND .....	±100 mA
Maximum package thermal impedance ( $\theta_{JA}$ ) (case outline X) .....	259°C/W <sup>4/</sup>
Storage temperature range ( $T_{STG}$ ) .....	-65°C to 150°C

<sup>1/</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>2/</sup> The input and output negative voltage ratings may be exceeded if the input and output current rating are observed.

<sup>3/</sup> The value of  $V_{CC}$  is provided in the recommended operating condition table.

<sup>4/</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

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1.4 Recommended operating conditions. 5/

Supply voltage ( $V_{CC}$ ):	
For operating.....	1.65 V to 5.5 V
For data retention only .....	1.5 V
Minimum high level control input voltage ( $V_{IH}$ ):	
$V_{CC} = 1.65$ V to 1.95 V .....	0.65x $V_{CC}$ V
$V_{CC} = 2.3$ V to 2.7 V .....	1.7 V
$V_{CC} = 3.0$ V to 3.6 V .....	2.0 V
$V_{CC} = 4.5$ V to 5.5 V .....	0.7x $V_{CC}$ V
Maximum low level control input voltage ( $V_{IL}$ ):	
$V_{CC} = 1.65$ V to 1.95 V .....	0.35 x $V_{CC}$ V
$V_{CC} = 2.3$ V to 2.7 V .....	0.7 V
$V_{CC} = 3.0$ V to 3.6 V .....	0.8 V
$V_{CC} = 4.5$ V to 5.5 V .....	0.3 x $V_{CC}$ V
Input voltage ( $V_i$ ) .....	0 V to 5.5 V
Output voltage ( $V_o$ ) .....	0 V to 5.5 V
Maximum low level output current ( $I_{OL}$ ):	
$V_{CC} = 1.65$ V.....	4 mA
$V_{CC} = 2.3$ V.....	8 mA
$V_{CC} = 3.0$ V.....	16 mA
$V_{CC} = 4.5$ V.....	24 mA
Maximum input transition rise or fall time rate ( $\Delta t/\Delta v$ ) :	
$V_{CC} = 1.8$ V $\pm$ 0.15 V .....	20 ns/V
$V_{CC} = 2.5$ V $\pm$ 0.20 V .....	20 ns/V
$V_{CC} = 3.3$ V $\pm$ 0.3 V .....	10 ns/V
Operating free-air temperature range ( $T_A$ ) .....	-55°C to +125°C

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices
- JEDEC STD 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and /or distributor maintain no responsibility or liability for product used beyond the stated limits.

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3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function table or truth table. The Function table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Load circuit and timing waveforms. The load circuit and timing waveforms shall be as shown in figure 5.

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TABLE I. Electrical performance characteristics. 1/

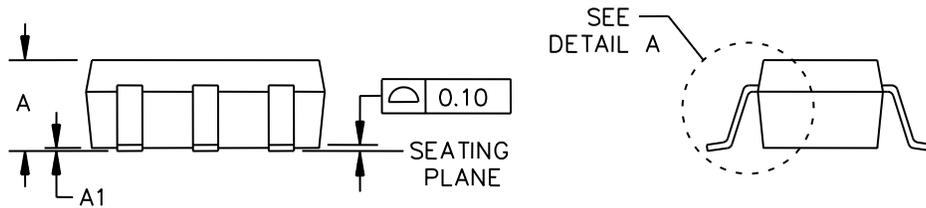
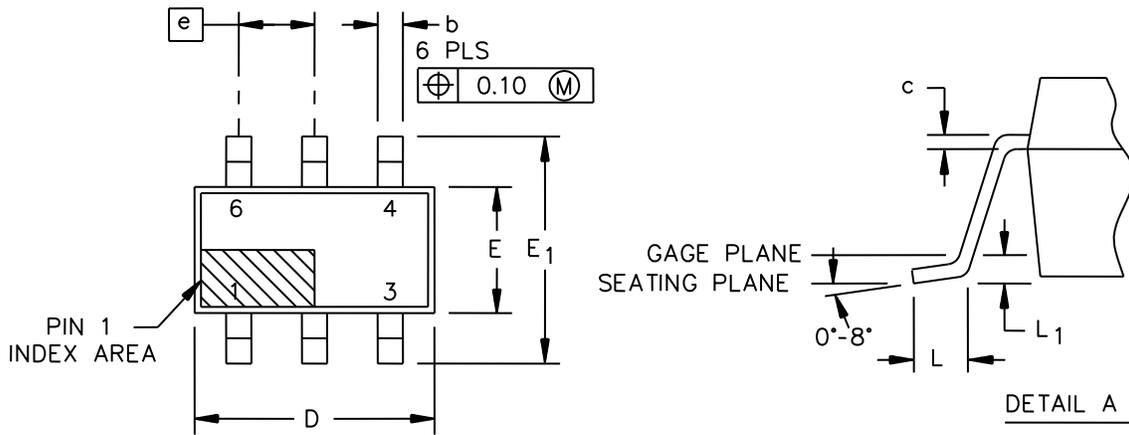
Test	Symbol	Conditions <u>2/</u> unless otherwise specified	V <sub>CC</sub>	Limits		Unit
				Min	Max	
Maximum output low level voltage	V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V		0.1	V
		I <sub>OL</sub> = 4 mA	1.65 V		0.45	
		I <sub>OL</sub> = 8 mA	2.3 V		0.3	
		I <sub>OL</sub> = 16 mA	3.0 V		0.4	
		I <sub>OL</sub> = 24 mA	3.0 V		0.55	
		I <sub>OL</sub> = 24 mA	4.5 V		0.55	
Input current (A input)	I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V		±5	μA
Offset current	I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0 V		±10	μA
Supply current	I <sub>CC</sub>	V <sub>I</sub> = 5.5 V or GND I <sub>0</sub> = 0	1.65 V to 5.5 V		10	μA
Incremental supply current (control inputs)	ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V		500	μA
Input capacitance (control inputs)	C <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0 V	3.3 V	3.5 Typ		pF
Power dissipation capacitance	C <sub>pd</sub>	f = 10 MHz; T <sub>A</sub> = 25°C	3.3 V	4 Typ		pF
		f = 10 MHz; T <sub>A</sub> = 25°C	3.3 V	4 Typ		
<b>Switching Characteristics</b>						
Propagation delay time From input A to output Y	t <sub>pd</sub>		3.3 V ± 0.3 V	1	5.7	ns
			5.0 V ± 0.5 V	0.5	4.9	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design

2/ Over recommended operating free-air temperature range (unless otherwise noted)

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Case X



Dimension					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.80	1.10	E	1.10	1.40
A1	0.00	0.10	E1	1.80	2.40
b	0.15	0.30	e	0.65 NOM	
c	0.08	0.22	L	0.26	0.46
D	1.85	2.15			

NOTES:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion not to exceed 0.15 mm (0.006 inches) per side.
4. Falls within JEDEC MO-203 variation AB.

FIGURE 1. Case outline - Continued.

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Case X

Terminal number	Terminal symbol
1	1A
2	GND
3	2A
4	2Y
5	V <sub>CC</sub>
6	1Y

FIGURE 2. Terminal connections.

Input A	Output Y
H	H
L	L

H = High voltage level  
L = Low voltage level

FIGURE 3. Function table.

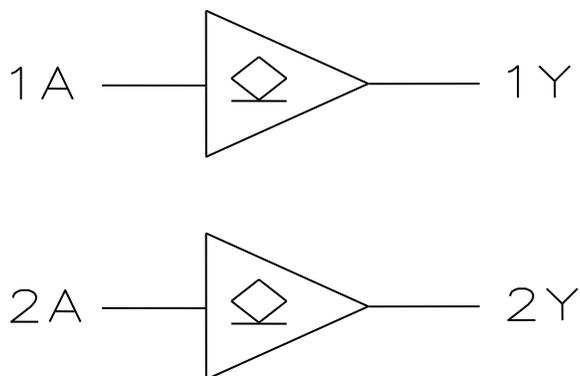
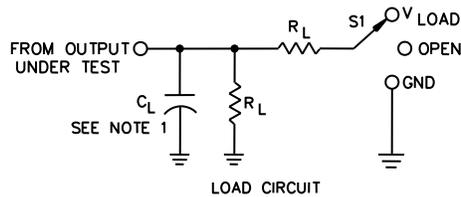


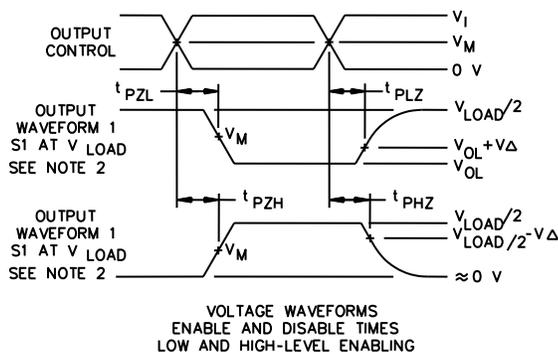
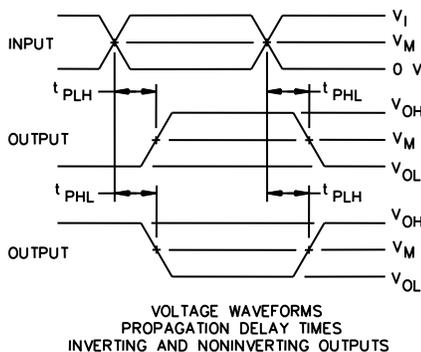
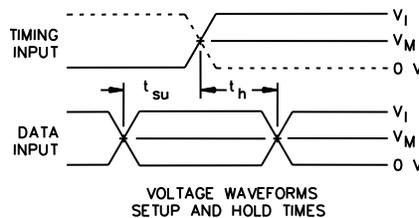
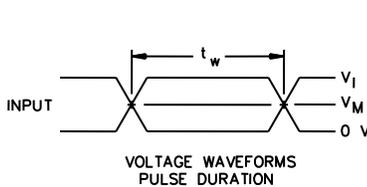
FIGURE 4. Logic diagram.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218-3990</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/08616</b>
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TEST	S1
$t_{PZL}$ (SEE NOTES 5 AND 6)	$V_{LOAD}$
$t_{PLZ}$ (SEE NOTES 5 AND 7)	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	$V_{LOAD}$

$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
1.8 V $\pm$ 0.15 V	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	3 V	$\leq 2.5$ ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
5 V $\pm$ 0.5 V	$V_{CC}$	$\leq 2.5$ ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V



NOTES:

- $C_L$  includes probe and test –fixture capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators have the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ .
- The outputs are measured one at a time with one input transition per measurement.
- Because this device has open-drain outputs,  $t_{PLZ}$  and  $t_{PZL}$  are the same as  $t_{PD}$ .
- $t_{PZL}$  is measured at  $V_M$ .
- $t_{PLZ}$  is measured at  $V_{OL} + V_{\Delta}$ .
- All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and timing waveforms.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 2 (2,000V human body model) minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top side Marking
V62/08616-01XE	01295	SN74LVC2G07MDCKTEP	CHC

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
Semiconductor Group  
8505 Forest lane  
P.O. Box 660199  
Dallas, TX 75243

Point of contact: U.S. Highway 75 South  
P.O. Box 84, M/S 853  
Sherman, TX 75090-9493

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