



1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low voltage 4 bit 1 of 2 FET multiplexer/Demultiplexer microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/08615</u> Drawing number	-	<u>01</u> Device type (See 1.2.1)	<u>X</u> Case outline (See 1.2.2)	<u>E</u> Lead finish (See 1.2.3)
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1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74CBTLV3257-EP	Low voltage 4 bit 1 of 2 FET multiplexer/demultiplexer

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	16	MO-153	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range ( $V_{CC}$ ) .....	-0.5 V to +4.6 V
Input voltage range ( $V_I$ ) .....	-0.5 V to +4.6 V <u>2/</u>
Maximum input clamp current ( $I_{IK}$ ) ( $V_I < 0$ ) .....	-50 mA
Maximum continuous channel current.....	+128 mA
Maximum package thermal impedance ( $\theta_{JA}$ ) .....	108°C/W <u>3/</u>
Storage temperature range ( $T_{STG}$ ) .....	-65°C to 150°C

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ The input and output negative voltage ratings may be exceeded if the input and output clamp current rating are observed.

3/ The package thermal impedance is calculated in accordance with JESD 51-7.

<b>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO 43218-3990</b>	<b>SIZE A</b>	<b>CODE IDENT NO. 16236</b>	<b>DWG NO. V62/08615</b>
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1.4 Recommended operating conditions. 4/ 5/

Supply voltage ( $V_{CC}$ ) .....	2.3 V to 3.6 V
Minimum high level control input voltage ( $V_{IH}$ ):	
$V_{CC} = 2.3$ V to 2.7 V .....	1.7 V
$V_{CC} = 2.7$ to 3.6 V .....	2.0 V
Maximum low level control input voltage ( $V_{IL}$ ):	
$V_{CC} = 2.3$ V to 2.7 V .....	0.7 V
$V_{CC} = 2.7$ V to 3.6 V .....	0.8 V
Operating free-air temperature range ( $T_A$ ) .....	-55°C to +125°C

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

- JEP95            –           Registered and Standard Outlines for Semiconductor Devices
- JESD 51-7       –           High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

Applications for copies should be addressed to the Electronic Industries Alliance, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107 or online at <https://www.jedec.org>.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function table or truth table. The Function table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Load circuit and timing waveforms. The load circuit and timing waveforms shall be as shown in figure 5.

4/ All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.

5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and /or distributor maintain no responsibility or liability for product used beyond the stated limits.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	V <sub>CC</sub>	Limits		Unit	
				Min	Max		
Input clamp voltage	V <sub>IK</sub>	I <sub>I</sub> = -18 mA	3.0 V		-1.2	V	
Input current	I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V		±1	μA	
Offset current	I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 3.6 V	0 V		15	μA	
Supply current	I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6 V		10	μA	
Incremental supply current (control inputs)	ΔI <sub>CC</sub> 3/	One input at 3.0 V, other inputs at V <sub>CC</sub> or GND	3.6 V		300	μA	
Input capacitance (control inputs)	C <sub>I</sub>	V <sub>I</sub> = 3.0 V or 0 V	3.3 V	3 Typical 4/		pF	
Input/Output capacitance	A port	C <sub>IO(OFF)</sub>	V <sub>I</sub> = 3.0 V or 0 V, $\overline{OE}$ = V <sub>CC</sub>	3.3 V	10.5 Typical 4/		pF
	B port				5.5 Typical 4/		
On-state resistance	r <sub>on</sub> 5/	V <sub>I</sub> = 0 V, I <sub>I</sub> = +64 mA	2.3 V Typical at 2.5 V		8	Ω	
		V <sub>I</sub> = 0 V, I <sub>I</sub> = +24 mA			8		
		V <sub>I</sub> = 1.7 V, I <sub>I</sub> = +15 mA			40		
		V <sub>I</sub> = 0 V, I <sub>I</sub> = +64 mA	3.0 V		7	Ω	
		V <sub>I</sub> = 0 V, I <sub>I</sub> = +24 mA			7		
		V <sub>I</sub> = 2.4 V, I <sub>I</sub> = +15 mA			15		

**Switching Characteristics**

Propagation delay time	t <sub>pd</sub>	From input A or B 6/ to output B or A	2.5 V ± 0.2 V		0.15	ns
			3.3 V ± 0.3 V		0.25	
		From input S to output A or B	2.5 V ± 0.2 V	1.8	8.1	ns
			3.3 V ± 0.3 V	1.8	7.3	
Enable time	t <sub>en</sub>	From input S to output A or B	2.5 V ± 0.2 V	1.7	7.5	
			3.3 V ± 0.3 V	1.7	6.5	
Disable time	t <sub>dis</sub>	From input S to output A or B	2.5 V ± 0.2 V	1.0	6.3	
			3.3 V ± 0.3 V	1.0	6.0	
Enable time	t <sub>en</sub>	From input $\overline{OE}$ to output A or B	2.5 V ± 0.2 V	1.9	7.1	
			3.3 V ± 0.3 V	2.0	6.2	
Disable time	t <sub>dis</sub>	From input $\overline{OE}$ to output A or B	2.5 V ± 0.2 V	1.0	7.0	
			3.3 V ± 0.3 V	1.6	6.5	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design

2/ Over recommended operating free-air temperature range (unless otherwise noted).

3/ This is the increase supply current for each input that is at the specified voltage level, rather than V<sub>CC</sub> or GND.

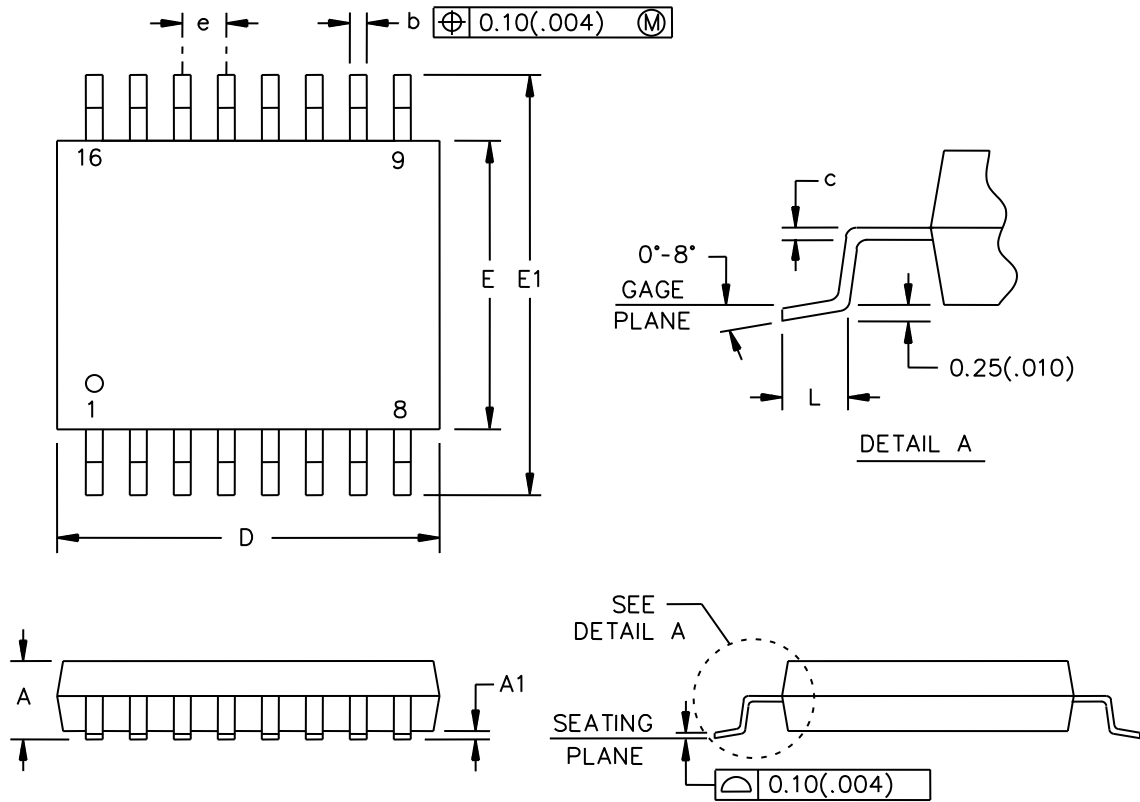
4/ All typical values are at V<sub>CC</sub> = 3.3 V (unless otherwise noted), T<sub>A</sub> = 25°C.

5/ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

6/ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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Case X



Dimension					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	1.20 Max		E	4.30	4.50
A1	0.05	0.15	E1	6.20	6.60
b	0.19	0.30	e	0.65 NOM	
c	0.15 NOM		L	0.50	0.75
D	4.90	5.10			

NOTES:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion not to exceed 0.15 mm (0.006 inches) per side.
4. Falls within JEDEC MO-153.

FIGURE 1. Case outline - Continued.

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Case X

Terminal number	Terminal symbol
1	S
2	1B1
3	1B2
4	1A
5	2B1
6	2B2
7	2A
8	GND
9	3A
10	3B2
11	3B1
12	4A
13	4B2
14	4B1
15	$\overline{OE}$
16	V <sub>CC</sub>

FIGURE 2. Terminal connections.

Inputs		Function
$\overline{OE}$	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect

H = High voltage level  
 L = Low voltage level  
 X = Don't care

FIGURE 3. Function table.

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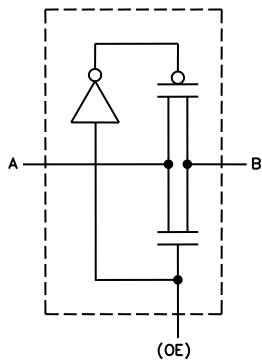
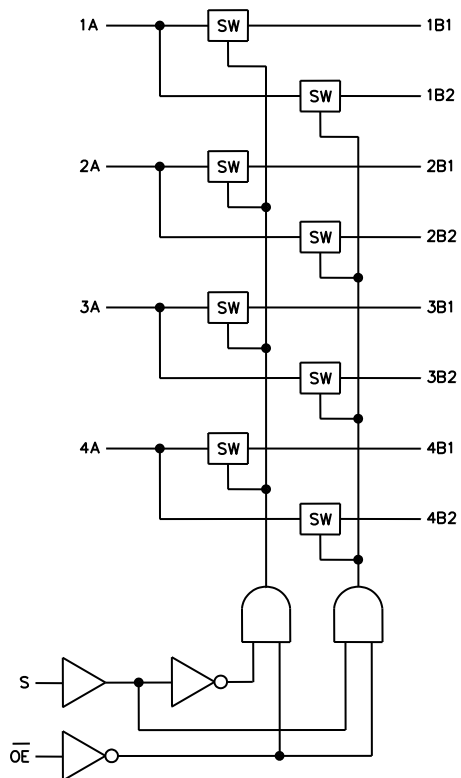
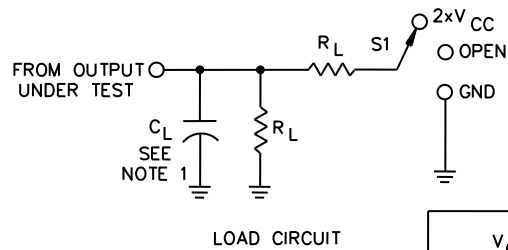


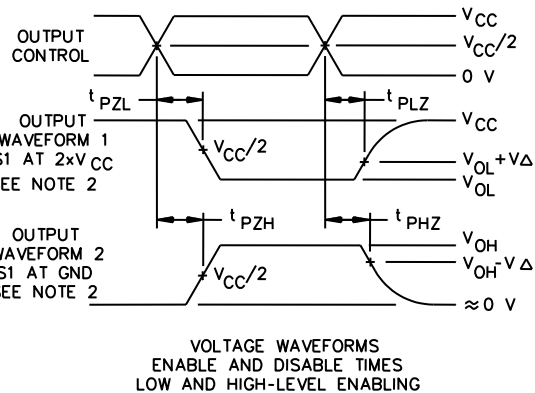
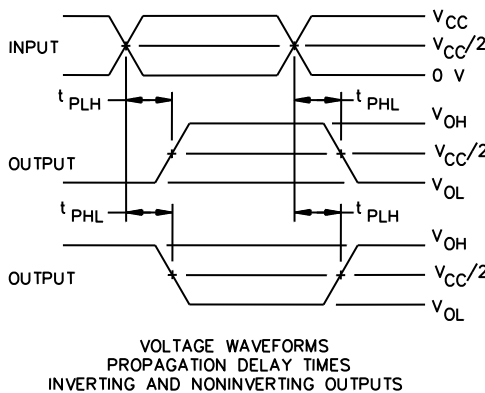
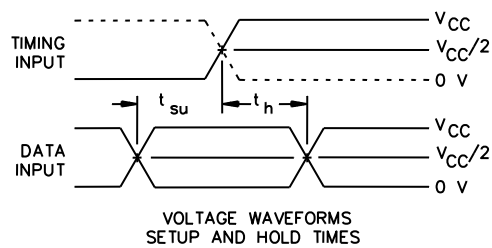
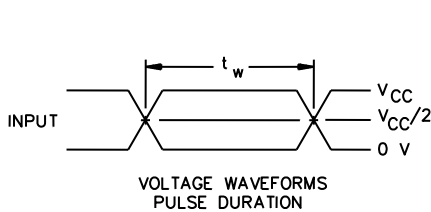
FIGURE 4. Logic diagram.

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TEST	S1
$t_{PLH} / t_{PHL}$	OPEN
$t_{PLZ} / t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ} / t_{PZH}$	GND

$V_{CC}$	$C_L$	$R_L$	$V_{\Delta}$
$2.5 \text{ V} \pm 0.2 \text{ V}$	30 pF	500 $\Omega$	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	50 pF	500 $\Omega$	0.3 V



**NOTES:**

1.  $C_L$  includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_o = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
4. The outputs are measured one at a time with one transition per measurement.
5. All parameters and waveforms are not applicable to all devices.
6.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
7.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
8.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
9. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and timing waveforms.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 2 (2,000V human body model) minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top side Marking
V62/08615-01XE	01295	CCBTLV3257MPWREP	CL257EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
Semiconductor Group  
8505 Forest lane  
P.O. Box 660199  
Dallas, TX 75243

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