REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	17-04-17	Thomas M. Hess

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	**REV**			A	A	A	A	A	A	A	A	A	A	A								
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PMIC N/A	**PREPARED BY** Muhammad A. Akbar	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO 43218 - 3990**
Original date of drawing YY - MM - DD 09-07-17	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, DIGITAL, DUAL D-TYPE POSITIVE EDGE TRIGGERED FLIP-FLOP WITH CLEAR AND PRESET, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/08613**
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AMSC N/A

5962-V032-17

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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual D-type positive edge triggered flip-flop with clear and preset microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/08613	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74HC74-EP	Dual D-type positive edge triggered flip-flop with clear and preset.

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	14	MO-153	Plastic small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.5 V to +7.0 V
Maximum input clamp current (I_{IK}) ($V_I < 0$ or $V_I = 0$ to V_{cc}) ..... ±20 mA
Maximum output clamp current (I_{OK}) ($V_O < 0$ or $V_O = 0$ to V_{CC}) ..... ±20 mA
Maximum continuous output current (I_O) ($V_O = 0$ to V_{CC}) ..... ±25 mA
Maximum continuous current through V_{CC} or GND ..... ±50 mA
Maximum package thermal impedance (θ_{JA}) ..... 113°C/W 2/
Storage temperature range (T_{STG}) ..... -60°C to 150°C

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ The package thermal impedance is calculated in accordance with JESD 51-7.

1.4 Recommended operating conditions. 3/ 4/

Supply voltage (V_{CC})	2.0 V to 6.0 V
Minimum high level input voltage (V_{IH}):	
V_{CC} = 2.0 V	1.5 V
V_{CC} = 4.5 V	3.15 V
V_{CC} = 6.0 V	4.2 V
Maximum low level input voltage (V_{IL}):	
V_{CC} = 2.0 V	0.5 V
V_{CC} = 4.5 V	1.35 V
V_{CC} = 6.0 V	1.80 V
Input voltage (V_I)	0 V to V_{CC}
Output voltage (V_O)	0 to V_{CC}
Maximum input transition rise or fall time rate ($\Delta t/\Delta v$) :	
V_{CC} = 2.0 V	1000 ns/V
V_{CC} = 4.5 V	500 ns/V
V_{CC} = 6.0 V	400 ns/V
Operating free-air temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and /or distributor maintain no responsibility or liability for product used beyond the stated limits.

4/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function table or truth table. The Function table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Load circuit and timing waveforms. The load circuit and timing waveforms shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	V_{CC}	Limits at T_A = 25°C		Limits at -55°C ≤ T_A ≤ 125°C		Unit
				Min	Max	Min	Max	
High level output voltage	V_{OH}	I_{OH} = -20 µA V_I = V_{IH} or V_{IL}	2.0 V	1.9		1.9		V
			4.5 V	4.4		4.4		
			6.0 V	5.9		5.9		
		I_{OH} = - 4 mA V_I = V_{IH} or V_{IL}	4.5 V	3.98		3.7		
		I_{OH} = -5.2 mA V_I = V_{IH} or V_{IL}	6.0 V	5.48		5.2		
Low level output voltage	V_{OL}	I_{OL} = +20 µA V_I = V_{IH} or V_{IL}	2.0 V		0.1		0.1	V
			4.5 V		0.1		0.1	
			6.0 V		0.1		0.1	
		I_{OL} = +4 mA V_I = V_{IH} or V_{IL}	4.5 V		0.26		0.40	
		I_{OL} = +5.2 mA V_I = V_{IH} or V_{IL}	6.0 V		0.26		0.40	
Input current	I_I	V_I = V_{CC} or 0	6.0 V		±100		±1000	nA
Supply current	I_{CC}	V_I = V_{CC} or 0, I_O = 0	6.0 V		4		80	µA
Input capacitance	C_i		2 V to 6 V		10		10	pF
Power dissipation capacitance	C_{pd}	No load; T_A = 25°C		35 typical				pF
Timing requirements								
Clock frequency	f_{clock}		2.0 V		6		4.2	MHz
			4.5 V		31		21	
			6.0 V	0	36	0	25	
Pulse duration	t_W	$\overline{PRE}$ or $\overline{CLR}$ low	2.0 V	100		150		ns
			4.5 V	20		20		
			6.0 V	17		17		
		CLK high or low	2.0 V	80		80		ns
			4.5 V	16		16		
			6.0 V	14		14		
Setup time before CLK↑	t_{SU}	$\overline{PRE}$ or $\overline{CLR}$ inactive	2.0 V	25		25		ns
			4.5 V	5		40		
			6.0 V	4		8		
		data	2.0 V	100		150		ns
			4.5 V	20		30		
			6.0 V	017		25		
Hold time data after CLK↑	t_h		2.0 V	0		0		ns
			4.5 V	0		0		
			6.0 V	0		0		

See footnote at end of table

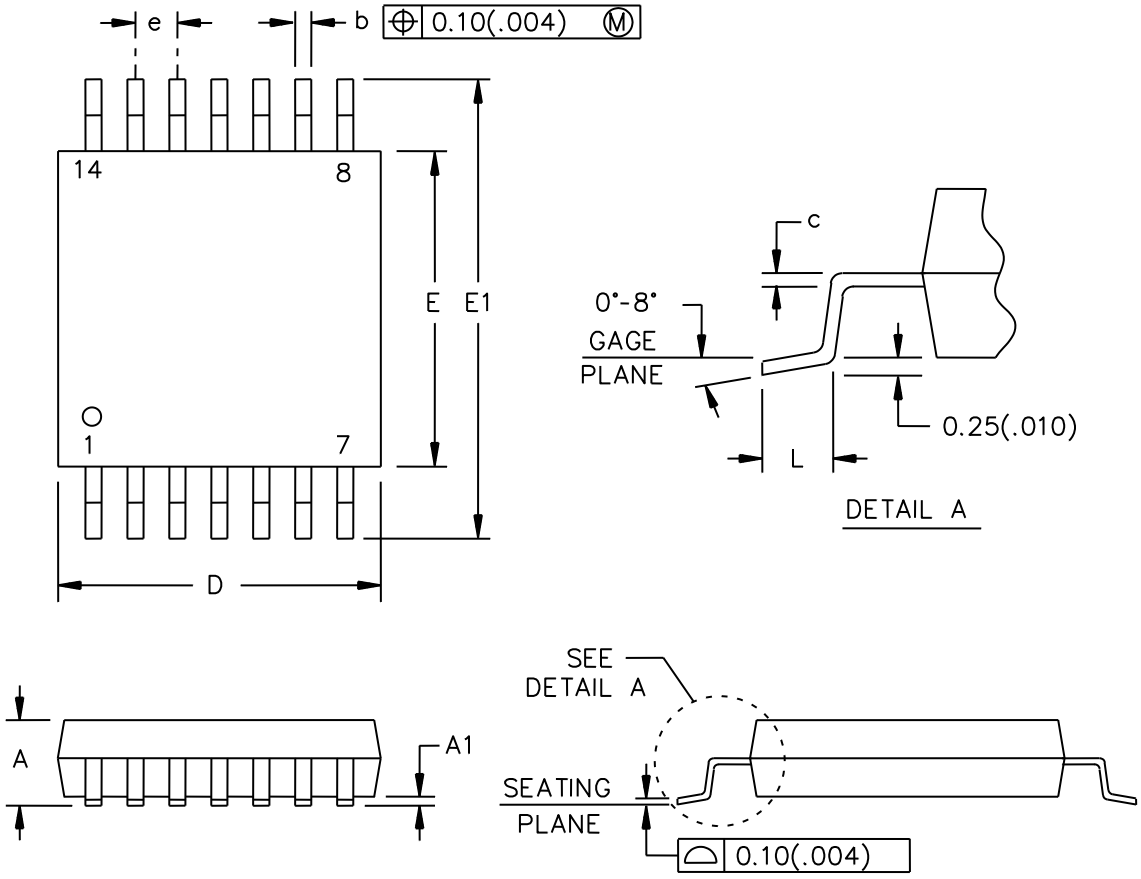
TABLE I. Electrical performance characteristics-Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	V_{CC}	Limits at T_A = 25°C		Limits at -55°C ≤ T_A ≤ 125°C		Unit
				Min	Max	Min	Max	
Switching characteristics								
Maximum frequency	f_{max}	C_L = 50 pF	2.0 V	6		4.2		MHz
			4.5 V	31		21		
			6.0 V	36		25		
Propagation delay time	t_{pd}	$\overline{PRE}$ to Q or $\overline{Q}$ $\overline{CLR}$ to Q or $\overline{Q}$	2.0 V		230		345	ns
			4.5 V		46		69	
			6.0 V		39		59	
		CLK to Q or $\overline{Q}$	2.0 V		175		250	ns
			4.5 V		35		50	
			6.0 V		30		42	
Transition times	t_t	Q or $\overline{Q}$	2.0 V		75		110	ns
			4.5 V		15		22	
			6.0 V		13		19	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Over operating free-air temperature range (unless otherwise noted).

Case X



Dimension					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	1.20 max		E	4.30	4.50
A1	0.05	0.15	E1	6.20	6.60
b	0.19	0.30	e	0.65 NOM	
c	0.15 NOM		L	0.50	0.75
D	5.10 NOM				

NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion not to exceed 0.15 mm (0.006 inches) per side.
4. Falls within JEDEC MO-153.

FIGURE 1. Case outline

Case X

Terminal number	Terminal symbol
1	$1\overline{CLR}$
2	1D
3	1CLK
4	$1\overline{PRE}$
5	1Q
6	$1\overline{Q}$
7	GND
8	$2\overline{Q}$
9	2Q
10	$2\overline{PRE}$
11	2CLK
12	2D
13	$2\overline{CLR}$
14	V_{CC}

FIGURE 2. Terminal connections.

Inputs				Output Y	
$\overline{PRE}$A	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H[1]	H[1]
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = High voltage level
L = Low voltage level
X = Don't care
1/ This configuration is non-stable; that sis t does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

FIGURE 3. Function table.

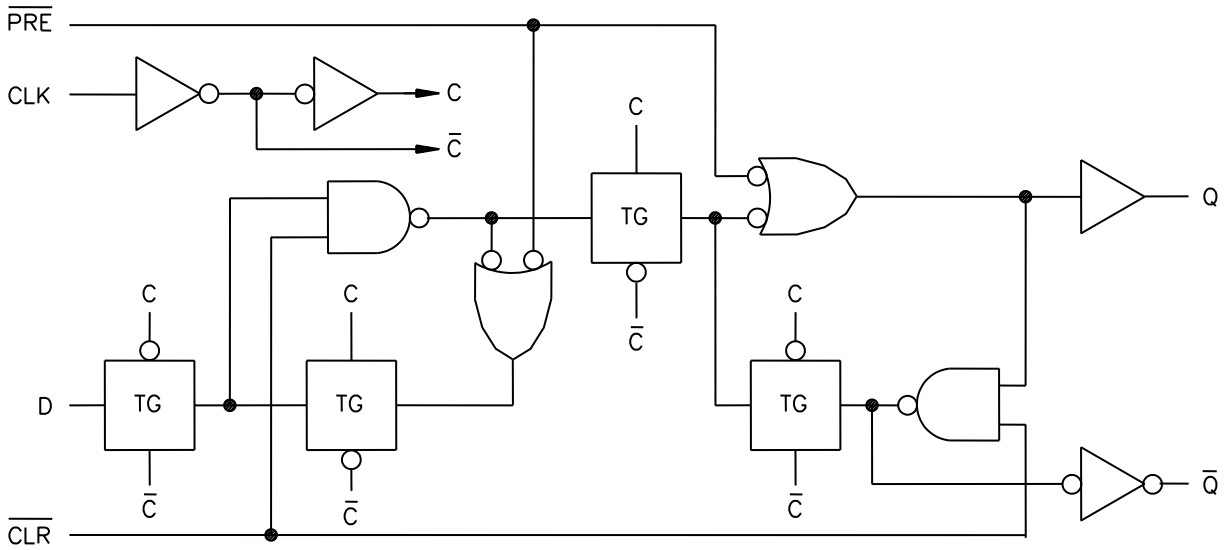
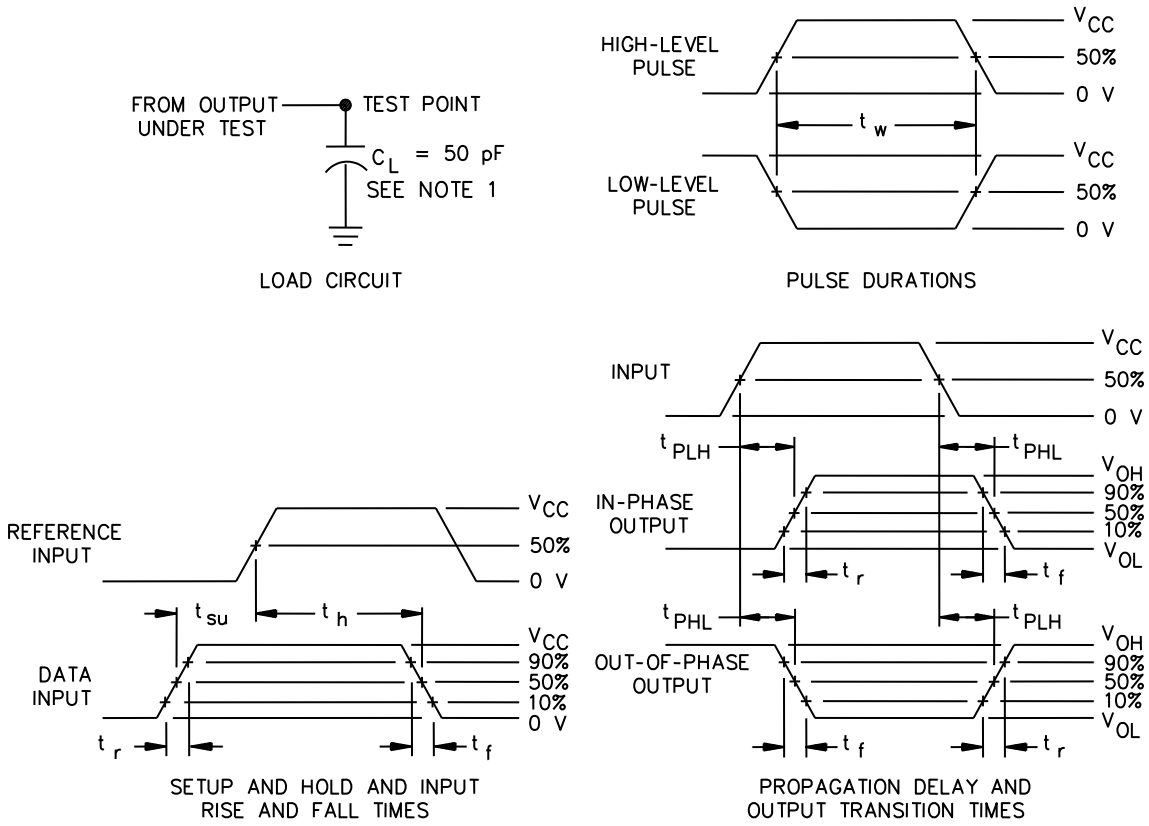


FIGURE 4. Logic diagram.



NOTES:

1. C_L includes probe and text –fixture capacitance.
2. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤.6 ns, t_f ≤.6 ns.
3. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
4. The outputs are measured one at a time with one input transition per measurement.
5. t_{PLH} and t_{PHL} are the same as t_{pd}.

FIGURE 5. Load circuit and timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side Marking
V62/08613-01XE	01295	SN74HC74MPWREP	HC74MEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493