REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	17-01-24	Thomas M. Hess
B	Update boilerplate paragraphs to current VID description requirements. - DRH	24-02-23	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**		B	B	B	B	B	B	B	B	B										
	PAGE		1	2	3	4	5	6	7	8	9										

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** https://www.dla.mil/landandmaritime
Original date of drawing YY MM DD 08-03-24	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL, SINGLE 2-INPUT EXCLUSIVE OR GATE, MONOLITHIC SILICON
	SIZE A **CODE IDENT. NO.** 16236	**DWG NO.** **V62/08612**
	REV B	**PAGE** 1 **OF** 9

AMSC N/A
5962-V041-24
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance single 2-input EXCLUSIVE-OR gate microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/08612	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74AHC1G86-EP	Single 2-input EXCLUSIVE-OR gate

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	5	MO-203	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to 7.0 V
Input voltage range (V_I)	-0.5 V to 7.0 V 2/
Output voltage range (V_O)	-0.5 V to V_{CC} + 0.5 V 2/
Maximum input clamp current (I_{IK}) ($V_I < 0$)	-20 mA
Maximum output clamp current (I_{OK}) ($V_O < 0$ or $V_O = 0$ to V_{CC})	±20 mA
Maximum continuous output current (I_O) ($V_O = 0$ to V_{CC})	±25 mA
Maximum continuous current through V_{CC} or GND	±50 mA
Maximum package thermal impedance (θ_{JA})	252°C/W 3/
Storage temperature range (T_{STG})	-65°C to 150°C

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
3/ The package thermal impedance is calculated in accordance with JESD 51-7.

1.4 Recommended operating conditions. 4/

Supply voltage (V_{CC})	2.0 V to 5.5 V
Minimum high level input voltage	
V_{CC} = 2.0 V	1.5 V
V_{CC} = 3.0 V	2.1 V
V_{CC} = 5.5 V	3.85 V
Maximum high level input voltage	
V_{CC} = 2.0 V	0.5 V
V_{CC} = 3.0 V	0.9 V
V_{CC} = 5.5 V	1.65 V
Input voltage (V_I)	0 V to 5.5 V
Output voltage (V_O)	0 to V_{CC}
Maximum high level output current (I_{OH}):	
V_{CC} = 2.0 V	-50 µA
V_{CC} = 3.0 V	-4 mA
V_{CC} = 5.5 V	-8 mA
Maximum low level output current (I_{OL}):	
V_{CC} = 2.0 V	50 µA
V_{CC} = 3.0 V	4 mA
V_{CC} = 5.5 V	8 mA
Maximum input transition rise or fall rate (Δt/Δv) :	
V_{CC} = 3.3 V ±0.3 V	100 ns/V
V_{CC} = 5.0 V ±0.5 V	20 ns/V
Operating free-air temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices
JESD 51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at https://www.jedec.org.)

4/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function table. The Function table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

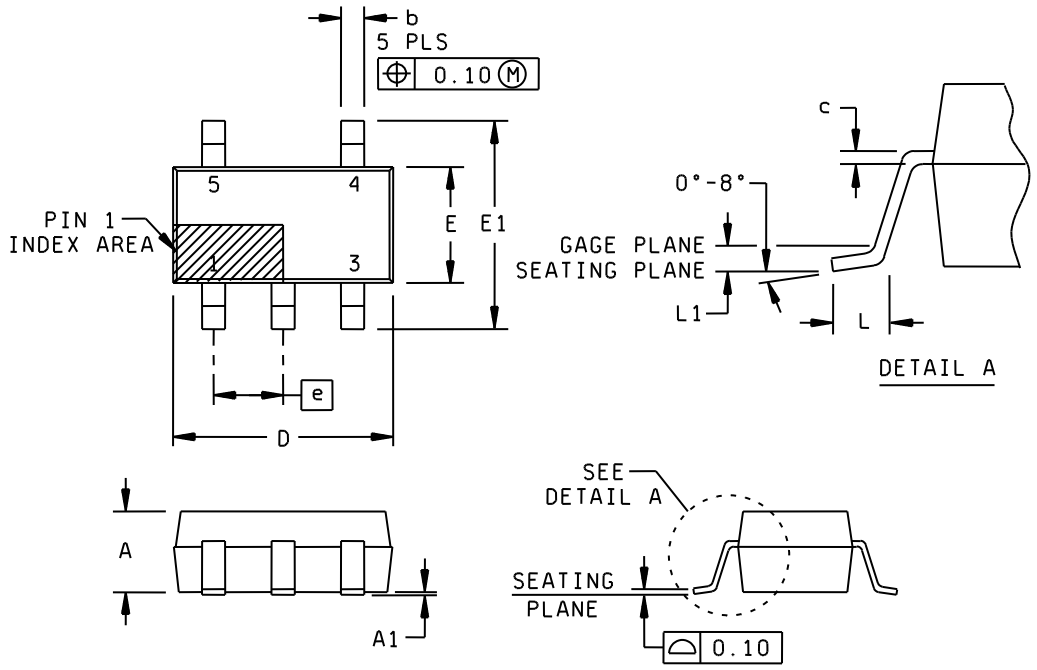
3.5.5 Load circuit and timing waveforms. The load circuit and timing waveforms shall be as shown in figure 5.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions unless otherwise specified	V_{CC}	Device type	T_A = 25°C		-55°C ≤ T_A ≤ 125°C		Unit
					Min	Max	Min	Max	
High level output voltage	V_{OH}	I_{OH} = -50 µA	2 V	All	1.9		1.9		V
			3 V		2.9		2.9		
			4.5 V		4.4		4.4		
		I_{OH} = - 4 mA	3 V		2.58		2.48		
		I_{OH} = -8 mA	4.5 V		3.94		3.8		
Low level output voltage	V_{OL}	I_{OL} = 50 µA	2 V			0.1		0.1	V
			3 V			0.1		0.1	
			4.5 V			0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.44	
Input current	I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1	µA
Supply current	I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			1		10	µA
Input capacitance	C_i	V_I = V_{CC} or GND	5 V			10		10	pF
Power dissipation capacitance	C_{pd}	No load, f = 1 MHz	5 V		18 TYP				pF
Switching characteristics									
Propagation delay time, from input A or B to output Y	t_{PLH}	C_L = 50 pF	3.3 ±0.3 V	All		14.5	1	16.5	ns
	t_{PHL}					14.5	1	16.5	
	t_{PLH}		5 ±0.5 V			8.8	1	10	
	t_{PHL}					8.8	1	10	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

Case X



Dimension					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.80	1.10	E	1.10	1.40
A1	0.00	0.10	E1	1.80	2.40
b	0.15	0.30	e	0.65 NOM	
c	0.08	0.22	L	0.26	0.46
D	1.85	2.15			

NOTES:
1. This drawing is subject to change without notice.
2. Body dimensions do not include mold flash or protrusion not to exceed 0.15 mm (0.006 inches) per side.
3. Falls within JEDEC MO-203 variation AA.

FIGURE 1. Case outline.

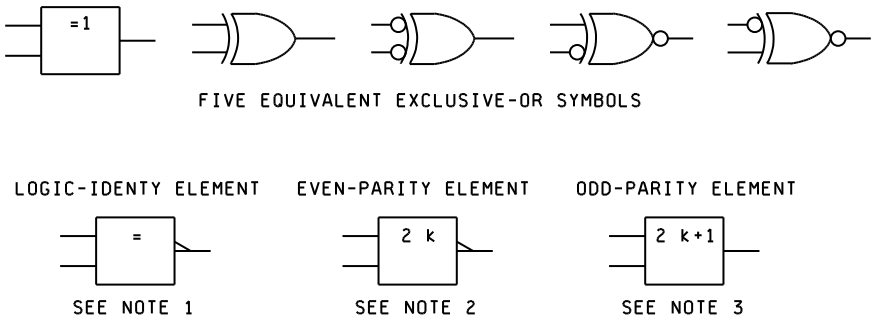
Case X

Terminal number	Terminal symbol
1	A
2	B
3	GND
4	Y
5	V_{CC}

FIGURE 2. Terminal connections.

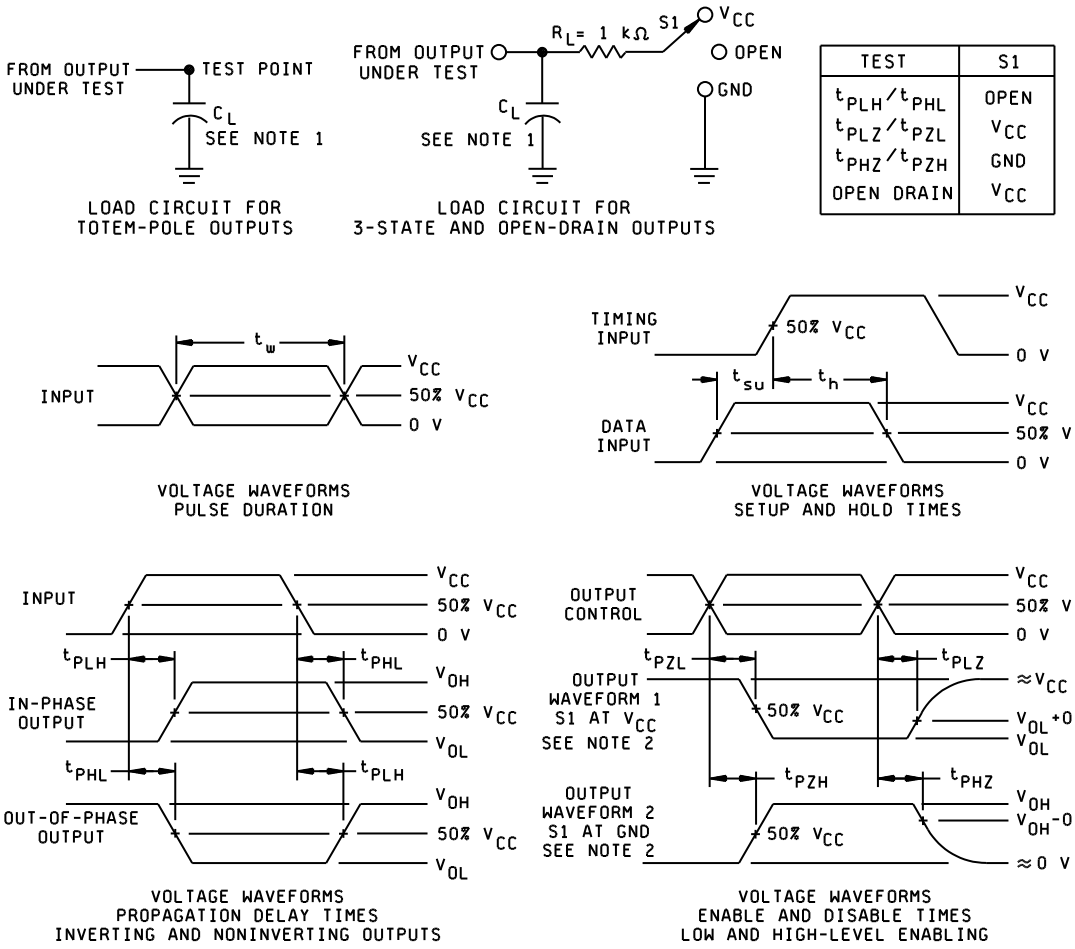
Inputs		Output Y
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

FIGURE 3. Function table.



NOTES:
1. The output is active (low) if all inputs stand at the same logic level (i.e., A = B)
2. The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.
3. The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

FIGURE 4. Logic diagram.



NOTES:

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤.3 ns, t_f ≤.3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side Marking
V62/08612-01XE	01295	SN74AHC1G86MDCKREP	CGB

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest lane P.O. Box 660199 Dallas, TX 75243