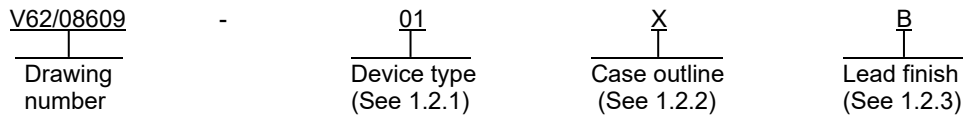


1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual low dropout (LDO) regulator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	ISL9000A	Dual low dropout (LDO) regulator

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	10	MO-229	Dual leadless plastic package, V _{OUT1} = 3.3 V, V _{OUT2} = 1.8 V

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{IN})	+6.0 V
All other pins	-0.3 V to [$V_{IN} + 0.3$] V
Power dissipation (P_D):	
$T_A = 100^\circ\text{C}$	590 mW
$T_A = 125^\circ\text{C}$	295 mW
Junction temperature (T_J)	+150°C
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum lead temperature (soldering 10 seconds)	+300°C
Thermal resistance, junction to case (θ_{JC})	10°C/W <u>2/</u>
Thermal resistance, junction to ambient (θ_{JA})	50°C/W <u>3/</u>

1.4 Recommended operating conditions. 4/

Supply voltage range (V_{IN})	2.3 V to 5.5 V
Operating free-air temperature range (T_A)	-55°C to +125°C

- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ For θ_{JC} , the case temperature location is the center of the exposed metal pad on the package underside.
- 3/ The θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with direct attach features. See manufacturer’s technical brief TB379.
- 4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
DC CHARACTERISTICS SECTION							
Supply voltage	V _{IN}		-55°C to +125°C	01	2.3	5.5	V
Ground current	I _{DD1}	One LDO active Quiescent condition: I _{O1} = 0 μA, I _{O2} = 0 μA	-55°C to +125°C	01		35	μA
	I _{DD2}	Both LDO active Quiescent condition: I _{O1} = 0 μA, I _{O2} = 0 μA				56	μA
Shutdown current	I _{DDS}		-55°C to +125°C	01		1.3	μA
Under voltage lock out (UVLO) threshold	V _{UV+}		-55°C to +125°C	01	1.9	2.3	V
	V _{UV-}				1.6	2.0	V
Regulation voltage accuracy		Initial accuracy at V _{IN} = [V _O + 0.5] V, I _O = 10 mA	T _J = +25°C	01	-0.7	+0.7	%
		V _{IN} = [V _O + 0.5] V to 5.5 V, I _O = 10 μA to 100 mA	T _J = +25°C		-0.8	+0.8	%
			-55°C to +125°C		-1.8	+1.8	%
Maximum output current	I _{MAX}	Continuous	T _J = +125°C	01		100	mA
			T _J = +150°C			50	mA
Internal current limit	I _{LIM}		-55°C to +125°C	01	350	600	mA
Dropout voltage <u>3/</u>	V _{DO1}	I _O = 100 mA, V _O < 2.5 V	-55°C to +125°C	01		500	mV
	V _{DO3}	I _O = 100 mA, V _O > 2.8 V				375	mV
Thermal shutdown temperature	T _{SD+}		+25°C	01	145 typical		°C
	T _{SD-}				110 typical		
AC CHARACTERISTICS SECTION							
Ripple rejection <u>4/</u>		At 1 kHz, I _O = 10 mA, V _O = 1.8 V, V _{IN} = 2.8 V (min), C _{BYP} = 0.1 μF	+25°C	01	90 typical		dB
		At 10 kHz, I _O = 10 mA, V _O = 1.8 V, V _{IN} = 2.8 V (min), C _{BYP} = 0.1 μF			70 typical		
		At 100 kHz, I _O = 10 mA, V _O = 1.8 V, V _{IN} = 2.8 V (min), C _{BYP} = 0.1 μF			50 typical		
Output noise <u>4/</u> voltage		I _O = 100 μA, V _O = 1.5 V, C _{BYP} = 0.1 μF, BW = 10 Hz to 100 kHz	+25°C	01	30 typical		μVrms
DEVICE START UP CHARACTERISTICS SECTION. SEE FIGURE 4							
Device enable time	t _{EN}	Time from assertion of the ENx pin to when the output voltage reaches 95% of the V _O (nom)	-55°C to +125°C	01		525	μs
LDO soft start ramp rate	t _{SSR}	Slope of linear portion of LDO output voltage ramp during start up	-55°C to +125°C	01		65	μs/V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
EN1, EN2 PIN CHARACTERISTICS SECTION							
Input low voltage	V _{IL}		-55°C to +125°C	01	-0.3	0.4	V
Input high voltage	V _{IH}		-55°C to +125°C	01	1.4	V _{IN} + 0.3	V
Input leakage current	I _{IL} , I _{IH}		-55°C to +125°C	01		0.1	μA
Pin capacitance	C _{PIN}	Informative	+25°C	01	5 typical		pF
POR1, POR2 PIN CHARACTERISTICS SECTION. SEE FIGURE 4							
POR1, POR2 thresholds	V _{POR+}	As a percentage of nominal output voltage	-55°C to +125°C	01	91	97	%
	V _{POR-}				87	93	
POR1 delay	t _{P1LH}		-55°C to +125°C	01	0.4	3.6	ms
	t _{P1HL}				25 typical		μs
POR2 delay	t _{P2LH}	C _{POR} = 0.01 μF	-55°C to +125°C	01	70	330	ms
	t _{P2HL}				25 typical		μs
POR1, POR2 pin output low voltage	V _{OL}	At I _{OL} = 1.0 Ma	-55°C to +125°C	01		0.2	V
POR1, POR2 pin internal pull up resistance	R _{POR}		-55°C to +125°C	01	78	180	kΩ

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{IN} = [V_O + 0.5] V to 6.5 V with a minimum V_{IN} of 2.3 V, C_{IN} = 1 μF, C_O = 1 μF, C_{BYP} = 0.0 μF, and C_{POR} = 0.01 μF.

3/ VO_x = 9.8 * VO_x(NOM); valid for VO_x greater than 1.85 V.

4/ Guaranteed by design and characterization.

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Case X

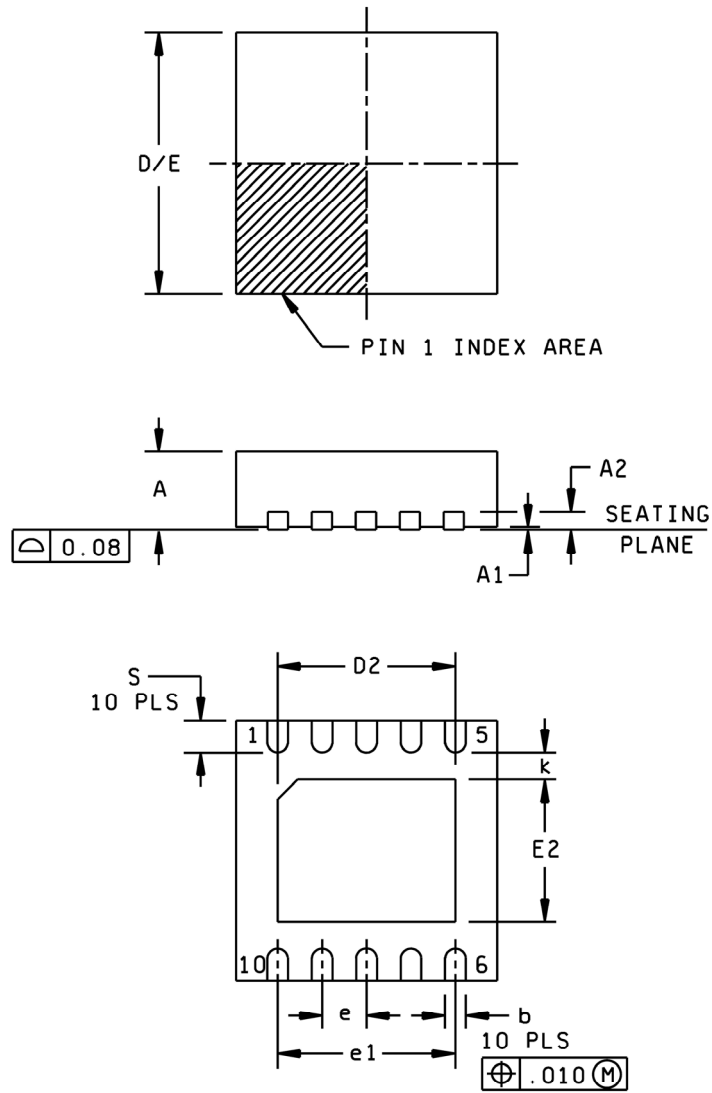


FIGURE 1. Case outline.

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Case X – continued.

Symbol	Dimensions				Notes
	Millimeters		Inches		
	Minimum	Maximum	Minimum	Maximum	
A	0.85	0.95	.033	.037	
A1		0.05		.001	
A2	0.20 REF		.007 REF		
b	0.20	0.30	.007	.011	3, 6
D	3.00 BSC		.118 BSC		
D2	2.33	2.43	.091	.095	
E	3.00 BSC		.118 BSC		
E2	1.59	1.69	.062	.066	
e	0.50 BSC		.019 BSC		
e1	2.33	2.43	.091	.095	5, 6
k	0.20		.007		
s	0.35	0.45	.013	.017	6

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Dimensioning and tolerance per ASME Y 14.5M-1994.
3. Dimension "b" lead width applies to the metallized terminal and is measured between 0.15 mm (.005 inch) and 0.30 mm (.011 inch) from the terminal tip.
4. The configuration of the pin 1 identifier is optional, but must be located within the zone indicated. The pin 1 identifier may be either a mold or mark feature.
5. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
6. Nominal dimensions are provide to assist with printed circuit board land pattern design efforts, see manufacturer's technical brief TB389.
7. Fall within JEDEC MO-229-WEED-3 except for dimensions E2 and D2.

FIGURE 1. Case outline - Continued.

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Device type	01		
Case outline	X		
Terminal number	Terminal symbol	Type	Description
1	V _{IN}	Analog I/O	Supply voltage / low dropout (LDO) regulator input: Connect a 1 μF capacitor to GND.
2	EN1	Low voltage compatible CMOS input	LDO – 1 enable
3	EN2	Low voltage compatible CMOS input	LDO – 2 enable
4	C _{BYP}	Analog I/O	Reference bypass capacitor pin: Optionally connect capacitor of value 0.01 μF to 1 μF between this pin and GND to tune in the desired noise and PSRR performance.
5	C _{POR}	Analog I/O	POR2 delay setting capacitor pin: Connect a capacitor between this pin and GND to delay the POR2 output release after LDO-2 output reaches 94% of its specified voltage level. (200 ms delay per 0.01 μF).
6	GND	Ground	GND is the connection to system ground. Connect to printed circuit board ground plane.
7	$\overline{\text{POR1}}$	Open drain output (1 mA)	Open drain POR output for LDO-1 (active low): Internally connected to VO1 through 100 kΩ resistor.
8	$\overline{\text{POR2}}$	Open drain output (1 mA)	Open drain POR output for LDO-2 (active low): Internally connected to VO2 through 100 kΩ resistor.
9	VO2	Analog I/O	LDO-2 output: Connect capacitor of value 1 μF to 10 μF to GND (1 μF recommended).
10	VO1	Analog I/O	LDO-1 output: Connect capacitor of value 1 μF to 10 μF to GND (1 μF recommended).

FIGURE 2. Terminal connections.

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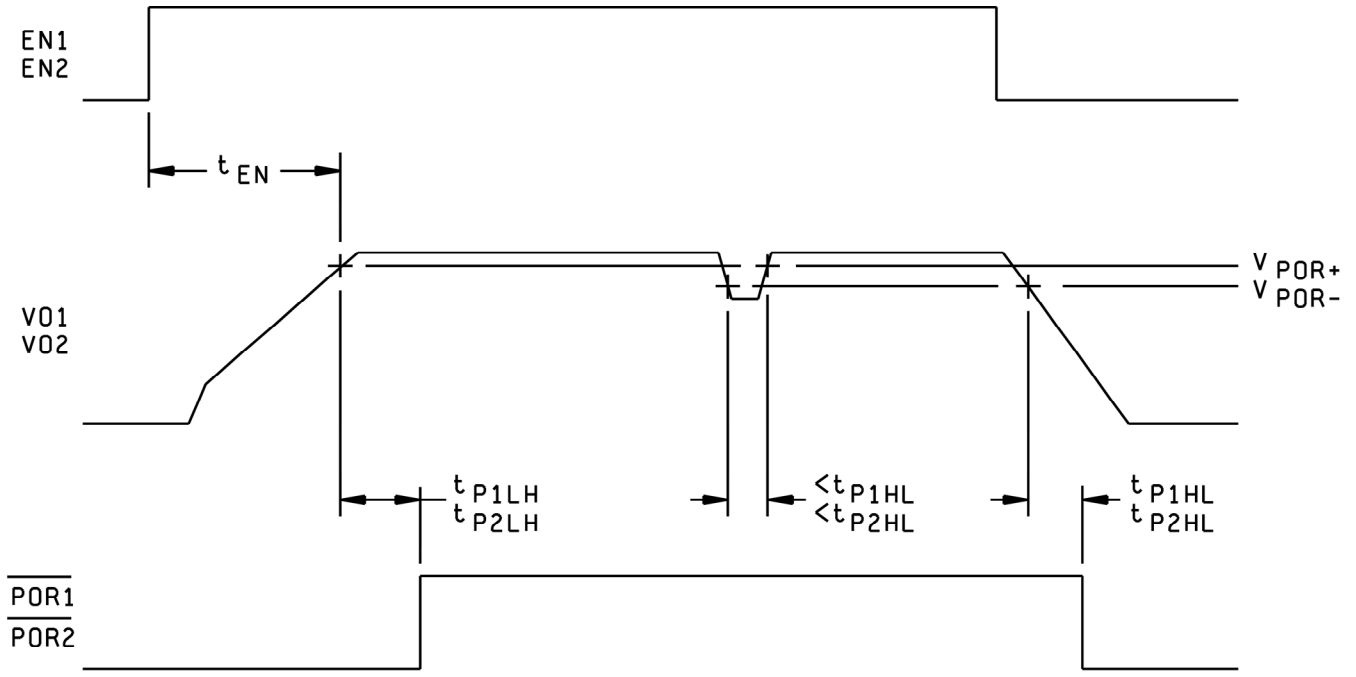


FIGURE 4. Timing waveforms.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer’s standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer’s data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number <u>2/</u>
V62/08609-01XB	<u>3/</u>	ISL9000AMRNCEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ Add –TK suffix to vendor part number for 1000 piece quantity with tape and reel packing option.

3/ Not available from an approved source of supply. The last known supplier is listed below.

CAGE code

34371

Source of supply

Renesas Electronics America Inc
1650 Robert J Conlan Blvd NE
Palm Bay, FL 32905-3406

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