REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Add device type 01. Make changes to V_{IL} and V_{IH}. Update unreleased vendor part numbers from “REP” to “TEP”. - ro	08-11-20	R. HEBER
B	Add footnotes and make changes to HBM and CDM ESD limits under paragraph 1.3. Add power up reset voltage parameter to paragraph 1.4. Add paragraph 1.5 Thermal characteristics. Add JEDEC references under section 2. Add typical limits to Table I parameters. Update the document paragraphs to current requirements. - ro	15-05-13	C. SAFFLE
C	Update JEDEC package from MO-178-AB to MO-178 and make change to “L” max dimension. Add JEDEC references under section 2. Add I/O column to figure 2 Terminal connections. Update document paragraphs to current requirements. - ro	20-11-04	J. ESCHMEYER

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	**REV**			C	C	C	C	C	C	C	C	C	C	C	C							
	PAGE			1	2	3	4	5	6	7	8	9	10	11	12							

PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 08-08-07	**CHECKED BY** RAJESH PITHADIA	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, PROGRAMMABLE DELAY SUPERVISORY CIRCUIT, MONOLITHIC SILICON
	APPROVED BY ROBERT M. HEBER	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/08607**
	REV **C**	**PAGE** 1 **OF** 12

AMSC N/A

5962-V081-20

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance programmable delay supervisory circuit microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/08607	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Nominal supply voltage	Threshold (V_{IT}) voltage	Circuit function
01	TPS3808G01	Adjustable	0.405 V	Programmable delay supervisory circuit
02	TPS3808G09	0.9 V	0.84 V	Programmable delay supervisory circuit
03	TPS3808G12	1.2 V	1.12 V	Programmable delay supervisory circuit
04	TPS3808G125	1.25 V	1.16 V	Programmable delay supervisory circuit
05	TPS3808G15	1.5 V	1.40 V	Programmable delay supervisory circuit
06	TPS3808G18	1.8 V	1.67 V	Programmable delay supervisory circuit
07	TPS3808G25	2.5 V	2.33 V	Programmable delay supervisory circuit
08	TPS3808G30	3.0 V	2.79 V	Programmable delay supervisory circuit
09	TPS3808G33	3.3 V	3.07 V	Programmable delay supervisory circuit
10	TPS3808G50	5.0 V	4.65 V	Programmable delay supervisory circuit

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	6	MO-178	Plastic surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Input voltage range (V_{DD}) ..... -0.3 V to 7.0 V
C_T voltage range (V_{CT}) ..... -0.3 V to V_{DD} + 0.3 V
Other voltage ranges: V_{RESET}, V_{MR}, V_{SENSE} ..... -0.3 V to 7 V
$\overline{RESET}$ pin current ..... 5 mA maximum
Operating junction temperature (T_J) ..... -55°C to +150°C 2/
Storage temperature range (Tstg) ..... -65°C to +150°C
Electrostatic discharge (ESD) rating:
Human body model (HDM), per JEDEC JS-001, all pins ..... ±3000 V 3/
Charge device model (CDM), per JEDEC JESD22-C101, all pins ..... ±1000 V 4/
Thermal resistance, junction to case (θ_{JC}) ..... 55°C/W
Thermal resistance, junction to ambient (θ_{JA}) ..... 290°C/W typical

1.4 Recommended operating conditions. 5/

Input supply voltage range (V_{DD}) ..... 1.7 V to 6.5 V
Power up reset voltage (V_{OL}(max) = 0.2 V, $I_{\overline{RESET}}$ = 15 μA) ..... 0.8 V
Operating free-air temperature range (T_A) ..... -55°C to +125°C

1.5 Thermal characteristics.

Thermal metric	Symbol	Case X	Unit
Thermal resistance, junction-to-ambient	θ_{JA}	180.9	°C/W
Thermal resistance, junction-to-case (top)	$\theta_{JC(TOP)}$	117.8	°C/W
Thermal resistance, junction-to-board	θ_{JB}	27.8	°C/W
Characterization parameter, junction-to-top	ψ_{JT}	1.12	°C/W
Characterization parameter, junction-to-board	ψ_{JB}	27.3	°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.
3/ JEDEC document JEP 155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
4/ JEDEC document JEP 157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.
5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC JS-001	-	Human Body Model Testing of Integrated Circuits
JESD22-C101	-	Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronics Components
JEDEC PUB 95	-	Registered and Standard Outlines for Semiconductor Devices
JEDEC JEP 155	-	Recommended ESD Target Levels for HBM/MM Qualification
JEDEC JEP 157	-	Recommended ESD-CDM Target Levels

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Input supply range	V_{DD}		-55°C to +125°C	All	1.7	6.5	V
Supply current (current into V_{DD} pin)	I_{DD}	V_{DD} = 3.3 V, $\overline{RESET}$ not asserted $\overline{MR}$, $\overline{RESET}$, C_T open	-55°C to +125°C	All		5.0	µA
					2.4 typical		
		V_{DD} = 6.5 V, $\overline{RESET}$ not asserted $\overline{MR}$, $\overline{RESET}$, C_T open				6.0	
					2.7 typical		
Low level output voltage	V_{OL}	1.3 V ≤ V_{DD} < 1.8 V, I_{OL} = 0.4 mA	-55°C to +125°C	All		0.3	V
		1.8 V ≤ V_{DD} ≤ 6.5 V, I_{OL} = 1.0 mA				0.4	
Power up reset 3/ voltage		V_{OL} (max) = 0.2 V, $I_{\overline{RESET}}$ = 15 µA	-55°C to +125°C	All		0.8	V
Negative going input threshold accuracy	V_{IT}		-55°C to +125°C	01	-2.0	+2.0	%
					±1.0 typical		
		V_{IT} ≤ 3.3 V		02 - 09	-1.7	+1.7	
					±0.5 typical		
		3.3 V < V_{IT} ≤ 5.0 V		10	-2.0	+2.0	
					±1.0 typical		
Hysteresis on V_{IT} pin	V_{HYS}		-55°C to +125°C	01		3.0	%V_{IT}
					1.5 typical		
				02 - 10		2.5	
					1.0 typical		
$\overline{MR}$ internal pullup resistance	$R_{\overline{MR}}$		-55°C to +125°C	All	70		kΩ
					90 typical		
Input current at SENSE pin	I_{SENSE}	V_{SENSE} = V_{IT}	-55°C to +125°C	01	-25	25	nA
		V_{SENSE} = 6.5 V	+25°C	02 - 10	1.7 typical		µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
$\overline{\text{RESET}}$ leakage current	I_{OH}	$V_{\overline{\text{RESET}}}$ = 6.5 V, $\overline{\text{RESET}}$ not asserted	-55°C to +125°C	All		300	nA
Input capacitance, any pin	C_{IN}	C_T pin, V_{IN} = 0 V to V_{DD}	+25°C	All	5 typical		pF
		Other pins, V_{IN} = 0 V to 6.5 V			5 typical		
$\overline{\text{MR}}$ logic low input	V_{IL}		-55°C to +125°C	All	0	0.3 V_{DD}	V
$\overline{\text{MR}}$ logic high input	V_{IH}		-55°C to +125°C	All	0.7 V_{DD}	V_{DD}	V
Input pulse width to $\overline{\text{RESET}}$	t_W	SENSE, V_{IH} = 1.05 V_{IT}, V_{IL} = 0.95 V_{IT}	+25°C	All	20 typical		µs
		$\overline{\text{MR}}$, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}			0.001 typical		
$\overline{\text{RESET}}$ delay time	t_d	C_T = open, see figure 4	-55°C to +125°C	All	12	29	ms
					20 typical		
		C_T = V_{DD}, see figure 4			180	440	
					300 typical		
		C_T = 100 pF, see figure 4			0.75	1.8	
					1.25 typical		
		C_T = 180 nF, see figure 4			0.7	1.8	s
					1.2 typical		
Propagation delay	t_{PHL}	$\overline{\text{MR}}$ to $\overline{\text{RESET}}$, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}	+25°C	All	150 typical		ns
High to low level $\overline{\text{RESET}}$ delay	t_{PHL}	SENSE to $\overline{\text{RESET}}$, V_{IH} = 1.05 V_{IT}, V_{IL} = 0.95 V_{IT}	+25°C	All	20 typical		ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, 1.7 V ≤ V_{DD} ≤ 6.5 V, R_{LRESET} = 100 kΩ, C_{LRESET} = 50 pF.

3/ The lowest supply voltage (V_{DD}) at which $\overline{\text{RESET}}$ becomes active. $t_{rise(VDD)}$ ≥ 15 µs / V.

Case X

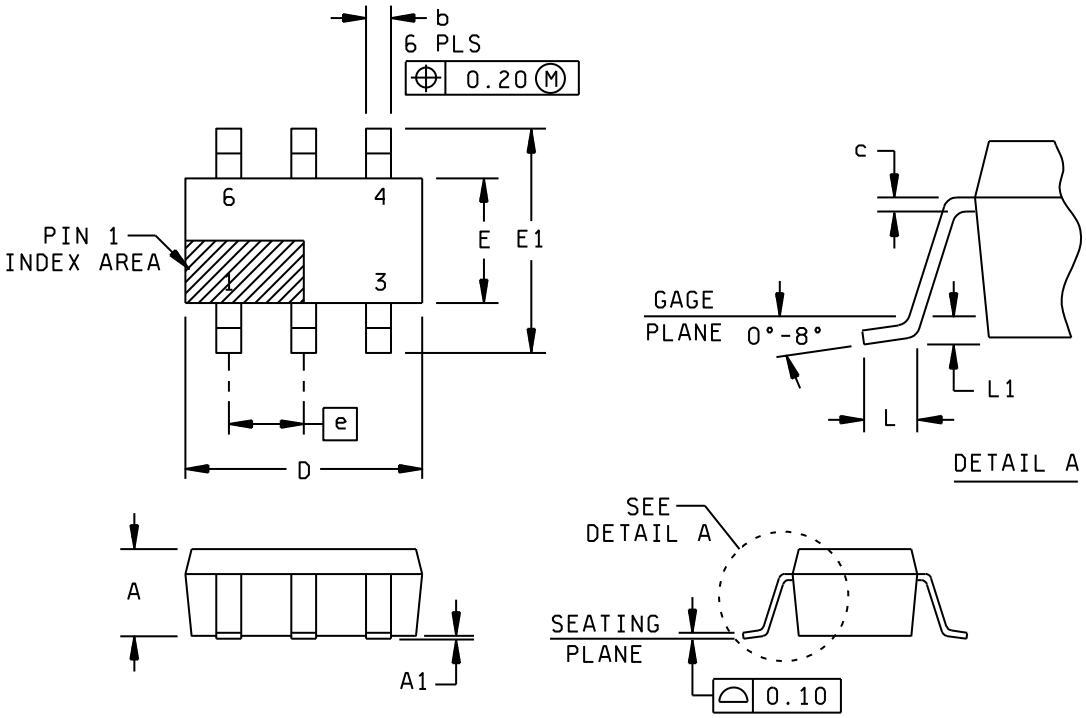

FIGURE 1. Case outline.

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Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	.057	---	1.45
A1	.000	.005	0.00	0.15
b	.009	.019	0.25	0.50
c	.003	.008	0.08	0.22
D	.108	.120	2.75	3.05
E	.057	.068	1.45	1.75
E1	.102	.118	2.60	3.00
e	.037 BSC		0.95 BSC	
L	.011	.024	0.30	0.60
L1	.009 BSC		0.25 BSC	
n	6		6	

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 mm (0.005 inch) per side.
3. Leads 1, 2, 3 may be wider than leads 4, 5, 6 for package orientation.
4. Falls within JEDEC MO-178.

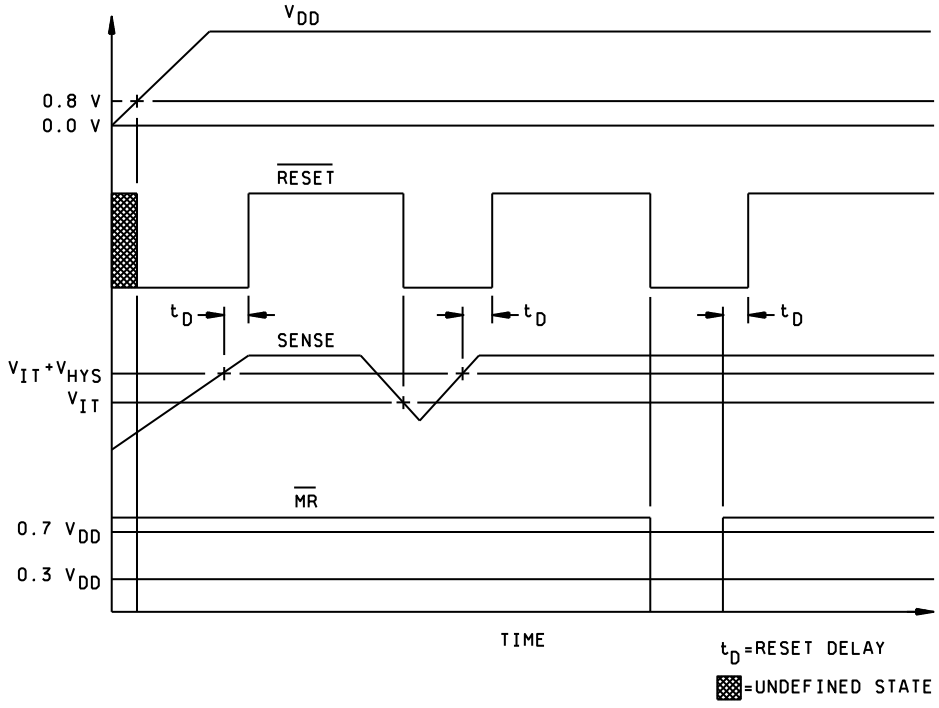
FIGURE 1. Case outline – Continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	I/O	Description
1	$\overline{\text{RESET}}$	O	$\overline{\text{RESET}}$ is an open drain output that is driven to a low impedance state when $\overline{\text{RESET}}$ is asserted (either the SENSE input is lower than the threshold voltage (V_{IT}) or the $\overline{\text{MR}}$ pin is set to a logic low). $\overline{\text{RESET}}$ remains low (asserted) for the reset period after both SENSE is above V_{IT} and $\overline{\text{MR}}$ is set to a logic high. A pullup resistor from 10 kΩ to 1 MΩ should be used on this pin, and allows the reset pin to attain voltages higher than V_{DD}.
2	GND	---	Ground.
3	$\overline{\text{MR}}$	I	Driving the manual reset pin ($\overline{\text{MR}}$) low asserts $\overline{\text{RESET}}$. $\overline{\text{MR}}$ is internally tied to V_{DD} by a 90 kΩ pullup resistor.
4	C_T	I	Reset period programming pin. Connecting this pin to V_{DD} through a 40 kΩ to 200 kΩ resistor or leaving it open results in fixed delays times. Connecting this pin to a ground referenced capacitor ≥ 100 pF gives a user programmable delay time.
5	SENSE	I	This pin is connected to the voltage to be monitored. If the voltage at this terminal drops below the threshold voltage V_{IT}, then $\overline{\text{RESET}}$ is asserted.
6	V_{DD}	I	Supply voltage. It is good analog design practice to place a 0.1 μF ceramic capacitor close to this pin.

FIGURE 2. Terminal connections.

$\overline{MR}$	SENSE > VIT	$\overline{RESET}$
L	0	L
L	1	L
H	0	L
H	1	H

FIGURE 3. Truth table.



$\overline{MR}$ and SENSE reset timing

FIGURE 4. Timing diagram.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/ 2/ 3/	Device manufacturer CAGE code	Nominal 4/ supply voltage	Vendor part number
V62/08607-01XE	01295	Adjustable	TPS3808G01MDBVTEP
V62/08607-02XE	5/	0.9 V	TPS3808G09MDBVTEP
V62/08607-03XE	5/	1.2 V	TPS3808G12MDBVTEP
V62/08607-04XE	5/	1.25 V	TPS3808G125MDBVTEP
V62/08607-05XE	5/	1.5 V	TPS3808G15MDBVTEP
V62/08607-06XE	5/	1.8 V	TPS3808G18MDBVTEP
V62/08607-07XE	5/	2.5 V	TPS3808G25MDBVTEP
V62/08607-08XE	5/	3.0 V	TPS3808G30MDBVTEP
V62/08607-09XE	01295	3.3 V	TPS3808G33MDBVREP
V62/08607-10XE	5/	5.0 V	TPS3808G50MDBVTEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's data sheet.
3/ Package drawings, thermal data, and symbolization are available from the manufacturer.
4/ Customer threshold voltages from 0.82 V to 3.3 V, 4.4 V to 5.0 V are available through the use of factory EEPROM programming. Minimum order quantities apply. Contact factory for details and availability.
5/ Not available from an approved source of supply.

6.3 Suggested source(s) of supply - continued.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243