

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	16-11-28	Thomas M. Hess
B	Add Maximum Junction Temperature , Machine Model. and Thermal resistance in section 1.3. Modify Power rating in section 1.4. Add minimum limit Power on Recall voltage; change input buffer to HIGH voltage in V _{IH} ; change test condition in t _{BUF} ; Modify T _{MIN} test temperature in foot note 10 and 16; change RMATCH in footnote 15 in Table I. -PHN	16-12-06	Thomas M. Hess
C	Make change to the lead finish designator from "E" to "B". - ro	22-06-01	James R. Eschmeyer



Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

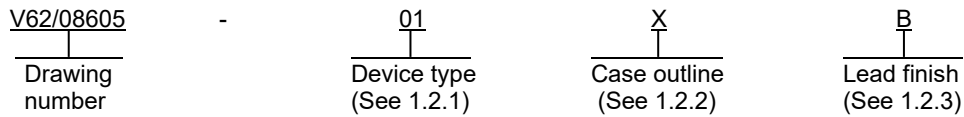
REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C	C	C	C							
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13							

PMIC N/A Original date of drawing 08-01-07	PREPARED BY Phu H. Nguyen					DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/landandmaritime									
	CHECKED BY Phu H. Nguyen					TITLE MICROCIRCUIT, DIGITAL, CMOS, QUAD DIGITALLY CONTROLLED POTENTIOMETERS, MONOLITHIC SILICON									
	APPROVED BY Thomas M. Hess														
	SIZE A		CAGE CODE 16236			DWG NO. V62/08605									
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual digitally controlled potentiometers microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	ISL22346	Quad digitally controlled potentiometers

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	20	MO-153	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range (VCC).....	-0.3 V to 6.0 V
Voltage at any digital interface pin with respect to GND	-0.3 V to VCC + 0.3 V
Voltage at any DCP pin with respect to GND	-0.3 V to VCC
Lead temperature (soldering, 10 seconds)	300°C
IW (10 seconds)	±6 mA
Latch up	Class II, Level B at +125°C <u>2/</u>
Maximum Junction Temperature.....	+150°C
Storage temperature range (T _{STG})	-65°C to 150°C
Electrostatic discharge (ESD) rating :	
Human body model (HBM)	2.5 kV
Charge device model (CDM)	1 kV
Machine model (MM)	350 V
Thermal resistance (θJA) (case X)	95°C/W <u>3/</u>

1.4 Recommended operating conditions.

Supply voltage range (VCC).....	2.7 V to 5.5 V
Power rating of each DCP	15 mW
Wiper current of each DCP	±3.0 mA
Operating free-air temperature range (TA).....	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ JEDEC class II pulse conditions and failure criterion used. Level B exceptions are: using a max positive pulse of 6.5 V on the SHDN pin, and using a max negative pulse of -0.8 V for all pins.

3/ θJA is measured with the component mounted on a high effective thermal conductivity test board in free air. See manufacturer data for more information.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions <u>2/</u> unless otherwise specified	Limits		Unit
			Min	Max	
RH to RL resistance	RTOTAL	W option <u>3/</u>	10 typical		kΩ
RH to RL resistance tolerance	RTOTAL	W option	-20	+20	%
End to end temperature coefficient	RTOTAL	W option <u>3/</u>	±50 typical		ppm/°C <u>16/</u>
Wiper resistance	RW	VCC = 3.3 V, TA = +25°C, wiper current = VCC/RTOTAL		200	Ω
VRH and VRL terminal voltage	VRH, VRL	VRH and VRL to GND	0	VCC	V
Potentiometer capacitance	CH/ CL/ CW <u>3/</u>		10/ 10/ 25 typical		pF
Leakage on DCP pins	ILkgDCP	Voltage at pin from GND to VCC		1	μA
Voltage divider mode (0 V atRLi; VCC at RHi; measured at Rwi, unloaded; i = 0, 1, 2, or 3)					
Integral non-linearity	INL <u>4/</u>	Monotonic over all tap positions	-1	1	LSB <u>5/</u>
Differential non linearity	DNL <u>6/</u>	Monotonic over all tap positions	-1	1	LSB <u>5/</u>
Zero scale error	ZSerror <u>7/</u>	W option	0	5	LSB <u>5/</u>
Full scale error	FSerror <u>8/</u>	W option	-5	0	LSB <u>5/</u>
DCP to DCP matching	VMATCH <u>9/</u>	Any two DCPs at same tap position, same voltage at all RH terminals, and same voltage at all RL terminals.	-2	2	LSB <u>5/</u>
Ratiometric temperature coefficient	TCV <u>3/ 10/</u>	DCP register set to 40 hex	±4 typical		ppm/°C
Resistor mode (Measurements between Rwi and RLi with RHi not connected, or between Rwi and RHi with RLi not connected, i = 0 or 1)					
Integral non-linearity	RINL <u>11/</u>	DCP register set between 10h and 7Fh; monotonic over all tap positions	-1	1	MI <u>12/</u>
Differential non-linearity	RDNL <u>13/</u>	DCP register set between 10h and 7Fh; monotonic over all tap positions	-1	1	MI <u>12/</u>
Offset	Roffset <u>14/</u>	W option	0	5	MI <u>12/</u>
DCP to DCP matching	RMATCH <u>15/</u>	Any two DCPs at the same tap position with the same terminal voltages	-2	2	MI <u>12/</u>

See footnote at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u> unless otherwise specified	Limits		Unit
			Min	Max	
VCC Supply current (volatile write/read)	ICC1	fSCL = 400 kHz; SDA = Open; (for I ² C, active, read and write states)		0.5	mA
VCC Supply current (non-volatile write/read)	ICC2	fSCL = 400 kHz; SDA = Open; (for I ² C, active, read and write states)		3	mA
VCC current (standby)	I _{sb}	VCC = 5.5 V at I ² C interface in standby state		7	μA
		VCC = 3.6 V at I ² C interface in standby state		5	
VCC current (shutdown)	I _{sd}	VCC = 5.5 V at I ² C interface in standby state		5	μA
		VCC = 3.6 V at I ² C interface in standby state		4	
Leakage current at pins A0, A1, A2, $\overline{\text{SHDN}}$, SDA, and SCL	I _{LkgDig}	Voltage at pin from GND to VCC	-1	1	μA
DCP wipe response time	t _{WRT} <u>3/</u>	SCL falling edge of last bit of DCP data byte to wiper new position	1.5 typical		μs
DCP recall time from shutdown mode	t _{ShdnRec}	From rising edge of $\overline{\text{SHDN}}$ signal to wiper stored position and RH connection	1.5 typical		μs
	<u>3/</u>	SCL falling edge of last bit of ACR data byte to wiper stored position and RH connection	1.5 typical		
Power on recall voltage	V _{por}	Minimum VCC at which memory recall occurs	2.0	2.6	V
VCC ramp rate	VCC _{ramp}		0.2		V/ms
Power up delay	t _D	VCC above V _{por} , to DCP initial value register recall completed, and I ² C interface stand by state		3	ms

EEPROM specification

EEPROM endurance			1,000,000		Cycles
EEPROM retention		Temperature T ≤ 55°C	50		Years
EEPROM retention		Temperature T ≤ 90°C	15		Years
EEPROM retention		Temperature T ≤ 125°C	10		Years
Non-volatile write cycle time	t _{WC} <u>17/</u>			20	ms

Serial interface specs

A2, A1, A0, $\overline{\text{SHDN}}$, SDA, and SCL input buffer LOW voltage	V _{IL}		-0.3	0.3*VCC	V
A2, A1, A0, $\overline{\text{SHDN}}$, SDA, and SCL input buffer HIGH voltage	V _{IH}		0.7*VCC	VCC+0.3	V
SDA and SCL input buffer Hysteresis	Hysteresis		0.05*VCC		V

See footnote at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	Limits		Unit
			Min	Max	
Serial interface specs - Continued					
SDA output buffer LOW voltage, sinking 4 mA	VOL		0	0.4	V
A2, A1, A0, $\overline{\text{SHDN}}$, SDA, and SCL pin capacitance	Cpin 3/		10 typical		pF
SCL frequency	fSCL			400	kHz
Pulse width suppression time at SDA and SCL inputs	tsp	Any pulse narrower than the max spec is suppressed		50	ns
SCL falling edge to SDA output data valid	tAA	SCL falling edge crossing 30% of VCC, until SDA exits the 30% to 70% of VCC window		900	ns
Time the bus must be free before the start of a new transmission	tBUF	SDA crossing 70% of VCC during a STOP condition, to SDA crossing 70% of VCC during the following START condition	1300		ns
Clock LOW time	tLOW	Measured at the 30% of VCC crossing	1300		ns
Clock HIGH tim	tHIGH	Measured at the 70% of VCC crossing	600		ns
START condition setup time	tSU:STA	SCL rising edge to SDA falling edge; both crossing 70% of VCC	600		ns
START condition hold time	tHD:STA	From SDA falling edge crossing 30% of VCC to SCL falling edge crossing 70% of VCC	600		ns
Input data setup time	tSU:DAT	From SDA exiting the 30% to 70% of VCC window, to SCL rising edge crossing 30% of VCC	100		ns
Input data hold time	tSU:DAT	From SCL rising edge crossing 70% of VCC to SDA entering the 30% to 70% of VCC window	0		ns
STOP condition setup time	tSU:STO	From SCL rising edge crossing 70% of VCC, to SDA rising edge crossing 30% of VCC	600		ns
STOP condition hold time for Read or Volatile only Write	tHD:STO	From SDA rising edge to SCL falling edge; both crossing 70% of VCC	1300		ns
Output data hold time	tDH	From SCL falling edge crossing 30% of VCC, until SDA enters the 30% to 70% of VCC window	0		ns
SDA and SCL rise time	tR	From 30% to 70% of VCC	20 + 0.1*Cb	250	ns
SDA and SCL fall time	tF	From 70% to 30% of VCC	20 + 0.1*Cb	250	ns
Capacitive loading of SDA or SCL	Cb	Total on chip and off chip	10	400	pF
SDA and SCL bus pull up resistor off chip	Rpu	Maximum is determined by tR and tF, For Cb = 400 pF, max is about 2 ~ 2.5 k Ω , For Cb = 40 pF, max is about 15 ~ 20 k Ω	1		k Ω
A2, A1 and A0 setup time	tSU:A	Before START condition	600		ns
A2, A1, and A0 hold time	tHD:A	After STOP condition	600		ns

See footnote at end of table.

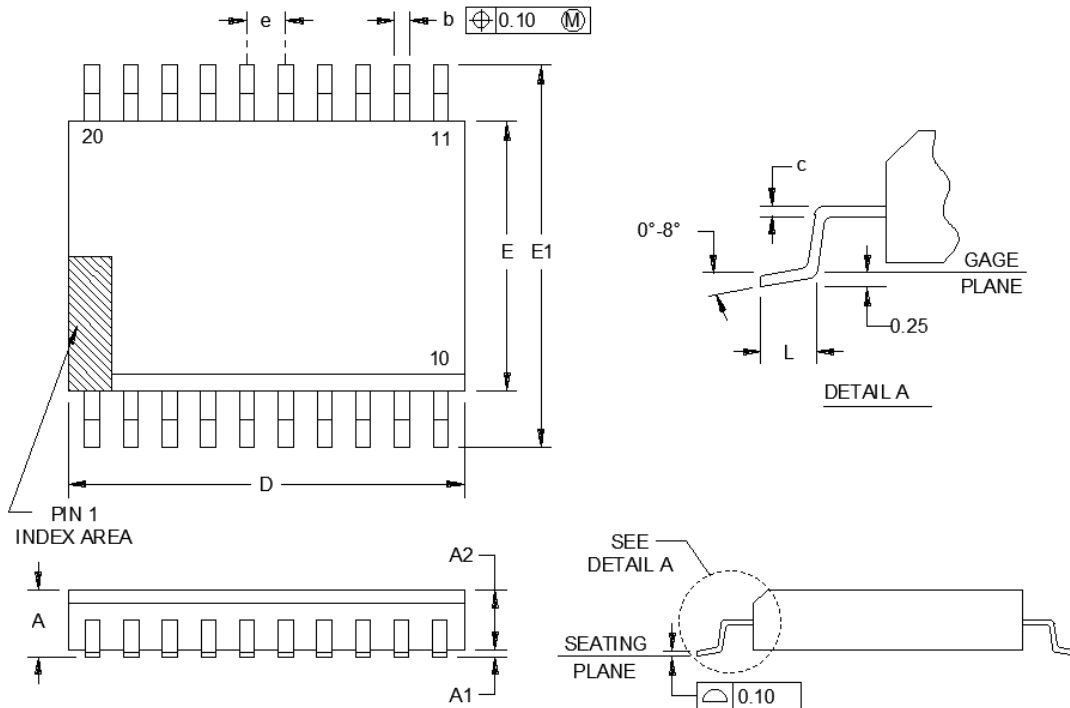
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TABLE I. Electrical performance characteristics – Continued. 1/

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Over recommended operating conditions. All typical values are for TA = +25°C and 3.3 V supply voltage.
- 3/ This parameter is not 100% tested.
- 4/ $INL = [V(RW)_i - i * LSB - V(RW)_0]/LSB$ for $i = 1$ to 127.
- 5/ $LSB: [V(RW)_{127} - V(RW)_0]/127$. $V(RW)_{127}$ and $V(RW)_0$ are $V(RW)$ for the DCP register set to 7F hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
- 6/ $DNL = [V(RW)_i - V(RW)_{i-1}]/LSB-1$, for $i = 1$ to 127. i is the DCP register setting.
- 7/ $ZS\ error = V(RW)_0/LSB$.
- 8/ $FS\ error = [V(RW)_{127} - VCC]/LSB$.
- 9/ $VMATCH = [V(RW_x)_i - V(RW_y)_i]/LSB$, for $i = 1$ to 127, $x = 0$ to 3 and $y = 0$ to 3.
- 10/ $TC_V = \frac{Max(V(RW)_i) - Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)] / 2} \times \frac{10^6}{165^\circ C}$ for $i = 16$ to 112 decimal, $T = -55^\circ C$ to $+125^\circ C$. $Max()$ is the maximum value of the wiper voltage and $Min()$ is the minimum value of the wiper voltage over the temperature range
- 11/ $RINL = [RW_i - M(MI * i) - RW_0]/MI$ for $i = 16$ to 127.
- 12/ $MI = [RW_{127} - RW_0]/127$. MI is a minimum increment. RW_{127} and RW_0 are the measured resistances for the DCP register set to 7F hex and 00 hex respectively.
- 13/ $RDNL = [RW_i - RW_{i-1}]/MI-1$, for $i = 16$ to 127.
- 14/ $Roffset = RW_0/MI$, when measured between RW and RL.
 $Roffset = RW_{127}/MI$ when measured between RW and RH.
- 15/ $RMATCH = (RW_{i,x} - RW_{i,y})/MI$, for $i = 1$ to 127, $x = 0$ to 3 and $y = 0$ to 3.
- 16/ $TC_R = \frac{Max(R_i) - Min(R_i)}{[Max(R_i) + Min(R_i)] / 2} \times \frac{10^6}{165^\circ C}$ for $i = 16$ to 112, $T = -55^\circ C$ to $+125^\circ C$. $Max()$ is the maximum value of the resistance and $Min()$ is the minimum value of the resistance over the temperature range
- 17/ t_{WC} is the time from a valid STOP condition at the end of a Write sequence I²C serial interface, to the end of the self timed internal non-volatile write cycle.

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Case X



Dimension					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	e	0.65 BSC	
A1	0.05	0.15	E	4.30	4.50
A2	0.80	1.05	E1	6.25	6.50
b	0.19	0.30	L	0.45	0.75
c	0.09	0.20	α	0°	8°
D	6.40	6.60			

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153 AC.
2. Body dimensions do not include mold flash, protrusion or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 0.15 mm per side.
3. "L" is the length of terminal for soldering to a substrate.
4. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07 mm.

FIGURE 1. Case outline.

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Case X

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	RH3	11	RW1
2	RL3	12	RL1
3	RW3	13	RH1
4	A2	14	A0
5	SCL	15	A1
6	SDA	16	VCC
7	GND	17	SHDN
8	RW2	18	RH0
9	RL2	19	RL0
10	RH2	20	RW0

FIGURE 2. Terminal connections.

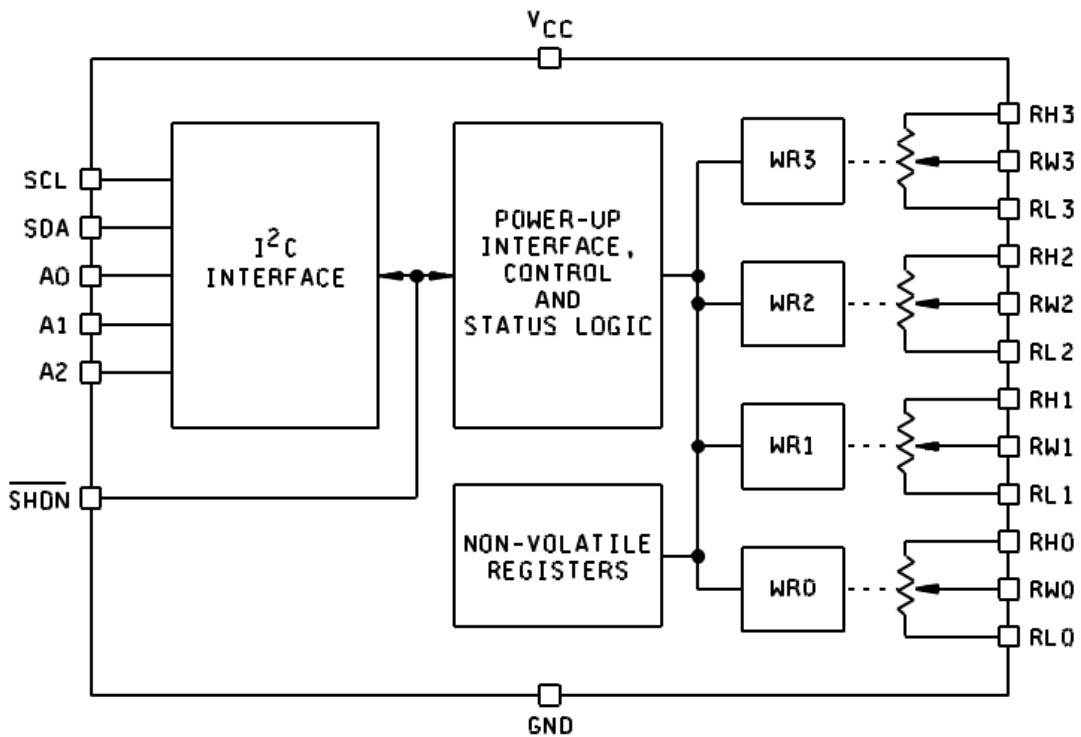
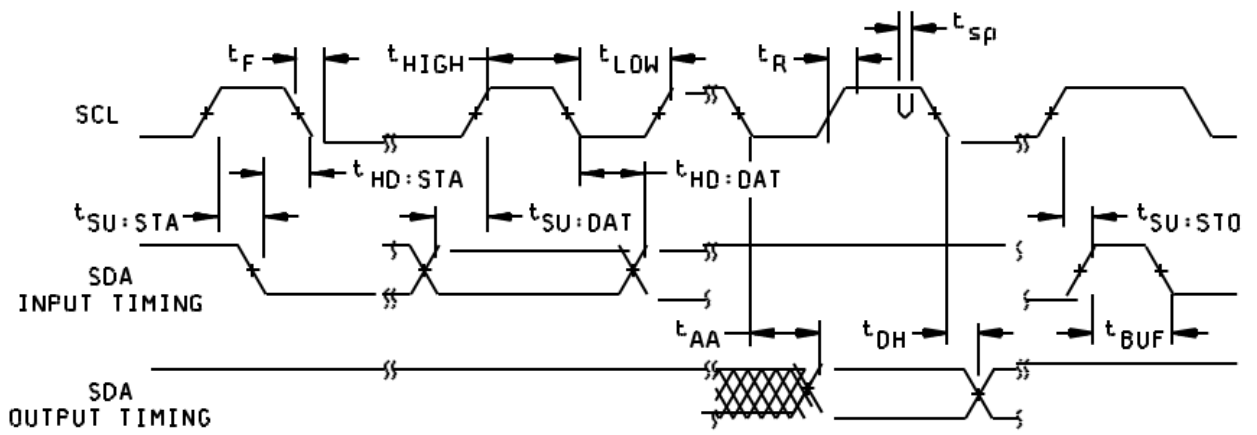
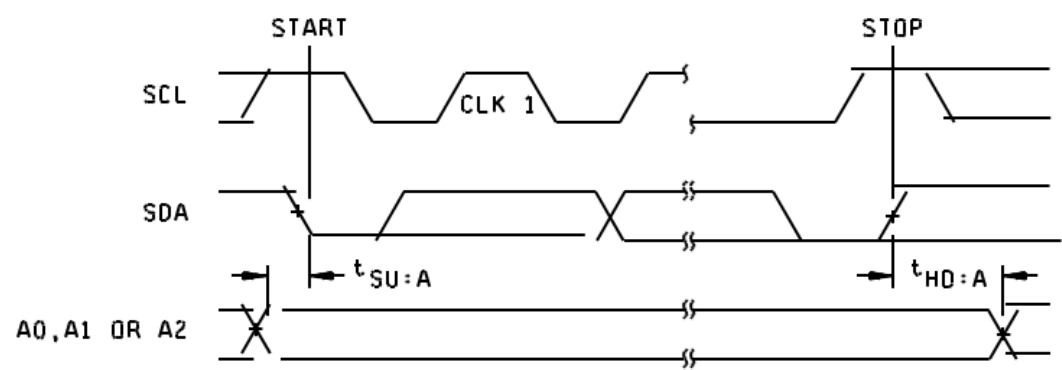


FIGURE 3. Block diagram.

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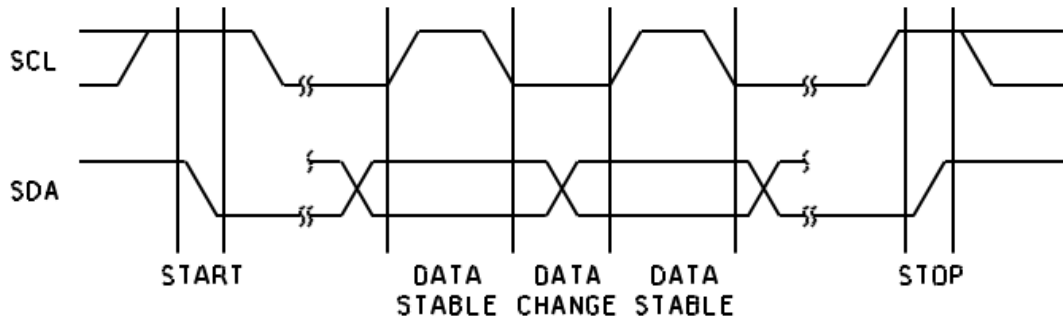
SDA vs SCL TIMING



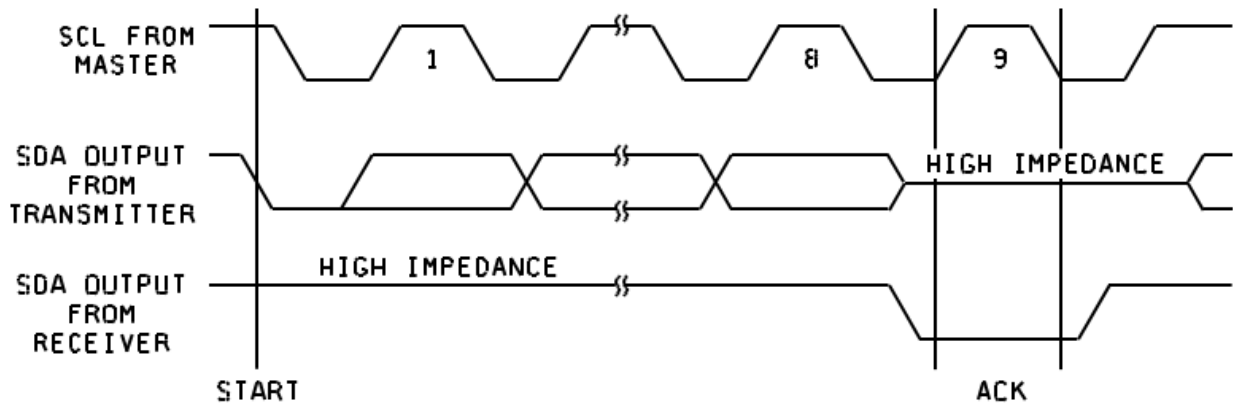
A0, A1, AND A2 PIN TIMING

FIGURE 4. Timing waveforms.

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VALID DATA CHANGES, START AND STOP CONDITIONS



ACKNOWLEDGE RESPONSE FROM RECEIVER

FIGURE 4. Timing waveforms - Continued.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Top side marking <u>2/</u>	Vendor part number
V62/08605-01XB	34371	22346WMVEP	ISL22346WMVEP
V62/08605-01XE	<u>3/</u>	22346WMVEP	ISL22346WMVEP

- 1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
- 2/ Add -TK suffix to vendor part number for 1000 piece quantity with tape and reel packaging option.
- 3/ This device with gold flash palladium lead finish is no longer available from an approved source of supply.

CAGE code

34371

Source of supply

Renesas Electronics America
1650 Robert J. Conlan Blvd. NE
Palm Bay, FL 32905-3406

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