

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual digitally controlled potentiometers microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/08604</u> Drawing number	-	<u>01</u> Device type (See 1.2.1)	<u>X</u> Case outline (See 1.2.2)	<u>E</u> Lead finish (See 1.2.3)
---------------------------------------	---	---	---	--

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	ISL22326	Dual digitally controlled potentiometers

1.2.2 Case outline(s). The case outlines are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	14	MO-153	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/08604
		REV B	PAGE 2

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.3 V to 6.0 V
Voltage at any digital interface pin with respect to GND	-0.3 V to $V_{CC} + 0.3$ V
Voltage at any DCP pin with respect to GND	-0.3 V to V_{CC}
Lead temperature (Soldering, 10s)	300°C
I_w (10s)	±6 mA
Latch up	Class II, Level B @ +125°C 2/
Storage temperature range (T_{STG})	-65°C to 150°C
Maximum Junction Temperature.....	+150°C
ESD :	
(HBM)	2.5 kV
(CDM)	1 kV
(MM).....	350 V
Thermal resistance (θ_{JA}) (case X)	100°C/W 3/

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	2.7 V to 5.5 V
Power rating of each DCP	15 mW
Wiper current of each DCP	±3.0 mA
Operating free-air temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

2/ JEDEC class II pulse conditions and failure criterion used. Level B exceptions are: using a max positive pulse of 6.5 V on the SHDN pin, and using a max negative pulse of -0.8 V for all pins.

3/ θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See manufacturer data for more information.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/08604
		REV B	PAGE 3

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/08604
		REV B	PAGE 4

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions <u>2/</u> unless otherwise specified	Limits		Unit
			Min	Max	
R _H to R _L resistance	R _{TOTAL}	W option <u>3/</u>	10 TYP		kΩ
R _H to R _L resistance tolerance		W option	-20	+20	%
End to end temperature coefficient		W option <u>3/</u>	±50 TYP		ppm/°C <u>16/</u>
Wiper resistance	R _W	V _{CC} = 3.3 V, T _A = +25°C, wiper current = V _{CC} /R _{TOTAL}		200	Ω
VR _H and VRL terminal voltage	V _{RH} , V _{RL}	V _{RH} and V _{RL} to GND	0	V _{CC}	V
Potentiometer capacitance	C _H / C _L / C _W <u>3/</u>		10/ 10/ 25 TYP		pF
Leakage on DCP pins	I _{LkgDCP}	Voltage at pin from GND to V _{CC}		1	μA

Voltage divider mode (0V @ R_{Li}; V_{CC} @ R_{Hi}; measured at R_{wi}, unloaded; I = 0 or 1)

Integral non-linearity	INL <u>4/</u>	Monotonic over all tap positions	-1	1	LSB <u>5/</u>
Differential non linearity	DNL <u>6/</u>	Monotonic over all tap positions	-1	1	
Zero scale error	ZSerror <u>7/</u>	W option	0	5	
Full scale error	FSerror <u>8/</u>	W option	-5	0	
DCP to DCP matching	V _{MATCH} <u>9/</u>	Any two DCPs at same tap position, same voltage at all R _H terminals, and same voltage at all R _L terminals.	-2	2	
Ratiometric temperature coefficient	TC _V <u>3/ 10/</u>	DCP register set to 40 hex	±4 TYP		ppm/°C

Resistor mode (Measurements between R_{wi} and R_{Li} with R_{Hi} not connected, or between R_{wi} and R_{Hi} with R_{Li} not connected, i = 0 or 1)

Integral non-linearity	RINL <u>11/</u>	DCP register set between 10h and 7Fh; monotonic over all tap positions	-1	1	Ml <u>12/</u>
Differential non-linearity	RDNL <u>13/</u>	DCP register set between 10h and 7Fh; monotonic over all tap positions	-1	1	
Offset	Roffset <u>14/</u>	W option	0	5	
DCP to DCP matching	R _{MATCH} <u>15/</u>	Any two DCPs at the same tap position with the same terminal voltages	-2	2	

See footnote at end of table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/08604
		REV B	PAGE 5

TABLE I. Electrical performance characteristics – Continued . 1/

Test	Symbol	Conditions <u>2/</u> unless otherwise specified	Limits		Unit
			Min	Max	
V _{CC} Supply current (volatile write/read)	I _{CC1}	f _{SCL} = 400 kHz; SDA = Open; (for I ² C, active, read and write states)		0.5	mA
V _{CC} Supply current (non-volatile write/read)	I _{CC2}	f _{SCL} = 400 kHz; SDA = Open; (for I ² C, active, read and write states)		3	
V _{CC} current (standby)	I _{sb}	V _{CC} = 5.5 V @ I ² C interface in standby state		7	μA
		V _{CC} = 3.6 V @ I ² C interface in standby state		5	
V _{CC} current (shutdown)	I _{sd}	V _{CC} = 5.5 V @ I ² C interface in standby state		5	
		V _{CC} = 3.6 V @ I ² C interface in standby state		4	
Leakage current at pins A0, A1, A2, $\overline{\text{SHDN}}$, SDA, and SCL	I _{LkgDig}	Voltage at pin from GND to V _{CC}	-1	1	
DCP wipe response time	t _{WRT} <u>3/</u>	SCL falling edge of last bit of DCP data byte to wiper new position	1.5 TYP		μs
DCP recall time from shutdown mode	t _{ShdnRec} <u>3/</u>	From rising edge of $\overline{\text{SHDN}}$ signal to wiper stored position and RH connection	1.5 TYP		
		SCL falling edge of last bit of ACR data byte to wiper stored position and RH connection	1.5 TYP		
Power on recall voltage	V _{por}	Minimum V _{CC} at which memory recall occurs	2.0	2.6	V
V _{CC} ramp rate	V _{CCRamp}		0.2		V/ms
Power up delay	t _D	V _{CC} above V _{por} , to DCP initial value register recall completed, and I ² C interface stand by state		3	ms

EEPROM specification

EEPROM endurance			1,000,000		Cycles
EEPROM retention		Temperature T ≤ 55°C	50		Years
EEPROM retention		Temperature T ≤ 90°C	15		
EEPROM retention		Temperature T ≤ 125°C	10		
Non-volatile write cycle time	t _{WC} <u>17/</u>			20	ms

Serial interface specs

A2, A1, A0, $\overline{\text{SHDN}}$, SDA, and SCL input buffer LOW voltage	V _{IL}		-0.3	0.3*V _{CC}	V
A2, A1, A0, $\overline{\text{SHDN}}$, SDA, and SCL input buffer HIGH voltage	V _{IH}		0.7*V _{CC}	V _{CC} +0.3	
SDA and SCL input buffer Hysteresis	Hysteresis		0.05*V _{CC}		

See footnote at end of table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/08604
		REV B	PAGE 6

TABLE I. Electrical performance characteristics – Continued . 1/

Test	Symbol	Conditions 2/ unless otherwise specified	Limits		Unit
			Min	Max	
Serial interface specs - Cotinued					
SDA output buffer LOW voltage, Sinking 4 mA	V _{OL}		0	0.4	V
A2, A1, A0, SHDN, SDA, and SCL pin capacitance	C _{pin} 3/		10 TYP		pF
SCL frequency	f _{SCL}			400	kHz
Pulse width suppression time at SDA and SCL inputs	t _{sp}	Any pulse narrower than the max spec is suppressed		50	ns
SCL falling edge to SDA output data valid	t _{AA}	SCL falling edge crossing 30% of V _{CC} , until SDA exits the 30% to 70% of V _{CC} window		900	
Time the bus must be free before the start of a new transmission	t _{BUF}	SDA crossing 70% of V _{CC} during a STOP condition, to SDA crossing 70% of V _{CC} during the following START condition	1300		
Clock LOW time	t _{LOW}	Measured at the 30% of V _{CC} crossing	1300		
Clock HIGH time	t _{HIGH}	Measured at the 70% of V _{CC} crossing	600		
START condition setup time	t _{SU:STA}	SCL rising edge to SDA falling edge; both crossing 70% of V _{CC}	600		
START condition hold time	t _{HD:STA}	From SDA falling edge crossing 30% of V _{CC} to SCL falling edge crossing 70% of V _{CC}	600		
Input data setup time	t _{SU:DAT}	From SDA exiting the 30% to 70% of V _{CC} window, to SCL rising edge crossing 30% of V _{CC}	100		
Input data hold time	t _{SU:DAT}	From SCL rising edge crossing 70% of V _{CC} to SDA entering the 30% to 70% of V _{CC} window	0		
STOP condition setup time	t _{SU:STO}	From SCL rising edge crossing 70% of V _{CC} , to SDA rising edge crossing 30% of V _{CC}	600		
STOP condition hold time for Read or Volatile only Write	t _{HD:STO}	From SDA rising edge to SCL falling edge; both crossing 70% of V _{CC}	1300		
Output data hold time	t _{DH}	From SCL falling edge crossing 30% of V _{CC} , until SDA enters the 30% to 70% of V _{CC} window	0		
SDA and SCL rise time	t _R	From 30% to 70% of V _{CC}	20 + 0.1*Cb	250	
SDA and SCL fall time	t _F	From 70% to 30% of V _{CC}	20 + 0.1*Cb	250	
Capacitive loading of SDA or SCL	C _b	Total on chip and off chip	10	400	pF
SDA and SCL bus pull up resistor off chip	R _{pu}	Maximum is determined by t _R and t _F For C _b = 400 pF, max is about 2 ~ 2.5 kΩ For C _b = 40 pF, max is about 15 ~ 20 kΩ	1		kΩ
A2, A1 and A0 setup time	t _{SU:A}	Before START condition	600		ns
A2, A1, and A0 hold time	t _{HD:A}	After STOP condition	600		

See footnote at end of table.

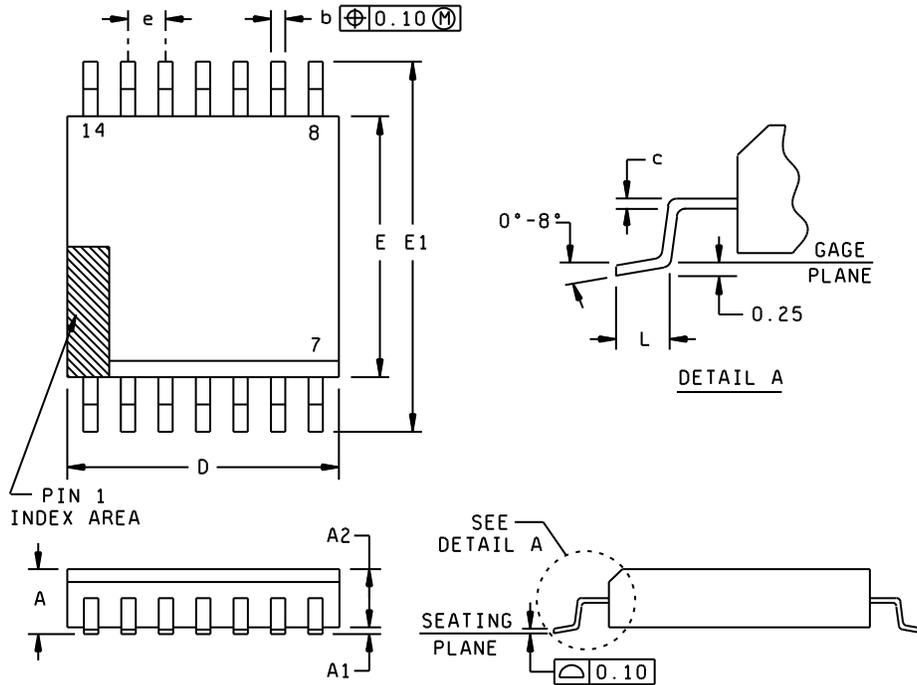
DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/08604
		REV B	PAGE 7

TABLE I. Electrical performance characteristics – Continued . 1/

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Over recommended operating conditions. All typical values are for $T_A = +25^\circ\text{C}$ and 3.3 V supply voltage.
- 3/ This parameter is not 100% tested.
- 4/ $\text{INL} = [V(\text{RW})_i - i * \text{LSB} - V(\text{RW})_0]/\text{LSB}$ for $i = 1$ to 127.
- 5/ $\text{LSB}:[V(\text{RW})_{127} - V(\text{RW})_0]/127$. $V(\text{RW})_{127}$ and $V(\text{RW})_0$ are $V(\text{RW})$ for the DCP register set to 7F hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
- 6/ $\text{DNL} = [V(\text{RW})_i - V(\text{RW})_{i-1}]/\text{LSB}-1$, for $i = 1$ to 127. i is the DCP register setting.
- 7/ $\text{ZS error} = V(\text{RW})_0/\text{LSB}$.
- 8/ $\text{FS error} = :[V(\text{RW})_{127} - V_{\text{CC}}]/\text{LSB}$.
- 9/ $V_{\text{MATCH}} = [V(\text{RW}_x)_i - V(\text{RW}_y)_j]/\text{LSB}$, for $i = 1$ to 127, $x = 0$ to 1 and $y = 0$ to 1.
- 10/ $\text{TC}_V = \frac{\text{Max}(V(\text{RW})_i) - \text{Min}(V(\text{RW})_j)}{[\text{Max}(V(\text{RW})_i) + \text{Min}(V(\text{RW})_j)]/2} \times \frac{10^6}{165^\circ\text{C}}$ for $i = 16$ to 112 decimal, $T = -55^\circ\text{C}$ to $+125^\circ\text{C}$. Max() is the maximum value of the wiper voltage and Min() is the minimum value of the wiper voltage over the temperature range
- 11/ $\text{RINL} = [\text{RW}_i - \text{M}(\text{MI} * i) - \text{RW}_0]/\text{MI}$ for $i = 16$ to 127.
- 12/ $\text{MI} = [\text{RW}_{127} - \text{RW}_0]/127$. MI is a minimum increment. RW_{127} and RW_0 are the measured resistances for the DCP register set to 7F hex and 00 hex respectively.
- 13/ $\text{RDNL} = [\text{RW}_i - \text{RW}_{i-1}]/\text{MI}-1$, for $i = 16$ to 127.
- 14/ $\text{Roffset} = \text{RW}_0/\text{MI}$, when measured between RW and RL.
 $\text{Roffset} = \text{RW}_{127}/\text{MI}$ when measured between RW and RH.
- 15/ $\text{RMATCH} = (\text{RW}_{i,x} - \text{RW}_{i,y})/\text{MI}$, for $i = 1$ to 127, $x = 0$ to 1 and $y = 0$ to 1.
- 16/ $\text{TC}_R = \frac{\text{Max}(\text{Ri}) - \text{Min}(\text{Ri})}{[\text{Max}(\text{Ri}) + \text{Min}(\text{Ri})]/2} \times \frac{10^6}{165^\circ\text{C}}$ for $i = 16$ to 112, $T = -55^\circ\text{C}$ to $+125^\circ\text{C}$. Max() is the maximum value of the resistance and Min() is the minimum value of the resistance over the temperature range
- 17/ t_{wc} is the time from a valid STOP condition at the end of a Write sequence I²C serial interface, to the end of the self timed internal non-volatile write cycle.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/08604</p>
		<p>REV B</p>	<p>PAGE 8</p>

Case X



Dimension					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	e	0.65 BSC	
A1	0.05	0.15	E	4.30	4.50
A2	0.80	1.05	E1	6.25	6.50
b	0.19	0.30	L	0.45	0.75
c	0.09	0.20	α	0°	8°
D	4.95	5.05			

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153 AC.
2. Body dimensions do not include mold flash, protrusion or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 0.15 mm per side.
3. "L" is the length of terminal for soldering to a substrate.
4. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07 mm.

FIGURE 1. Case outline.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/08604
		REV B	PAGE 9

Case X

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V _{CC}	8	SDA
2	SHDN	9	GND
3	RH0	10	RW1
4	RL0	11	RL1
5	RW0	12	RH1
6	A2	13	A0
7	SCL	14	A1

FIGURE 2. Terminal connections.

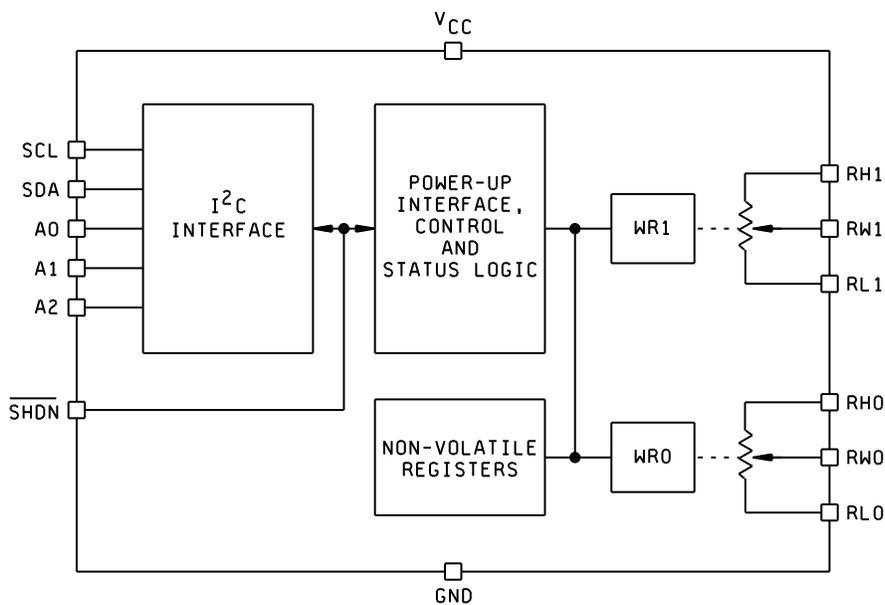
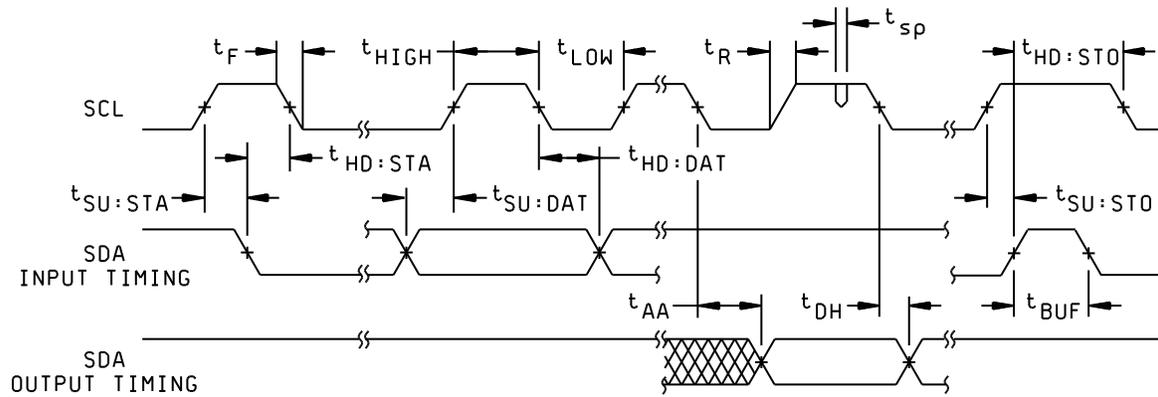
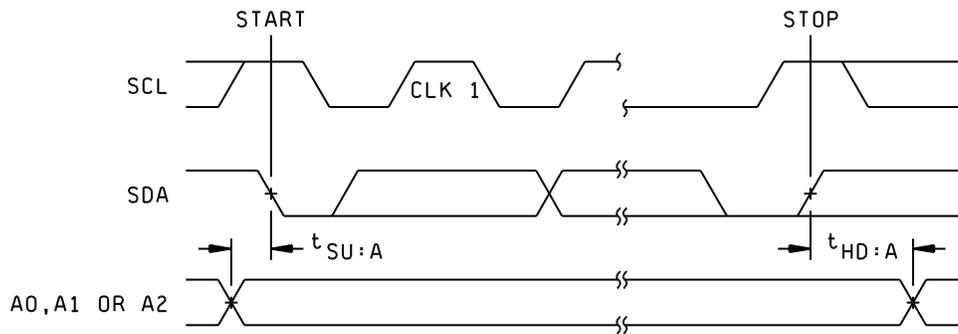


FIGURE 3. Block diagram.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/08604
		REV B	PAGE 10



SDA vs SCL TIMING



A0, A1, AND A2 PIN TIMING

FIGURE 4. Timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/08604
		REV B	PAGE 11

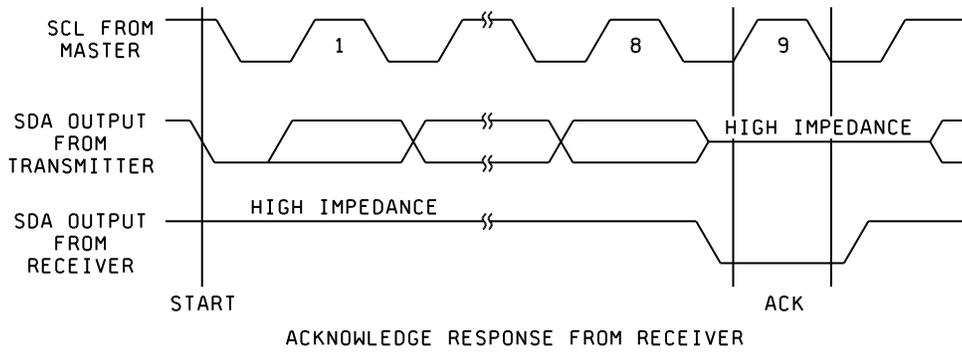
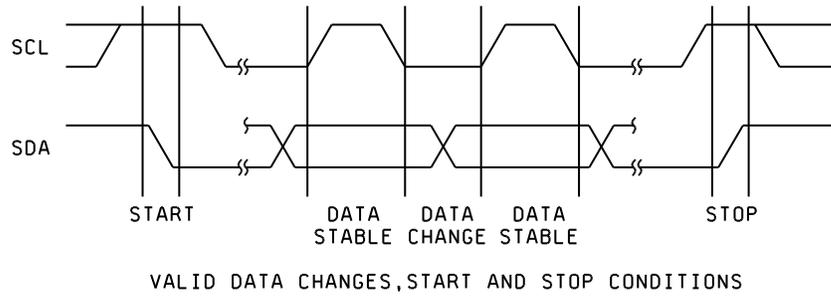


FIGURE 4. Timing waveforms - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/08604
		REV B	PAGE 12

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx>

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number	Top side Marking <u>2/</u>
V62/08604-01XE	34371	ISL22326WMVEP	22326WMVEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ Add -TK suffix to vendor part number for 1000 piece quantity with tape and reel packaging option.

CAGE code

34371

Source of supply

Intersil Corporation
 1001 Murphy Ranch Road
 Milpitas, CA 95035-5680
 Point of contact: 2401 Palm Bay Blvd.
 P.O. Box 883
 Melbourne, FL 32902-0883

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/08604
		REV B	PAGE 13