REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	16-11-28	Thomas M. Hess
B	Add Maximum Junction Temperature and Machine Model in section 1.3. Modify Power rating in section 1.4. Add minimum limit Power on Recall voltage; change input buffer to HIGH voltage in $V_{IH;}$ change test condition in t_{HIGH}; modify T_{MIN} test temperature in footnote 10 and 16; change RMATCH in footnote 15 in Table I. - PHN	16-12-05	Thomas M. Hess
C	Make correction to lead finish by deleting “E” and replacing with “B”. - ro	20-04-09	James R. Eschmeyer

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	**REV**			C	C	C	C	C	C	C	C	C	C	C	C	C						
	PAGE			1	2	3	4	5	6	7	8	9	10	11	12	13						

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 08-01-07	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, DIGITAL, CMOS, DUAL DIGITALLY CONTROLLED POTENTIOMETERS, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/08604**
	REV **C**	**PAGE** 1 **OF** 13

AMSC N/A

5962-V036-20

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance dual digitally controlled potentiometers microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/08604	-	01	X	B
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ISL22326	Dual digitally controlled potentiometers

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	14	MO-153	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.3 V to 6.0 V
Voltage at any digital interface pin with respect to GND	-0.3 V to V_{CC} + 0.3 V
Voltage at any DCP pin with respect to GND	-0.3 V to V_{CC}
Lead temperature (soldering, 10 seconds)	300°C
I_W (10 seconds)	±6 mA
Latch up	Class II, Level B at +125°C 2/
Storage temperature range (T_{STG})	-65°C to 150°C
Maximum junction temperature	+150°C
Electrostatic discharge (ESD) :	
Human body model (HBM)	2.5 kV
Charged device model (CDM)	1 kV
Machine model (MM)	350 V
Thermal resistance, junction to ambient (θ_{JA}) (case X)	100°C/W 3/

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	2.7 V to 5.5 V
Power rating of each DCP	15 mW
Wiper current of each DCP	±3.0 mA
Operating free-air temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

2/ JEDEC class II pulse conditions and failure criterion used. Level B exceptions are: using a max positive pulse of 6.5 V on the SHDN pin, and using a max negative pulse of -0.8 V for all pins.

3/ θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See manufacturer data for more information.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/ unless otherwise specified	Limits		Unit
			Min	Max	
R_H to R_L resistance	R_{TOTAL}	W option 3/	10 typical		kΩ
R_H to R_L resistance tolerance		W option	-20	+20	%
End to end temperature coefficient		W option 3/	±50 typical		ppm/°C 16/
Wiper resistance	RW	V_{CC} = 3.3 V, T_A = +25°C, wiper current = V_{CC}/R_{TOTAL}		200	Ω
VRH and VRL terminal voltage	V_{RH}, V_{RL}	V_{RH} and V_{RL} to GND	0	V_{CC}	V
Potentiometer capacitance	C_H/ C_L/ C_W 3/		10/ 10/ 25 typical		pF
Leakage on DCP pins	I_{LkgDCP}	Voltage at pin from GND to V_{CC}		1	µA
Voltage divider mode (0 V at R_{Li}; V_{CC} at R_{Hi}; measured at R_{Wi}, unloaded; I = 0 or 1)					
Integral non-linearity	INL 4/	Monotonic over all tap positions	-1	1	LSB 5/
Differential non linearity	DNL 6/	Monotonic over all tap positions	-1	1	LSB 5/
Zero scale error	ZSerror 7/	W option	0	5	LSB 5/
Full scale error	FSerror 8/	W option	-5	0	LSB 5/
DCP to DCP matching	V_{MATCH} 9/	Any two DCPs at same tap position, same voltage at all RH terminals, and same voltage at all RL terminals.	-2	2	LSB 5/
Ratiometric temperature coefficient	TC_V 3/ 10/	DCP register set to 40 hex	±4 typical		ppm/°C
Resistor mode (Measurements between R_{Wi} and R_{Li} with R_{Hi} not connected, or between R_{Wi} and R_{Hi} with R_{Li} not connected, i = 0 or 1)					
Integral non-linearity	RINL 11/	DCP register set between 10h and 7Fh; monotonic over all tap positions	-1	1	MI 12/
Differential non-linearity	RDNL 13/	DCP register set between 10h and 7Fh; monotonic over all tap positions	-1	1	MI 12/
Offset	Roffset 14/	W option	0	5	MI 12/
DCP to DCP matching	R_{MATCH} 15/	Any two DCPs at the same tap position with the same terminal voltages	-2	2	MI 12/

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued . 1/

Test	Symbol	Conditions 2/ unless otherwise specified	Limits		Unit
			Min	Max	
V_{CC} Supply current (volatile write/read)	I_{CC1}	f_{SCL} = 400 kHz; SDA = Open; (for I^2C, active, read and write states)		0.5	mA
V_{CC} Supply current (non-volatile write/read)	I_{CC2}	f_{SCL} = 400 kHz; SDA = Open; (for I^2C, active, read and write states)		3	mA
V_{CC} current (standby)	Isb	V_{CC} = 5.5 V at I^2C interface in standby state		7	µA
		V_{CC} = 3.6 V at I^2C interface in standby state		5	
V_{CC} current (shutdown)	Isd	V_{CC} = 5.5 V at I^2C interface in standby state		5	µA
		V_{CC} = 3.6 V at I^2C interface in standby state		4	
Leakage current at pins A0, A1, A2, $\overline{SHDN}$, SDA, and SCL	I_{LkgDig}	Voltage at pin from GND to V_{CC}	-1	1	µA
DCP wipe response time	t_{WRT} 3/	SCL falling edge of last bit of DCP data byte to wiper new position	1.5 typical		µs
DCP recall time from shutdown mode	$t_{ShdnRec}$ 3/	From rising edge of $\overline{SHDN}$ signal to wiper stored position and RH connection	1.5 typical		µs
		SCL falling edge of last bit of ACR data byte to wiper stored position and RH connection	1.5 typical		
Power on recall voltage	V_{por}	Minimum VCC at which memory recall occurs	2.0	2.6	V
V_{CC} ramp rate	VCCRamp		0.2		V/ms
Power up delay	t_D	V_{CC} above Vpor, to DCP initial value register recall completed, and I^2C interface stand by state		3	ms
EEPROM specification					
EEPROM endurance			1,000,000		Cycles
EEPROM retention		Temperature T ≤ 55°C	50		Years
EEPROM retention		Temperature T ≤ 90°C	15		Years
EEPROM retention		Temperature T ≤ 125°C	10		Years
Non-volatile write cycle time	t_{WC} 17/			20	ms
Serial interface specs					
A2, A1, A0, $\overline{SHDN}$, SDA, and SCL input buffer LOW voltage	V_{IL}		-0.3	0.3*V_{CC}	V
A2, A1, A0, $\overline{SHDN}$, SDA, and SCL input buffer HIGH voltage	V_{IH}		0.7*V_{CC}	V_{CC}+0.3	V
SDA and SCL input buffer Hysteresis	Hysteresis		0.05*V_{CC}		V
SDA output buffer LOW voltage, Sinking 4 mA	V_{OL}		0	0.4	V

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued . 1/

Test	Symbol	Conditions 2/ unless otherwise specified	Limits		Unit
			Min	Max	
Serial interface specs - Cotinued					
A2, A1, A0, $\overline{SHDN}$, SDA, and SCL pin capacitance	Cpin 3/		10 typical		pF
SCL frequency	f_{SCL}			400	kHz
Pulse width suppression time at SDA and SCL inputs	t_{sp}	Any pulse narrower than the max spec is suppressed		50	ns
SCL falling edge to SDA output data valid	t_{AA}	SCL falling edge crossing 30% of V_{CC}, until SDA exits the 30% to 70% of V_{CC} window		900	ns
Time the bus must be free before the start of a new transmission	t_{BUF}	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{CC} during the following START condition	1300		ns
Clock LOW time	t_{LOW}	Measured at the 30% of V_{CC} crossing	1300		ns
Clock HIGH time	t_{HIGH}	Measured at the 70% of V_{CC} crossing	600		ns
START condition setup time	$t_{SU:STA}$	SCL rising edge to SDA falling edge; both crossing 70% of V_{CC}	600		ns
START condition hold time	$t_{HD:STA}$	From SDA falling edge crossing 30% of V_{CC} to SCL falling edge crossing 70% of V_{CC}	600		ns
Input data setup time	$t_{SU:DAT}$	From SDA exiting the 30% to 70% of V_{CC} window, to SCL rising edge crossing 30% of V_{CC}	100		ns
Input data hold time	$t_{SU:DAT}$	From SCL rising edge crossing 70% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window	0		ns
STOP condition setup time	$t_{SU:STO}$	From SCL rising edge crossing 70% of V_{CC}, to SDA rising edge crossing 30% of V_{CC}	600		ns
STOP condition hold time for Read or Volatile only Write	$t_{HD:STO}$	From SDA rising edge to SCL falling edge; both crossing 70% of V_{CC}	1300		ns
Output data hold time	t_{DH}	From SCL falling edge crossing 30% of V_{CC}, until SDA enters the 30% to 70% of V_{CC} window	0		ns
SDA and SCL rise time	t_R	From 30% to 70% of V_{CC}	20 + 0.1*Cb	250	ns
SDA and SCL fall time	t_F	From 70% to 30% of V_{CC}	20 + 0.1*Cb	250	ns
Capacitive loading of SDA or SCL	Cb	Total on chip and off chip	10	400	pF
SDA and SCL bus pull up resistor off chip	R_{pu}	Maximum is determined by tR and tF For Cb = 400 pF, max is about 2 ~ 2.5 kΩ For Cb = 40 pF, max is about 15 ~ 20 kΩ	1		kΩ
A2, A1 and A0 setup time	$t_{SU:A}$	Before START condition	600		ns
A2, A1, and A0 hold time	$t_{HD:A}$	After STOP condition	600		ns

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued . 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Over recommended operating conditions. All typical values are for T_A = +25°C and 3.3 V supply voltage.

3/ This parameter is not 100% tested.

4/ INL = $[V(RW)_i – i * LSB – V(RW)_0]/LSB$ for i = 1 to 127.

5/ LSB:$[V(R_W)127 – V(R_W)0]/127$. $V(R_W)127$ and $V(R_W)_0$ are $V(R_W)$ for the DCP register set to 7F hex and 00 hes respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.

6/ DNL = $[V(R_W)_i – V(R_W)_{i-1}]/LSB-1$, for i = 1 to 127. i is the DCP register setting.

7/ ZS error = $V(R_W)0/LSB$.

8/ FS error = :$[V(R_W)127 – V_{CC}]/LSB$.

9/ $V_{MATCH} = [V(RWx)_i – V(RWy)_i]/LSB$, for i = 1 to 127, x = 0 to 1 and y = 0 to 1.

10/ $TC_V = \frac{Max(V(RW)_i) - Min(V(RW)_i)}{[Max(V(RW)_i] + Min(V(RW)_i] / 2} \times \frac{10^6}{165°C}$ for i = 16 to 112 decimal, T = -55°C to + 125°C. Max() is the maximum value of the wiper voltage and Min() is the minimum value of the wiper voltage over the temperature range

11/ RINL = $[RW_i – M(MI * i) – RW_0]/MI$ for I = 16 to 127.

12/ MI = $[RW_{127} – RW_0]/127$. MI is a minimum increment. RW_{127} and RW_0 are the measured resistances for the DCP register set to 7F hex and 00 hex respectively.

13/ RDNL = $[RW_i – RW_{i-1}]/MI-1$, for i = 16 to 127.

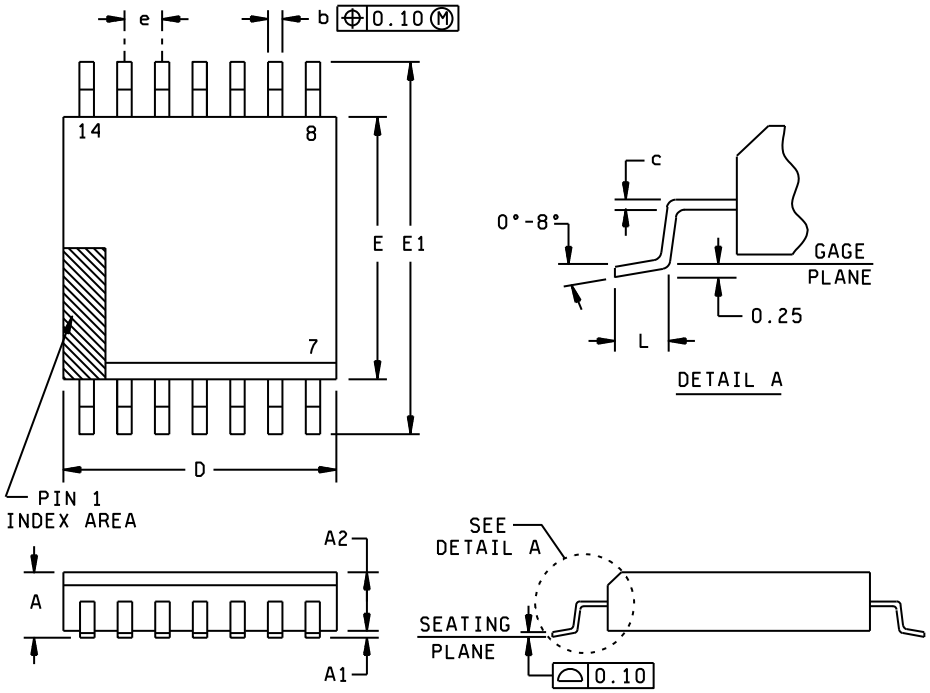
14/ Roffset = RW_0/MI, when measured between RW and RL.
Roffset = RW_{127}/MI when measured between RW and RH.

15/ RMATCH = $(RW_{i,x} – RW_{i,y})/MI$, for i = 1 to 127, x = 0 to 1 and y = 0 to 1.

16/ $TC_R = \frac{Max(Ri) - Min(Ri)}{[Max(Ri) + Min(Ri)] / 2} \times \frac{10^6}{165°C}$ for i = 16 to 112, T = -55°C to + 125°C. Max() is the maximum value of the resistance and Min() is the minimum value of the resistance over the temperature range

17/ t_{WC} is the time from a valid STOP condition at the end of a Write sequence I^2C serial interface, to the end of the self timed internal non-volatile write cycle.

Case X



Dimension					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	e	0.65 BSC	
A1	0.05	0.15	E	4.30	4.50
A2	0.80	1.05	E1	6.25	6.50
b	0.19	0.30	L	0.45	0.75
c	0.09	0.20	α	0°	8°
D	4.95	5.05			

NOTES:
1. These package dimensions are within allowable dimensions of JEDEC MO-153 AC.
2. Body dimensions do not include mold flash, protrusion or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 0.15 mm per side.
3. “L” is the length of terminal for soldering to a substrate.
4. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07 mm.

FIGURE 1. Case outline.

Case X

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V_{CC}	8	SDA
2	$\overline{SHDN}$	9	GND
3	RH0	10	RW1
4	RL0	11	RL1
5	RW0	12	RH1
6	A2	13	A0
7	SCL	14	A1

FIGURE 2. Terminal connections.

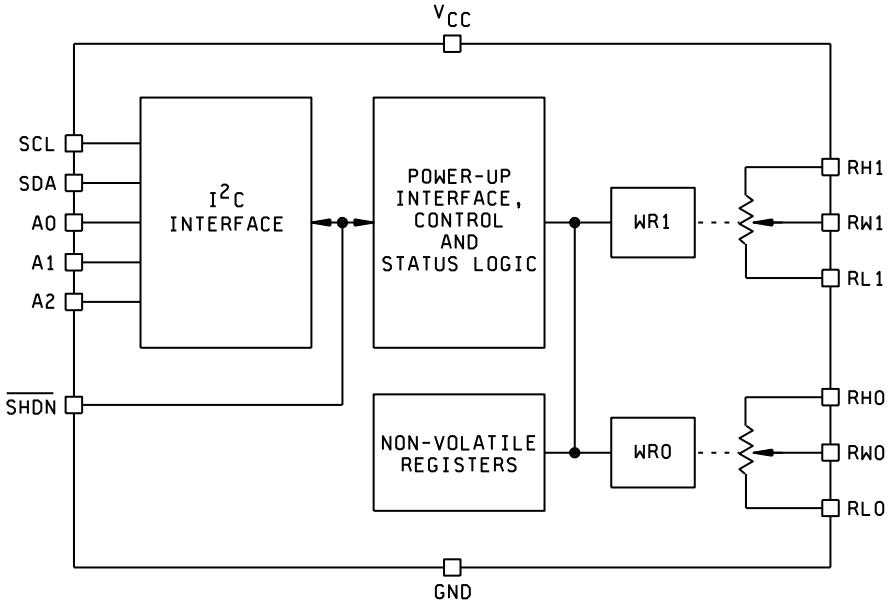
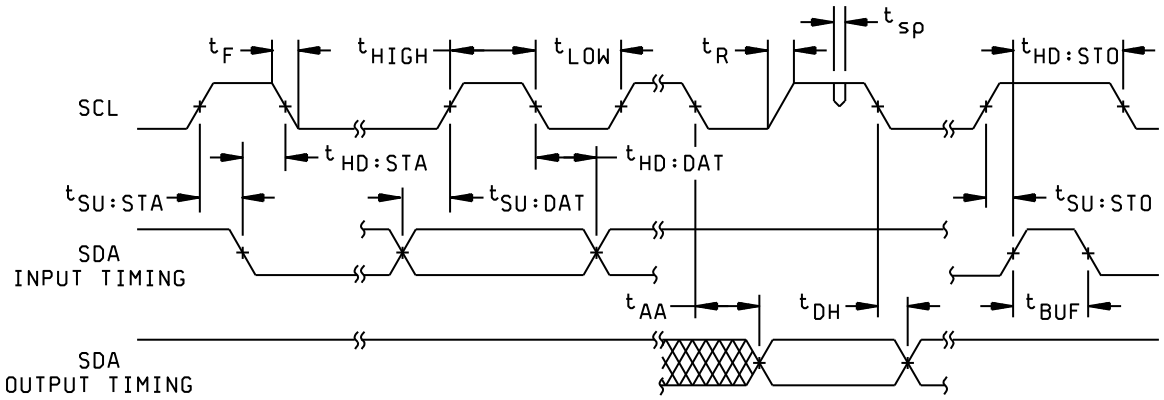
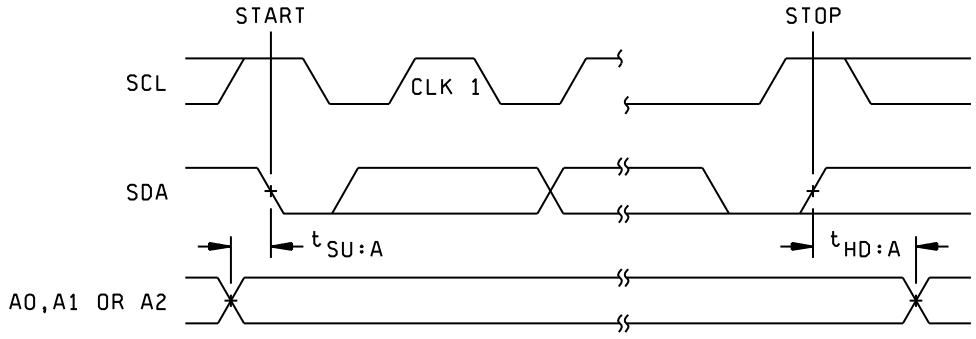


FIGURE 3. Block diagram.

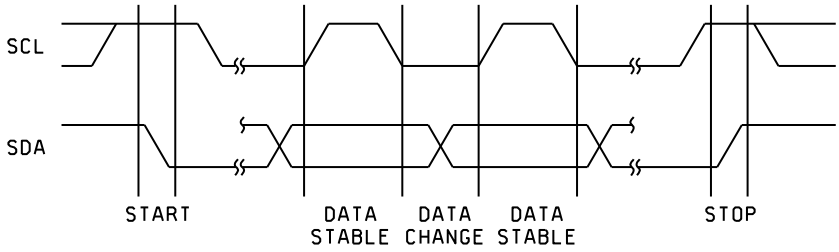


SDA vs SCL TIMING

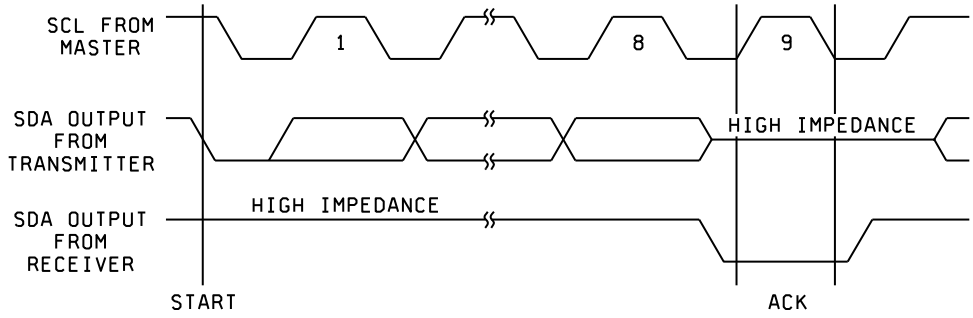


A0,A1, AND A2 PIN TIMING

FIGURE 4. Timing waveforms.



VALID DATA CHANGES,START AND STOP CONDITIONS



ACKNOWLEDGE RESPONSE FROM RECEIVER

FIGURE 4. Timing waveforms - Continued.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Top side marking 2/	Vendor part number
V62/08604-01XB	34371	22326WMVEP	ISL22326WMVEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Add –TK suffix to vendor part number for 1000 piece quantity with tape and reel packaging option.

CAGE code	Source of supply
34371	Renesas Electronics America 1650 Robert J. Conlan Blvd. NE Palm Bay, FL 32905-3406