

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Correct the θ_{JA} limit from 120°C/W to 162°C/W as specified under paragraph 1.3. Add a sentence to <u>SHDN</u> description as specified under Figure 1. - ro	09-10-06	C. SAFFLE
B	Make changes to R_{TOTAL} , INL, and R_{pu} tests under Table I. Update document paragraphs to current requirements. - ro	15-04-16	C. SAFFLE



CURRENT DESIGN ACTIVITY CAGE CODE 16236
 HAS CHANGED NAMES TO:
 DLA LAND AND MARITIME
 COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																				
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PMIC N/A	PREPARED BY RICK OFFICER	DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990
Original date of drawing YY-MM-DD 07-12-19	CHECKED BY RAJESH PITHADIA	TITLE MICROCIRCUIT, DIGITAL-LINEAR, SINGLE DIGITAL CONTROLLED POTENTIOMETER, MONOLITHIC SILICON
	APPROVED BY ROBERT M. HEBER	
	SIZE A	CODE IDENT. NO. 16236
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance single digital controlled potentiometer microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/08603</u>	-	<u>01</u>	<u>X</u>	<u>E</u>
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	ISL22316	Single digital controlled potentiometer (DCP)

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	10	MO-187BA	Plastic surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.3 V to +6 V
Voltage at any digital interface pin with respect to GND	-0.3 V to $V_{CC} + 0.3$ V
Voltage at any digital controlled potentiometer (DCP) pin with respect to GND	-0.3 V to V_{CC}
Wiper current (I_W) (10 seconds)	± 6 mA
Latchup	Class II, level B at +125°C 2/
Electrostatic discharge (ESD):	
Human body model	5 kV
Charge device model	1 kV
Maximum junction temperature (T_J)	+150°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-ambient (θ_{JA})	162°C/W 3/

1.4 Recommended operating conditions. 4/

Supply voltage range (V_{CC})	2.7 V to 5.5 V
Power rating of each DCP	5 mW
Wiper current of each DCP	± 3.0 mA
Operating free-air temperature range (T_A)	-55°C to +125°C

-
- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ JEDEC class II pulse conditions and failure criterion used. Level B exceptions are: using a maximum positive pulse of 6.5 V on the shutdown (SHDN) pin, and using a maximum negative pulse of -1 V for all pins.
- 3/ θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See manufacturer’s technical brief TB379 for details.
- 4/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figure 4.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions $V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
High terminal (RH) to low terminal (RL) resistance	R_{TOTAL}	W option, $V_{CC} = 3.3 \text{ V}$	+25°C	01	10 typical		k Ω
R_H to R_L resistance tolerance	R_{TOTAL}		-55°C to +125°C	01	-20	+20	%
End to end temperature coefficient	R_{TOTAL}	W option, $V_{CC} = 3.3 \text{ V}$ 2/	+25°C	01	±50 typical		ppm/°C
Wiper resistance	R_W	$V_{CC} = 3.3 \text{ V}$ at 25°C, wiper control = V_{CC} / R_{TOTAL}	-55°C to +125°C	01		200	Ω
V_{RH} and V_{RL} terminal voltages	V_{RH} , V_{RL}	V_{RH} and V_{RL} to GND	-55°C to +125°C	01	0	V_{CC}	V
Potentiometer capacitance	C_H 2/	High terminal, $V_{CC} = 3.3 \text{ V}$	+25°C	01	10 typical		pF
	C_L 2/	Low terminal, $V_{CC} = 3.3 \text{ V}$			10 typical		
	C_W 2/	Wiper terminal, $V_{CC} = 3.3 \text{ V}$			25 typical		
Leakage on DCP pins	I_{LkgDCP}	Voltage at pin from GND to V_{CC}	-55°C to +125°C	01		1	μA
Voltage divider mode section 0 V at R_L ; V_{CC} at R_H ; measured at R_W , unloaded							
Integral non linearity	INL 3/	Monotonic over all tap positions	-55°C to +125°C	01	-1	1	LSB 4/
Differential non linearity	DNL 5/	Monotonic over all tap positions	-55°C to +125°C	01	-1	+1	LSB 4/
Zero scale error	Z_{Serror} 6/	W option	-55°C to +125°C	01	0	5	LSB 4/
Full scale error	F_{Serror} 7/	W option	-55°C to +125°C	01	-5	0	LSB 4/
Ratiometric temperature coefficient	TC_V 2/, 8/	DCP register set to 40 hex for W option, $V_{CC} = 3.3 \text{ V}$	+25°C	01	±4 typical		ppm/°C

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V _{CC} = 2.7 V to 5.5 V, unless otherwise specified	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Resistor mode section							
Measurements between R _W and R _L with R _H not connected, or between R _W and R _H with R _L not connected.							
Integral non-linearity	R _{INL} 9/	DCP register set between 10 hex and 70 hex; monotonic over all tap positions; W option	-55°C to +125°C	01	-1	+1	MI 10/
Differential non-linearity	RDNL 11/	W option	-55°C to +125°C	01	-1	+1	MI 10/
Offset	R _{offset} 12/	W option	-55°C to +125°C	01	0	5	MI 10/
Operating specifications section							
V _{CC} supply current (volatile write / read)	I _{CC1}	f _{SCL} = 400 kHz; SDA = open; (for inter-integrated circuit (I ² C), active, read and write states)	-55°C to +125°C	01		0.5	mA
V _{CC} supply current (non-volatile write / read)	I _{CC2}	f _{SCL} = 400 kHz; SDA = open; (for I ² C, active, read and write states)	-55°C to +125°C	01		3	mA
V _{CC} current (standby)	I _{SB}	V _{CC} = +5.5 V, I ² C interface in standby state	-55°C to +125°C	01		7	μA
		V _{CC} = +3.6 V, I ² C interface in standby state				5	
V _{CC} current (shutdown)	I _{SD}	V _{CC} = +5.5 V, I ² C interface in standby state	-55°C to +125°C	01		5	μA
		V _{CC} = +3.6 V, I ² C interface in standby state				4	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Operating specifications section - continued.							
Leakage current, at pins A0, A1, $\overline{\text{SHDN}}$, SDA, and SCL	I_{LkgDig}	Voltage at pin from GND to V_{CC} , SDA is inactive	-55°C to +125°C	01	-1	1	μA
DCP wiper response time	$t_{DCP}^{2/}$	SCL falling edge of last bit of DCP data byte to wiper new position, $V_{CC} = 3.3\text{ V}$	+25°C	01	1.5 typical		μs
DCP recall time from shutdown mode	$t_{shdnrec}$	From rising edge of $\overline{\text{SHDN}}$ signal to wiper stored position and RH connection, $V_{CC} = 3.3\text{ V}$	+25°C	01	1.5 typical		μs
		SCL falling edge of last bit of ACR data byte to wiper stored position and RH connection, $V_{CC} = 3.3\text{ V}$			1.5 typical		
Power on recall voltage	V_{por}	Minimum V_{CC} at which memory recall occurs	-55°C to +125°C	01		2.6	V
V_{CC} ramp rate	V_{CCRamp}		-55°C to +125°C	01	0.2		V/ms
Power up delay	t_D	V_{CC} above V_{por} , to DCP initial value register recall completed, and inter-integrated circuit (I ² C) interface in standby state	-55°C to +125°C	01		3	ms
EEPROM specification section							
EEPROM endurance			-55°C to +125°C	01	1,000,000		Cycles
EEPROM retention			$\leq +55^\circ\text{C}$	01	50		Years
			$\leq +90^\circ\text{C}$		15		
			$\leq +125^\circ\text{C}$		10		
Non-volatile write cycle time	$t_{WC}^{13/}$		-55°C to +125°C	01		20	ms

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions $V_{CC} = 2.7\text{ V to }5.5\text{ V}$, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Serial interface specification section							
A1, A0, $\overline{\text{SHDN}}$, SDA, and SCL input buffer low voltage	V_{IL}		-55°C to +125°C	01	-0.3	$0.3 * V_{CC}$	V
A1, A0, $\overline{\text{SHDN}}$, SDA, and SCL input buffer high voltage	V_{IH}		-55°C to +125°C	01	$0.7 * V_{CC}$	$0.3 + V_{CC}$	V
SDA and SCL input buffer hysteresis	Hysteresis		-55°C to +125°C	01	$0.05 * V_{CC}$		V
SDA output buffer low voltage, sinking 4 mA	V_{OL}		-55°C to +125°C	01	0	0.4	V
A1, A0, $\overline{\text{SHDN}}$, SDA, and SCL pin capacitance	$C_{pin} \text{ } \underline{2/}$	$V_{CC} = 3.3\text{ V}$	+25°C	01	10 typical		pF
SCL frequency	f_{SCL}		-55°C to +125°C	01		400	kHz
Pulse width suppression time at SDA and SCL inputs	t_{sp}	Any pulse narrower than the maximum specification is suppressed	-55°C to +125°C	01		50	ns
SCL falling edge to SDA output data valid	t_{AA}	SCL falling edge crossing 30% of V_{CC} , until SDA exits the 30% to 70% of V_{CC} window	-55°C to +125°C	01		900	ns
Time the bus must be free before the start of a new transmission	t_{BUF}	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{CC} during the following START condition	-55°C to +125°C	01	1300		ns
Clock low time	t_{LOW}	Measured at the 30% of V_{CC} crossing	-55°C to +125°C	01	1300		ns
Clock high time	t_{HIGH}	Measured at the 70% of V_{CC} crossing	-55°C to +125°C	01	600		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V _{CC} = 2.7 V to 5.5 V, unless otherwise specified	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Serial interface specification section - continued.							
START condition setup time	t _{SU:STA}	SCL rising edge to SDA falling edge; both crossing 70% of V _{CC}	-55°C to +125°C	01	600		ns
START condition hold time	t _{HD:STA}	From SDA falling edge crossing 30% of V _{CC} to SCL falling edge crossing 70% of V _{CC}	-55°C to +125°C	01	600		ns
Input data setup time	t _{SU:DAT}	From SDA exiting the 30% to 70% of V _{CC} window, to SCL rising edge crossing 30% of V _{CC}	-55°C to +125°C	01	100		ns
Input data hold time	t _{HD:DAT}	From SCL rising edge crossing 70% of V _{CC} to SDA entering the 30% to 70% of V _{CC} window	-55°C to +125°C	01	0		ns
STOP condition setup time	t _{SU:STO}	From SCL rising edge crossing 70% of V _{CC} , to SDA rising edge crossing 30% of V _{CC}	-55°C to +125°C	01	600		ns
STOP condition hold time for read, or volatile only write	t _{HD:STO}	From SDA rising edge to SCL falling edge; both crossing 70% of V _{CC}	-55°C to +125°C	01	1300		ns
Output data hold time	t _{DH}	From SCL falling edge crossing 30% of V _{CC} , until SDA enters the 30% to 70% of V _{CC} window	-55°C to +125°C	01	0		ns
SDA to SCL rise time	t _R	From 30% to 70% of V _{CC}	-55°C to +125°C	01	20 + 0.1 * Cb	250	ns
SDA to SCL fall time	t _F	From 70% to 30% of V _{CC}	-55°C to +125°C	01	20 + 0.1 * Cb	250	ns
Capacitive loading of SDA or SCL	C _b	Total on chip and off chip	-55°C to +125°C	01	10	400	pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V _{CC} = 2.7 V to 5.5 V, unless otherwise specified	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Serial interface specification section - continued.							
SDA and SCL bus pull up resistor off chip	R _{pu}	Maximum is determine by t _R and t _F , For C _b = 400 pF, max is about 2 kΩ ~ 2.5 kΩ, For C _b = 40 pF, max is about 15 kΩ ~ 20 kΩ	-55°C to +125°C	01	1		kΩ
A1 and A0 setup time	t _{SU:A}	Before START condition	-55°C to +125°C	01	600		ns
A1 and A0 hold time	t _{HD:A}	After STOP condition	-55°C to +125°C	01	600		ns

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ This parameter is not 100 percent tested.
- 3/ $INL = [V(RW)_i - (i \cdot LSB) - V(RW)_0] / LSB$ for $i = 127$.
- 4/ $LSB = [V(RW)_{127} - V(RW)_0] / 127$. $V(RW)_{127}$ and $V(RW)_0$ are $V(RW)$ for the DCP register set to 7F hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
- 5/ $DNL = [V(RW)_i - V(RW)_{i-1}] / LSB - 1$, for $i = 1$ to 127, i is the DCP register setting.
- 6/ ZS error = $V(RW)_0 / LSB$.
- 7/ FS error = $[V(RW)_{127} - V_{CC}] / LSB$.
- 8/ $TC_V = \text{Max}(V(RW)_i) - \text{Min}(V(RW)_i) / [\text{Max}(V(RW)_i) + \text{Min}(V(RW)_i)] / 2 \times (10^6 / 165^\circ\text{C})$ for $i = 16$ to 127 decimal, $T = -55^\circ\text{C}$ to $+125^\circ\text{C}$. $\text{Max} ()$ is the maximum value of the wiper voltage and $\text{Min} ()$ is the minimum value of the wiper voltage over temperature range.
- 9/ $RINL = [RW_i - (MI \cdot i) - RW_0] / MI$, for $i = 16$ to 127.
- 10/ $MI = | RW_{127} - RW_0 | / 127$. MI is a minimum increment. RW_{127} and RW_0 are the measured resistances for the DCP register set to 7F hex and 00 hex respectively.
- 11/ $RDNL = (RW_i - RW_{i-1}) / MI - 1$, for $i = 16$ to 127.
- 12/ $R_{\text{offset}} = RW_0 / MI$, when measuring between RW and RL.
 $R_{\text{offset}} = RW_{127} / MI$, when measuring between RW and RH.
- 13/ t_{WC} is the time from a valid STOP condition at the end of a write sequence of inter-integrated circuit (I²C) serial interface, to the end of the self timed internal non-volatile write cycle.

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Case X

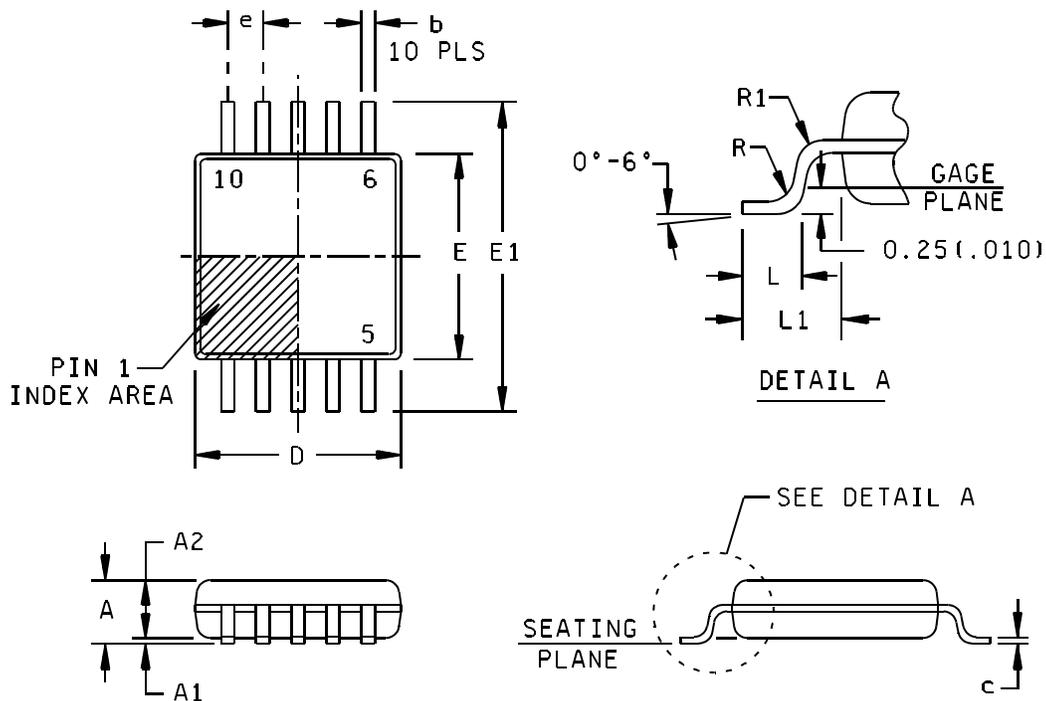


FIGURE 1. Case outline.

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Case X - continued

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
A	0.037	0.043	0.94	1.10	
A1	0.002	0.006	0.05	0.15	
A2	0.030	0.037	0.75	0.95	
b	0.007	0.011	0.18	0.27	8
c	0.004	0.008	0.09	0.20	
D	0.116	0.120	2.95	3.05	3
E	0.116	0.120	2.95	3.05	4
E1	0.187	0.199	4.75	5.05	
e	0.020 BSC		0.50 BSC		
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		
R	0.003	---	0.07	---	
R1	0.003	---	0.07	---	
n	10				7

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Dimensioning and tolerances per ANSI Y14.5M-1994.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15 mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions and are measured at datum plane. Interlead flash and protrusions shall not exceed 0.15 mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10 mm (0.004 inch) at seating plane.
6. "L" is the length of terminal for soldering to a substrate.
7. "n" is the number of terminal positions.
8. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07 mm (0.0027 inch).
9. Falls within JEDEC MO-187-BA.

FIGURE 1. Case outline - Continued.

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Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	SCL	Open drain inter-integrated circuit (I ² C) interface clock input.
2	SDA	Open drain serial data I/O for the inter-integrated circuit (I ² C) interface.
3	A1	Device address input for the inter-integrated circuit (I ² C) interface.
4	A0	Device address input for the inter-integrated circuit (I ² C) interface.
5	$\overline{\text{SHDN}}$	Shutdown active low input. This pin is logically ANDed with the SHDN bit in the access control register (ACR).
6	GND	Device ground pin.
7	R _L	"Low" terminal of digitally controlled potentiometer (DCP).
8	R _W	"Wiper" terminal of digitally controlled potentiometer (DCP).
9	R _H	"High" terminal digitally controlled potentiometer (DCP).
10	V _{CC}	Power supply pin.

FIGURE 2. Terminal connections.

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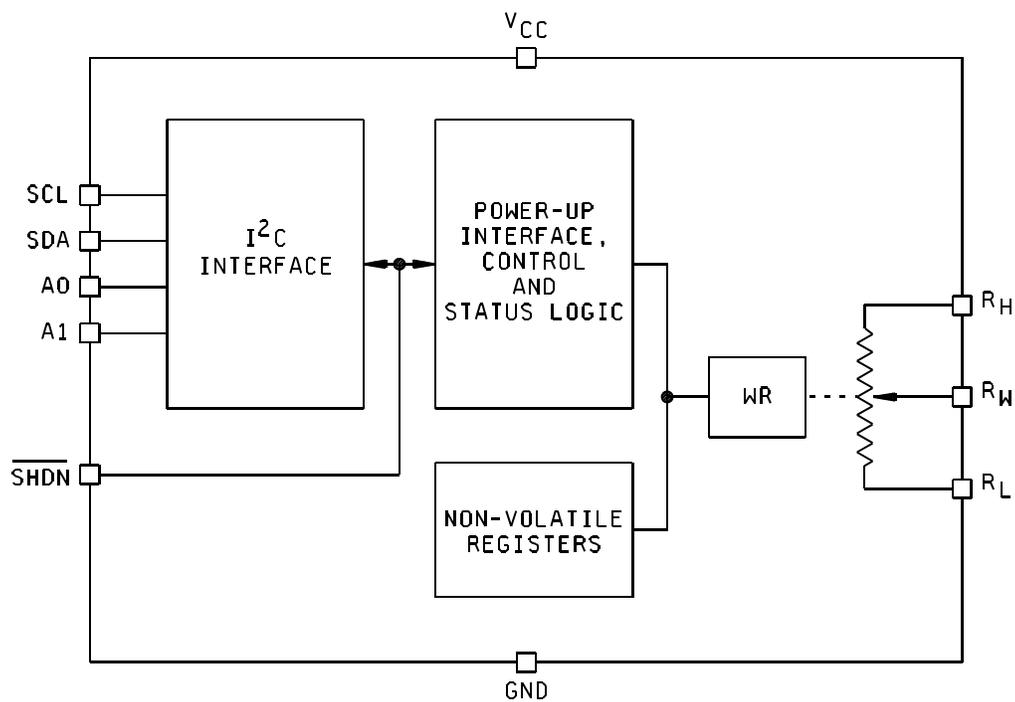


FIGURE 3. Block diagram.

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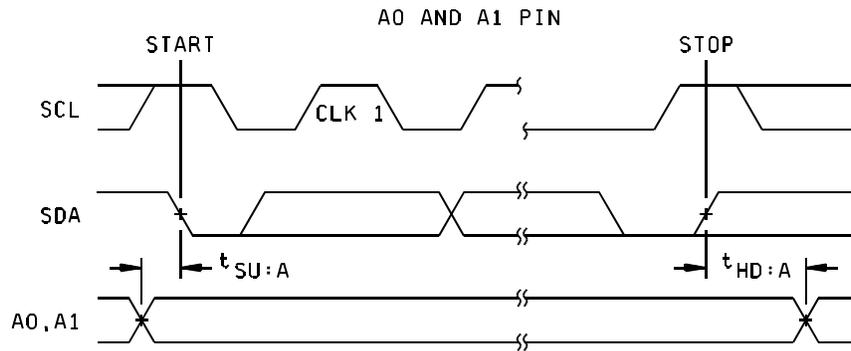
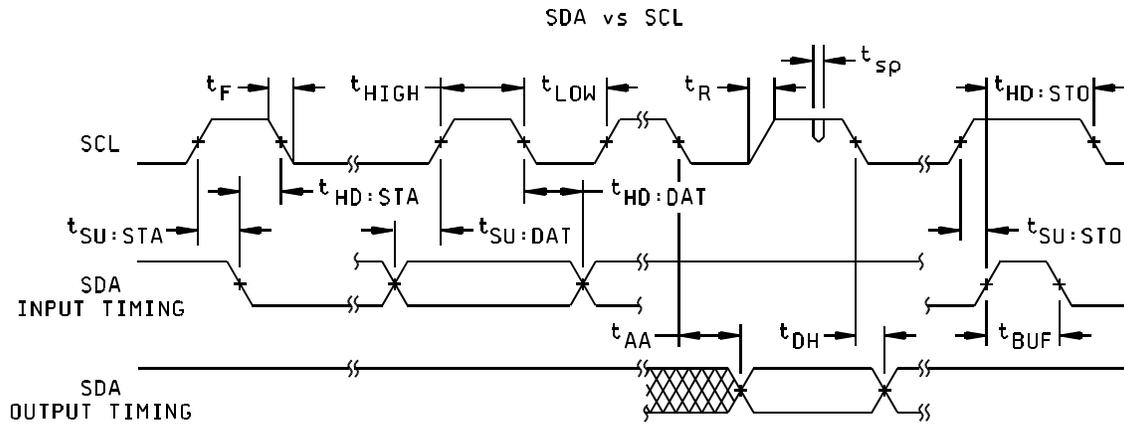


FIGURE 4. Timing waveforms.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Part marking	Vendor part number
V62/08603-01XB	34371	2316M	ISL22316WMUEP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ Add -TK suffix to vendor part number for 1000 piece quantity with tape and reel packaging option.

CAGE code

34371

Source of supply

Intersil Corporation
 1001 Murphy Ranch Road
 Milpitas, CA 95035-6803

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