REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	11-June-2015	Thomas M. Hess

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**
Original date of drawing YY MM DD 08-04-22	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL, FIXED POINT DIGITAL SIGNAL PROCESSOR, MONOLITHIC SILICON
	SIZE A / **CODE IDENT. NO.** 16236	**DWG NO.** **V62/07649**
	REV A	**PAGE** 1 **OF** 60

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance Fixed-Point Digital Signal Processor microcircuit, with an operating temperature range of 0°C to +90°C (devices type 01, 04, 05 and 06), an extended operating temperature range of -55°C to +105°C (device type 02) and an extended operating temperature range of -40°C to +105°C (device type 03).

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/07649	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s). 1/

Device type	Generic	Clock Rate	Temperature Range	Circuit function
01	SM320C6455-EP	1 GHz	0°C to +90°C	Fixed point digital signal Processor
02	SM320C6455-EP	1 GHz	-55°C to +105°C	Fixed point digital signal Processor
03	SM320C6455-EP	1 GHz	-40°C to +105°C	Fixed point digital signal Processor
04	SM320C6455-EP	720 MHz	0°C to +90°C	Fixed point digital signal Processor
05	SM320C6455-EP	850 MHz	0°C to +90°C	Fixed point digital signal Processor
06	SM320C6455-EP	1.2 GHz	0°C to +90°C	Fixed point digital signal Processor

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	Package style
X	697	Plastic ball grid array

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1/ Users are cautioned to review the manufacturers data manual for additional user information relating to this device.

1.3 Absolute maximum ratings. 2/

Supply voltage ranges:
- (CV_{DD}) ..... -0.5 V to +1.5 V 3/
- (DV_{DD33}) ..... -0.5 V to +4.2 V 3/
- (DV_{DDR}, DV_{DD18}, AV_{DLL1}, AV_{DLL2}) ..... -0.5 V to +2.5 V 3/
- (DV_{DD15}) ..... -0.5 V to +2.5 V 3/
- (DV_{DD12}, DV_{DDRM}, AV_{DDT}, AV_{DDA}) ..... -0.5 V to +1.5 V 3/
- (PLLV1, PLLV2) ..... -0.5 V to +2.5 V 3/

Input voltage ranges: (V_I):
- 3.3 V pins (except PCI capable pins) ..... -0.5 V to DV_{DD33} + 0.5 V
- PCI capable pins ..... -0.5 V to DV_{DD33} + 0.5 V
- RGMII pins ..... -0.5 V to +2.5 V
- DDR2 memory controller pins ..... -0.5 V to +2.5 V

Output voltage ranges:
- 3.3 V pins (except PCI capable pins) ..... -0.5 V to DV_{DD33} + 0.5 V
- PCI capable pins ..... -0.5 V to DV_{DD33} + 0.5 V
- RGMII pins ..... -0.5 V to +2.5 V
- DDR2 memory controller pins ..... -0.5 V to +2.5 V

Operating case temperature ranges, (T_C):
- Device type 01, 04, 05 and 06 ..... 0°C to +90°C
- Device type 02 ..... -55°C to +105°C
- Device type 03 ..... -40°C to +105°C

Storage temperature range, (T_{STG}) ..... -65°C to +150°C

1.4 Recommended operating conditions.

Supply voltage, core (CV_{DD}):
- device type 01, 02, and 03 ..... +1.2125 V to +1.2875 V
- device type 04, 05, and 06 ..... +1.1640 V to +1.2360 V

Supply voltage, core (DV_{DDRM})[required only for rapid IO]:
- device type 01, 02, and 03 ..... +1.2125 V to +1.2875 V
- device type 04, 05, and 06 ..... +1.1640 V to +1.2360 V

Supply voltage, core (DV_{DD12}, AV_{DDA}, AV_{DDT})[required only for rapid IO]:
- device type 01, 02, and 03 ..... +1.1875 V to +1.3125 V
- device type 04, 05 and 06 ..... +1.14 V to +1.26 V

Supply voltage, I/O (DV_{DD33}) ..... +3.14 V to +3.46 V
Supply voltage, I/O (DV_{DD18}) ..... +1.71 V to +1.89 V
Supply voltage, I/O (AV_{DLL1}) ..... +1.71 V to +1.89 V
Supply voltage, I/O (AV_{DLL2}) ..... +1.71 V to +1.89 V
Reference voltage ($V_{REFSSTL}$) ..... 0.49DV_{DD18} V to 0.51DV_{DD18} V
Supply voltage, I/O (DV_{DD15}):
- 1.8 V operation ..... +1.71 V to +1.89 V
- 1.5 V operation ..... +1.43 V to +1.57 V

Reference voltage, ($V_{REFHSTL}$):
- 1.8 V operation ..... +0.855 V to +0.945 V
- 1.5 V operation ..... +0.713 V to +0.787 V

Supply voltage, PLL (PLLV1, PLLV2) ..... +1.71 V to +1.89 V
Supply ground, (V_{SS}) ..... 0 V

2/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3/ All voltage values are with respect to V_{SS}.

1.4 Recommended operating conditions - Continued.

High level input voltage, (V_{IH}):
- 3.3 V pins (except PCI cable and I2C pins) ..... +2.0 V minimum
- PCI – cable pins ..... $0.5DV_{DD33}$ to DV_{DD33} + 0.5 V 4/
- I2C pins ..... $0.7DV_{DD33}$ V minimum
- RGMII pins ..... $V_{REFHSTL}$ + 0.10 to DV_{DD15} + 0.30 V
- DDR2 memory controller pins (DC) ..... $V_{REFSST}L$ + 0.125 to DV_{DD18} + 0.3 V

Low level input voltage, (V_{IL}) (except PCI) ..... +0.8 V
- 3.3 V pins (except PCI cable and I2C pins) ..... +0.8 V maximum
- PCI – cable pins ..... -0.5 V to $0.3DV_{DD33}$ V 4/
- I2C pins ..... $0.3DV_{DD33}$ V maximum
- RGMII pins ..... -0.3 V to $V_{REFHSTL}$ – 0.1 V
- DDR2 memory controller pins (DC) ..... -0.8 V to $V_{REFSSTL}$ – 0.125 V

Maximum voltage during overshoot/undershoot (V_{OS}) (PCI capable pins)..... -3.5 V to 7.1 V 5/

Operating case temperature (T_C):
- Device type 01, 04, 05 and 06: ..... 0°C to +90°C
- Device type 02 ..... -55°C to +105°C
- Device type 03 ..... -40°C to +105°C

Thermal resistance characteristics case X:

		°C/W	Air flow (m/s)
1	Junction to case, $R\Theta_{JC}$	1.45	N/A
2	Junction to board, $R\Theta_{JB}$	8.34	N/A
3	Junction to free air, $R\Theta_{JA}$	16.1	0.00
4		13.0	1.0
5		11.9	2.0
6		10.7	3.0
7	Junction to package top, Psi_{JT}	0.37	0.00
		0.89	1.0
		1.01	1.5
		1.17	3.0
8	Junction to board Psi_{JB}	7.6	0.0
		6.7	1.0
		6.4	1.5
		5.8	3.0

m/s = meter per second

4/ These rated numbers are from the PCI local bus specification. See data from manufacturer for more information.
5/ PCI capable pins can withstand a maximum overshoot/undershoot for up to 11 ns as required by the PCI local bus specification.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as specified in figure 3.

3.5.4 Test load circuit for AC timing measurement. The test load circuit for AC timing measurements shall be as specified in figure 4.

3.5.5 Timing waveforms. The timing waveforms shall be as shown in figures 5-57.

TABLE I. Electrical performance characteristics. 1/

Test		Symbol	Test condition 2/ Device type: All	Limits		Unit
				Min	Max	
High level output voltage	3.3 V pins (except PCI capable and I2C pins)	V_{OH}	DV_{DD33} = MIN, I_{OH} = MAX	$0.8DV_{DD33}$		V
	PCI capable pins 3/		IOH = -0.5 mA, DV_{DD33} = 3.3 V	$0.9DV_{DD33}$		
	RGMII pins			DV_{DD15} -0.4		
	DDR2 memory controller pins			1.4		
Low level output voltage	3.3 V pins (except PCI capable and I2C pins)	V_{OL}	DV_{DD33} = MIN, I_{OL} = MAX		$0.22DV_{DD33}$	V
	PCI capable pins 3/		IOH = -0.5 mA, DV_{DD33} = 3.3 V		$0.1DV_{DD33}$	
	I2C		Pulled up to 3.3 V, 3 mA sink current		0.4	
	RGMII pins				0.4	
	DDR2 memory controller pins				0.4	
Input current [DC]	3.3 V pins (except PCI capable and I2C pins)	I_I 4/	$V_I = V_{SS}$ to DV_{DD33}, pins without internal pullup or pulldown resistor	-1	1	µA
			$V_I = V_{SS}$ to DV_{DD33}, pins without internal pullup resistor	50	400	
			$V_I = V_{SS}$ to DV_{DD33}, pins without internal pulldown resistor	-400	-50	
	I2C pins		$0.1DV_{DD33} \le V_I \le 0.9DV_{DD33}$	-10	10	
	PCI capable pins 5/			-1000	1000	
	RGMII pins				0.4	V
High level output current [DC]	AECLKOUT, CLKR1/GP[0], CLKX1/GP[3], SYSCLK4/GP[1], EMU[18:0], CLKR0, CLKX0	I_{OH}			-8	mA
	EMIF pins (except AECLKOUT), NMI, TOUT0L, TINP0L, TOUT1L, TINP1L, PCI_EN, EMAC-capable pins (except RGMII pins), $\overline{\text{RESETSTAT}}$, McBSP-capable pins (except CLKR1/GP[0], CLKX1/GP[3], CLKR0, CLKX0) GP[7:4], and TDO				-4	
	PCI capable pins 3/				-0.5	
	RGMII pins				-8	
	DDR2 memory controller pins				4	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test		Symbol	Test condition 2/	Limits		Unit
				Min	Max	
Low level output current	AECLKOUT, CLKR1/GP[0], CLKX1/GP[3], SYSCLK4/GP[1], EMU[18:0], CLKR0, CLKX0	I_{OL}			8	mA
	EMIF pins (except AECLKOUT), NMI, TOUT0L, TINP0L, TOUT1L, TINP1L, PCI_EN, EMAC-capable pins (except RGMII pins), $\overline{\text{RESETSTAT}}$, McBSP-capable pins (except CLKR1/GP[0], CLKX1/GP[3], CLKR0, CLKX0) GP[7:4], and TDO				5	
	PCI capable pins 3/				1.5	
	RGMII pins				8	
	DDR2 memory controller pins				-4	
Off state output current [DC]	3.3 V pins	I_{OZ} 6/	$V_O = DV_{DD33}$ or 0 V	-20	20	µA
Core supply power 7/		P_{CDD}	CV_{DD} = 1.25 V, CPU frequency = 1200 MHz	1.79 TYP		W
			CV_{DD} = 1.25 V, CPU frequency = 1000 MHz	1.57 TYP		
			CV_{DD} = 1.2 V, CPU frequency = 850 MHz	1.30 TYP		
			CV_{DD} = 1.2 V, CPU frequency = 720 MHz	1.18 TYP		
I/O supply power 7/		P_{DDD}	DV_{DD33} = 3.3 V, $DV_{DD18} = DV_{DDR}$ = 1.8 V, PLLV1 = PLLV2 = $AV_{DLL1} = AV_{DLL2}$ = 1.8 V, CPU frequency = 1200 MHz	0.54 TYP		
			DV_{DD33} = 3.3 V, $DV_{DD18} = DV_{DDR}$ = 1.8 V, PLLV1 = PLLV2 = $AV_{DLL1} = AV_{DLL2}$ = 1.8 V, CPU frequency = 1000 MHz	0.54 TYP		
			DV_{DD33} = 3.3 V, $DV_{DD18} = DV_{DDR}$ = 1.8 V, PLLV1 = PLLV2 = $AV_{DLL1} = AV_{DLL2}$ = 1.8 V, CPU frequency = 850 MHz	0.53 TYP		
			DV_{DD33} = 3.3 V, $DV_{DD18} = DV_{DDR}$ = 1.8 V, PLLV1 = PLLV2 = $AV_{DLL1} = AV_{DLL2}$ = 1.8 V, CPU frequency = 720 MHz	0.52 TYP		
Input capacitance		C_I			10	pF
Output capacitance		C_O			10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test condition 2/ Device type: All	Limits		Unit
				Min	Max	
Timing requirements for power supply sequence						
1	Setup time, DV_{DD33} supply stable before CV_{DD12} supply stable	$t_{su(DVDD33-CVDD12)}$	See figure 5	0.5	200	ms
2	Setup time, DV_{DD33} supply stable before all other supplies stable	$t_{su(DVDD33-ALLSUP)}$		0	200	
Timing requirements for external interrupts 8/						
1	Width of the NMI interrupt pulse low	$t_{w(NMIL)}$	See figure 6	6P		ns
2	Width of the NMI interrupt pulse low	$t_{w(NMIH)}$		6P		
Timing requirements for Reset 9/ 10/ 11/						
5	Pulse duration, $\overline{POR}$ low	$t_{w(POR)}$	See figure 7and 8	256D 12/		ns
6	Pulse duration, $\overline{RESET}$ low	$t_{w(RESET)}$		24C		
7	Setup time, boot mode and configuration pins valid before $\overline{POR}$ high or $\overline{RESET}$ high 13/	$t_{su(boot)}$		6P		
8	Hold time, boot mode and configuration pins valid before $\overline{POR}$ high or $\overline{RESET}$ high 13/	$t_{h(boot)}$		6P		
Switching characteristics over recommended operating conditions during reset 9/						
9	Delay time, $\overline{POR}$ high and $\overline{RESET}$ high to $\overline{RESETSTAT}$ high		See figure 7		15000C	ns
PLL1 AND PLL1 CONTROLLER						
PLL1 clock frequency ranges						
	CLKIN1				66.6	MHz
	PLLREF (PLLEN = 1) 18/			33.3	66.6	
	PLLOUT			400	1200	
	SYSCLK4			25	166	
	SYSCLK5				333	
PLL1 stabilization, lock, and reset times 9/						
	PLL stabilization time			150		µs
	PLL lock time				2000C	ns
	PLL reset time			128C		ns
Timing requirements for CLKIN1 devices 17/						
1	Cycles time, CLKIN1 16/	$t_{c(CLKIN1)}$	See figure 9	15	30.3	ns
2	Pulse duration, CLKIN1 high	$t_{w(CLKIN1H)}$		0.4C		
3	Pulse duration, CLKIN1 low	$t_{w(CLKIN1L)}$		0.4C		
4	Transition time, CLKIN1	$t_{t(CLKIN1)}$			1.2	
5	Period jitter (peak to peak), CLKIN1	$t_{J(CLKIN1)}$			100	ps

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test condition 2/ Device type: All	Limits		Unit
				Min	Max	
	PLL1 AND PLL1 CONTROLLER - Continued					
	Switching characteristics over recommended operating conditions for SYSCLK4 [CPU/8 – CPU/12]					
2	Pulse duration, SYSCLK4 high	$t_{w(CKO3H)}$	See figure 10	4P-0.7	6P+0.7	ns
3	Pulse duration, SYSCLK4 low	$t_{w(CKO3L)}$		4P-0.7	6P+0.7	
4	Transition time, SYSCLK4	$t_{t(CKO3)}$			1	
	PLL2 AND PLL2 CONTROLLER					
	PLL2 clock frequency ranges					
	PLLREF (PLLEN = 1)			12.5	26.7	MHz
	PLLOUT			250	533	
	SYSCLK1 19/			50	125	
	Timing requirements for CLKIN2 14/ 20/ 21/					
1	Cycles time, CLKIN2	$t_{c(CLKIN2)}$	See figure 11	37.5	80	ns
2	Pulse duration, CLKIN2 high	$t_{w(CLKIN2H)}$		0.4C		
3	Pulse duration, CLKIN2 low	$t_{w(CLKIN2L)}$		0.4C		
4	Transition time, CLKIN2	$t_{t(CLKIN2)}$			1.2	
5	Period jitter (peak to peak), CLKIN2	$t_{J(CLKIN2)}$			100	ps
	EMIFA ELECTRICAL DATA/TIMING					
	Timing requirements for ECLKIN for EMIFA 14/ 22/					
1	Cycle time, AECLKIN	$t_{c(EKI)}$	See figure 12	6 23/	40	ns
2	Pulse duration, AECLKIN high	$t_{w(EHIH)}$		2.7		
3	Pulse duration, AECLKIN low	$t_{w(EKIL)}$		2.7		
4	Transaction, AECLKIN	$t_{t(EKI)}$			3	
5	Period jitter, AECLKIN	$t_{J(EKI)}$			0.02E 24/	
	Switching characteristics for AECLKOUT for EMIFA modules					
1	Cycle time, AECLKOUT	$t_{c(EKO)}$	See figure 13	E-0.7	E+0.7	ns
2	Pulse duration, AECLKOUT high	$t_{w(EKOH)}$		EH-0.7	EH+0.7	
3	Pulse duration, AECLKOUT low	$t_{w(EKOL)}$		EL-0.7	EL+0.7	
4	Transition time, AECLKOUT	$t_{t(EKO1)}$			1	
5	Delay time, AECLKIN high to AECLKOUT high	$t_{d(EKIH-EKOH)}$		1	8	
6	Delay time, AECLKIN low to AECLKOUT low	$t_{d(EKIL-EKOL)}$		1	8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test condition 2/ Device type: All	Limits Min	Limits Max	Unit
	EMIFA ELECTRICAL DATA/TIMING - Continued					
	Timing requirements for asynchronous memory cycles for EMIFA module 27/ 28/ 29/					
3	Setup time, AEDx valid before $\overline{AAOE}$ high	$t_{su(EDV-AOEH)}$	See figure 14 and 15	6.5		ns
4	Hold time, AEDx valid after $\overline{AAOE}$ high	$t_{h(AOEH-EDV)}$		0		
5	Setup time, AARDY valid before AECLKOUT low	$t_{su(ARDY-EKOH)}$		1		
6	Hold time, AARDY valid after AECLKOUT high	$t_{h(EKOH-ARDY)}$		2		
7	Pulse width, AARDY assertion and deassertion	$t_{w(ARDY)}$		2E+5		
8	Delay time, from AARDY sampled deasserted on AECLKOUT falling to beginning of programmed hold period	$t_{d(ARDY-HOLD)}$			4E	
9	Setup time, before end of programmed strobe period by which AARDY should be asserted in order to insert extended strobe wait states	$t_{su(ARDY-HOLD)}$		2E		
	Switching characteristics for asynchronous memory cycles for EMIFA module 27/ 30/ 31/					
1	Output setup time, select signals valid to $\overline{AAOE}$ low	$t_{osu(SELV-AROEL)}$	See figure 14 and 15	RS*E-1.5		ns
2	Output hold time, $\overline{AAOE}$ high to select signals invalid	$t_{oh(AOEH-SELIV)}$		RS*E-1.9		
10	Delay time, AECLKOUT high to $\overline{AAOE}$ valid	$t_{d(EKO1H-AOEV)}$		1	7	
11	Output setup time, select signals valid to $\overline{AAWE}$ low	$t_{osu(SELV-AWEL)}$		WS*E-1.7		
12	Output hold time, $\overline{AAWE}$ high to select signals invalid	$t_{oh(AWEH-SELIV)}$		WH*E-1.8		
13	Delay time, AECLKOUT high to $\overline{AAWE}$ valid	$t_{d(EKOH-AWEV)}$		1.3	7.1	
	Timing requirements for programmable synchronous interface cycles for EMIFA module					
6	Setup time, read AEDx valid before AECLKOUT high	$t_{su(EDV-EKOH)}$	See figure 16, 17, and 18	2		ns
7	Hold time, read AEDx valid after AECLKOUT high	$t_{h(EKOH-EDV)}$		1.5		
	Switching characteristics for programmable synchronous interface cycles for EMIFA module 32/					
1	Delay time, AECLKOUT high to $\overline{ACEx}$ valid	$t_{d(EKOH-CEV)}$	See figure 16, 17, and 18	1.3	4.9	ns
2	Delay time, AECLKOUT high to $\overline{ABEx}$ valid	$t_{d(EKOH-BEV)}$			4.9	
3	Delay time, AECLKOUT high to $\overline{ABEx}$ invalid	$t_{d(EKOH-BEIV)}$		1.3		
4	Delay time, AECLKOUT high to AEAx valid	$t_{d(EKOH-EAV)}$			4.9	
5	Delay time, AECLKOUT high to AEAx invalid	$t_{d(EKOH-EAIV)}$		1.3		
8	Delay time, AECLKOUT high to $\overline{ASADS}$ / $\overline{ASRE}$ valid	$t_{d(EKOH-ADSVV)}$		1.3	4.9	
9	Delay time, AECLKOUT high to $\overline{ASOE}$ valid	$t_{d(EKOH-OEV)}$		1.3	4.9	
10	Delay time, AECLKOUT high to AEDx valid	$t_{d(EKOH-EDV)}$			4.9	
11	Delay time, AECLKOUT high to AEDx invalid	$t_{d(EKOH-EDIVV)}$		1.3		
12	Delay time, AECLKOUT high to $\overline{ASWE}$ valid	$t_{d(EKOH-WEV)}$		1.3	4.9	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test condition 2/ Device type: All	Limits		Unit
				Min	Max	
	$\overline{HOLD}$ / $\overline{HOLDA}$ TIMING					
	Timing requirements for the $\overline{HOLD}$ / $\overline{HOLDA}$ cycles for EMIFA modules 33/					
3	Hold time, $\overline{HOLD}$ low after $\overline{HOLDA}$ low	$t_{h(HOLDAL-HOLDL)}$	See figure 7-39	E		ns
	Switching characteristics for the $\overline{HOLD}$ / $\overline{HOLDA}$ cycles for EMIFA modules 33/ 34/ 35/					
1	Delay time, $\overline{HOLD}$ low to EMIFA bus high impedance	$t_{d(HOLD-EMHZ)}$	See figure 19	2E	35/	ns
2	Delay time, EMIF bus high impedance to $\overline{HOLDA}$ low	$t_{d(EMHZ-HOLDAL)}$		0	2E	
4	Delay time, $\overline{HOLD}$ high to EMIF bus low impedance	$t_{d(HOLDH-EMLZ)}$		2E	7E	
5	Delay time, EMIFA bus low impedance to $\overline{HOLDA}$ high	$t_{d(EMLZ-HOLDAH)}$		0	2E	
	BUSREQ TIMING					
	Switching characteristics for the BUSREQ cycles for EMIFA modukle					
1	Delay time, AECLKOUTx high to ABUSREQ valid	$t_{d(AEKOH-ABUSRV)}$	See figure 20	1	5.5	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No.	Test	Symbol	Test condition 2/ Device types: All	Limits				Unit
				Standard mode		Fast mode		
				Min	Max	Min	Max	
	INTER-INTEGRATED CIRCUITS (I2C) TIMING							
Timing requirements for I^2C timings								
1	Cycle time, SCL	$t_{c(SCL)}$	See figure 21	10		2.5		µs
2	Setup time, SCL high before SDA low (for a repeated START condition)	$t_{su(SCLH-SDAL)}$		4.7		0.6		
3	Hold time, SCL low after SDA low (for a START and a repeated START condition)	$t_{h(SCLL-SDAL)}$		4		0.6		
4	Pulse duration, SCL low	$t_{w(SCLL)}$		4.7		1.3		
5	Pulse duration, SCL high	$t_{w(SCLH)}$		4		0.6		
6	Setup time, SDA valid before SCL high	$t_{su(SDAV-SDLH)}$		250		100 37/		ns
7	Hold time, SDA valid after SCL low	$t_{h(SDA-SDLL)}$		0 38/		0 38/	0.9 39/	µs
8	Pulse duration, SDA high between STOP and START conditions	$t_{w(SDAH)}$		4.7		1.3		
9	Rise time, SDA	$t_{r(SDA)}$			1000	$20+0.1C_b$ 40/	300	ns
10	Rise time, SCL	$t_{r(SCL)}$			1000	$20+0.1C_b$ 40/	300	
11	Fall time, SDA	$t_{f(SDA)}$			300	$20+0.1C_b$ 40/	300	
12	Fall time, SCL	$t_{f(SCL)}$			300	$20+0.1C_b$ 40/	300	
13	Setup time, SCL high before SDA high (for STOP condition)	$t_{su(SCLH-SDAH)}$		4		0.6		µs
14	Pulse duration, spike (must be suppressed)	$t_{w(SP)}$				0	50	ns
15	Capacitive load for each bus line	C_b 40/			400		400	pF
Switching characteristics for I^2C timings								
16	Cycle time, SCL	$t_{c(SCL)}$	See figure 22	10		2.5		µs
17	Delay time, SCL high to SDA low (for a repeated START condition)	$t_{d(SCLH-SDAL)}$		4.7		0.6		
18	Delay time, SDA low to SCL low (for a START and a repeated START condition)	$t_{d(SDAL-SCLL)}$		4		0.6		
19	Pulse duration, SCL low	$t_{w(SCLL)}$		4.7		1.3		
20	Pulse duration, SCL high	$t_{w(SCLH)}$		4		0.6		
21	Delay time, SDA valid to SCL high	$t_{d(SDAV-SDLH)}$		250		100 31/		ns
22	Valid time, SDA valid after SCL low	$t_{v(SDLL-SDAV)}$		0 32/		0 32/	0.9 33/	µs
23	Pulse duration, SDA high between STOP and START conditions	$t_{w(SDAH)}$		4.7		1.3		
24	Rise time, SDA	$t_{r(SDA)}$			1000	$20+0.1C_b$ 40/	300	ns
25	Rise time, SCL	$t_{r(SCL)}$			1000	$20+0.1C_b$ 40/	300	
26	Fall time, SDA	$t_{f(SDA)}$			300	$20+0.1C_b$ 40/	300	
27	Fall time, SCL	$t_{f(SCL)}$			300	$20+0.1C_b$ 40/	300	
28	Delay time, SCL high to SDA high (for STOP condition)	$t_{d(SCLH-SDAH)}$		4		0.6		µs
29	Capacitive load for each I^2C pin	C_b			10		10	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test condition 2/ Device types: All	Limits		Unit
				Min	Max	
	HOST PORT INTERFACE (HPI) PERIPHERAL					
	Timing requirements for host port interface cycles 41/ 42/					
9	Setup time, $\overline{HAS}$ low before $\overline{HSTROBE}$ low	$t_{su(HASL-HSTBL)}$	See figure 23-30	5		ns
10	Hold time, $\overline{HAS}$ low after $\overline{HSTROBE}$ low	$t_{h(HSTBL-HASL)}$		2		
11	Setup time, select signals 43/ valid before $\overline{HAS}$ low	$t_{su(SELV-HASL)}$		5		
12	Hold time, select signals 43/ valid after $\overline{HAS}$ low	$t_{h(HASL-SELV)}$		5		
13	Pulse duration, time, $\overline{HSTROBE}$ low	$t_{w(HSTBL)}$		15		
14	Pulse duration, time, $\overline{HSTROBE}$ high between consecutive accesses	$t_{w(HSTBH)}$		2M		
15	Setup time, select signals 43/ valid before $\overline{HSTROBE}$ low	$t_{su(SELV-HSTBL)}$		5		
16	Hold time, select signals 43/ valid after $\overline{HSTROBE}$ low	$t_{h(HSTBL-SELV)}$		5		
17	Setup time, host data valid before $\overline{HSTROBE}$ high	$t_{su(HDV-HSTBH)}$		5		
18	Hold time, host data valid after $\overline{HSTROBE}$ high	$t_{h(HSTBH-HDV)}$		1		
37	Setup time, $\overline{HCS}$ low before $\overline{HSTROBE}$ low	$t_{su(HCSL-HSBTL)}$		0		
37	Hold time, $\overline{HSTROBE}$ low after $\overline{HRDY}$ low. $\overline{HSTROBE}$ should not be inactivated until $\overline{HRDY}$ is active (low); otherwise, HPI writes will not complete properly.	$t_{h(HRDYL-HSTBL)}$		1.1		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test		Symbol	Test condition 2/ Device types: All	Limits		Unit
					Min	Max	
HOST PORT INTERFACE (HPI) PERIPHERAL (Continued)							
Switching characteristics during host port interface cycles 41/ 42/							
1	Delay time, $\overline{\text{HSTROBE}}$ low to DSP data valid	Case 1. HPIC or HPIA read	$t_{d(HSTBL-HDV)}$	See figure 23-30	5	15	ns
		Case 2. HPID read with no auto-increment				9*M+20	
		Case 3. HPID read with auto-increment and read FIFO initially empty 43/				9*M+20	
		Case 4. HPID read with auto-increment and data previously prefetched into the read FIFO			5	15	
2	Disable time, HD high impedance from $\overline{\text{HSTROBE}}$ high		$t_{dis(HSTBH-HDV)}$		1	4	
3	Enable time, HD driven from $\overline{\text{HSTROBE}}$ low		$t_{en(HSTBL-HD)}$		3	15	
4	Delay time, $\overline{\text{HSTROBE}}$ low to $\overline{\text{HRDY}}$ high		$t_{d(HSTBL-HRDYH)}$			12	
5	Delay time, $\overline{\text{HSTROBE}}$ high to $\overline{\text{HRDY}}$ high		$t_{d(HSTBH-HRDYH)}$			12	
6	Delay time, $\overline{\text{HSTROBE}}$ low to $\overline{\text{HRDY}}$ low	Case 1. HPID read with no auto-increment 43/	$t_{d(HSTBL-HRDYL)}$			10*M+20	
		Case 2. HPID read with auto-increment and read FIFO initially empty 43/				10*M+20	
7	Delay time, HD valid to $\overline{\text{HRDY}}$ low		$t_{d(HDV-HRDYL)}$		0		
34	Delay time, $\overline{\text{HSTROBE}}$ high to $\overline{\text{HRDY}}$ low	Case 1. HPIA write 43/	$t_{d(DSH-HRDYL)}$			5*M+20	
		Case 2. HPID write with no auto-increment 43/				5*M+20	
35	Delay time, $\overline{\text{HSTROBE}}$ high to $\overline{\text{HRDY}}$ low for HPIA write and FIFO not empty 43/		$t_{d(HSTBL-HRDYL)}$			40*M+20	
36	Delay time, $\overline{\text{HAS}}$ low to $\overline{\text{HRDY}}$ high		$t_{d(HASL-HRDYH)}$			12	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test condition 2/ Device types: All		Limits Min	Limits Max	Unit
	MULTICHANNEL BUFFERED SERIAL PORT (McBSP) TIMING						
Timing requirements for McBSP 44/							
2	Cycle time, CLKR/X	$t_{c(CKRX)}$	See figure 31	CLKR/X ext	6P or 10 8/ 45/		ns
3	Pulse duration, CLKR/X high or CLKR/X low	$t_{w(CKRX)}$		CLKR/X ext	$0.5t_{c(CKRX)} – 1$ 46/		
5	Setup time, external FSR high before CLKR low	$t_{su(FRH-CKRL)}$		CLKR int	9		
				CLKR ext	1.3		
6	Hold time, external FSR high after CLKR low	$t_{h(CKRL-FRH)}$		CLKR int	6		
				CLKR ext	3		
7	Setup time, DR valid before CLKR low	$t_{su(DRV-CKRL)}$		CLKR int	8		
				CLKR ext	0.9		
8	Hold time, DR valid after CLKR low	$t_{h(CKRL-DRV)}$		CLKR int	3		
				CLKR ext	3.1		
10	Setup time, external FSX high before CLKX low	$t_{su(FXH-CKXL)}$		CLKR int	9		
				CLKR ext	1.3		
11	Hold time, external FSX high after CLKX low	$t_{h(CKXL-FXH)}$		CLKR int	6		
				CLKR ext	3		
Switching characteristics for McBSP 44/ 47/							
1	Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input 48/	$t_{d(CKSH-CKRXH)}$	See figure 31		1.4	10	ns
2	Cycle time, CLKR/X	$t_{c(CKRX)}$		CLKR/X int	6P or 10 8/ 49/ 50/		
3	Pulse duration, CLKR/X high or CLKR/X low	$t_{w(CKRX)}$		CLKR/X int	C-1 51/	C+1 51/	
4	Delay time, CLKR high to internal FSR valid	$t_{d(CKRH-FRV)}$		CLKR int	-2.1	3.3	
9	Delay tine, CLKR high to internal FSX valid	$t_{d(CKXH-FXV)}$		CLKX int	-1.7	3	
				CLKX ext	1.7	9	
12	Disable time, DX high impedance following last data bit from CLKX high	$t_{d(CKXH-DXHZ)}$		CLKX int	-3.9	4	
				CLKX ext	2.1	9	
13	Delay time, CLKX high to DX valid	$t_{d(CKXH-DXV)}$		CLKX int	-3.9+D1 52/	4+D2 52/	
				CLKX ext	2.1+D1 52/	9+D2 52/	
14	Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode	$t_{d(FXH-DXV)}$		FSX int	-2.3+D1 53/	5.6+D2 53/	
				FSX ext	1.9+D1 53/	9+D2 53/	
Timing requirements for FSR when GSYNC = 1							
1	Setup time, FSR high before CLKS high	$t_{su(FRH-CKSH)}$	See figure 32		4		ns
2	Hold time, FSR high after CLKS high	$t_{h(CKSH-FRH)}$			4		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test condition 2/ Device types: All	Limits				Unit
				Master		Slave		
				Min	Max	Min	Max	
MULTICHANNEL BUFFERED SERIAL PORT (McBSP) TIMING - CONTINUED								
Timing requirements for McBSP as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0 8/ 54/								
4	Setup time, DR valid before CLKX low	$t_{su(DRV-CKXL)}$	See figure 33	12		2-18P		ns
5	Hold time, DR valid after CLKX low	$t_{h(CKXL-DRV)}$		4		5+36P		
Switching characteristics for McBSP as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0 8/ 54/								
1	Hold time, FSX low after CLKX low 55/	$t_{h(CKXL-FXL)}$	See figure 33	T-2	T+3			ns
2	Delay time, FSX low to CLKX high 56/	$t_{d(FXL-CKXH)}$		L-2	L+3			
3	Delay time, CLKX high to DX valid	$t_{d(CKXH-DXV)}$		-2	4	18P+2.8	30P+17	
6	Disable time, DX high impedance following last data bit for CLKX low	$t_{dis(CKXL-DXHZ)}$		L-2	L+3			
7	Disable time, DX high impedance following last data bit from FSX high	$t_{dis(FXH-DXHZ)}$				6P+3	18P+17	
8	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$				12P+2	24P+17	
Timing requirements for McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0 8/ 54/								
4	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	See figure 34	12		2-18P		ns
5	Hold time, DR valid after CLKX high	$t_{h(CKXH-DRV)}$		4		5+36P		
Switching characteristics for McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0 8/ 54/								
1	Hold time, FSX low after CLKX low 55/	$t_{h(CKXL-FXL)}$	See figure 34	L-2	L+3			ns
2	Delay time, FSX low to CLKX high 56/	$t_{d(FXL-CKXH)}$		T-2	T+3			
3	Delay time, CLKX low to DX valid	$t_{d(CKXL-DXV)}$		-2	4	18P+2.8	30P+17	
6	Disable time, DX high impedance following last data bit for CLKX low	$t_{dis(CKXL-DXHZ)}$		-2	4	18P+3	30P+17	
7	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$		H-2	H+4	12P+2	24P+17	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test condition 2/ Device types: All	Limits				Unit
				Master		Slave		
				Min	Max	Min	Max	
MULTICHANNEL BUFFERED SERIAL PORT (McBSP) TIMING - CONTINUED								
Timing requirements for McBSP as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1 8/ 54/								
4	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	See figure 35	12		2-18P		ns
5	Hold time, DR valid after CLKX high	$t_{h(CKXH-DRV)}$		4		5+36P		
Switching characteristics for McBSP as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1 8/ 54/								
1	Hold time, FSX low after CLKX high 55/	$t_{h(CKXH-FXL)}$	See figure 35	T-2	T+3			ns
2	Delay time, FSX low to CLKX low 56/	$t_{d(FXL-CKXL)}$		H-2	H+3			
3	Delay time, CLKX low to DX valid	$t_{d(CKXL-DXV)}$		-2	4	18P+2.8	30P+17	
6	Disable time, DX high impedance following last data bit for CLKX high	$t_{dis(CKXH-DXHZ)}$		H-2	H+3			
7	Disable time, DX high impedance following last data bit from FSX high	$t_{dis(FXH-DXHZ)}$				6P+3	18P+17	
8	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$				12P+2	24P+17	
Timing requirements for McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1 8/ 54/								
4	Setup time, DR valid before CLKX high	$t_{su(DRV-CKXH)}$	See figure 36	12		2-18P		ns
5	Hold time, DR valid after CLKX high	$t_{h(CKXH-DRV)}$		4		5+36P		
Switching characteristics for McBSP as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1 8/ 54/								
1	Hold time, FSX low after CLKX high 55/	$t_{h(CKXH-FXL)}$	See figure 36	H-2	H+3			ns
2	Delay time, FSX low to CLKX low 56/	$t_{d(FXL-CKXL)}$		T-2	T+1			
3	Delay time, CLKX high to DX valid	$t_{d(CKXH-DXV)}$		-2	4	18P+2.8	30P+17	
6	Disable time, DX high impedance following last data bit for CLKX high	$t_{dis(CKXH-DXHZ)}$		-2	4	18P+3	30P+17	
7	Delay time, FSX low to DX valid	$t_{d(FXL-DXV)}$		L-2	L+4	12P+2	24P+17	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No.	Test	Symbol	Test condition 2/ Device types: All	Limits						Unit
				Min	Max	Min	Max	Min	Max	
EMAC MII AND GMII ELECTRICAL DATA/TIMING										
Timing requirements for MRCLK – MII and GMII operation				1000 Mbps (GMII only)		100 Mbps		10 Mbps		
1	Cycle time, MRCLK	$t_{c(MRCLK)}$	See figure 37	8		40		400		ns
2	Pulse duration, MRCLK high	$t_{w(MRCLKH)}$		2.8		14		140		
3	Pulse duration, MRCLK low	$t_{w(MRCLKL)}$		2.8		14		140		
4	Transition time, MRCLK	$t_{t(MRCLK)}$			1		3		3	
Timing requirements for MTCLK-NII and GMII operation						100 Mbps		10 Mbps		
1	Cycle time, MTCLK	$t_{c(MTCLK)}$	See figure 38			40		400		ns
2	Pulse duration, MTCLK high	$t_{w(MTCLKH)}$				14		140		
3	Pulse duration, MTCLK low	$t_{w(MTCLKL)}$				14		140		
4	Transition time, MTCLK	$t_{t(MTCLK)}$					3		3	
Switching Characteristics for GMTCLK – GMII operation								1000 Mbps		
1	Cycle time, GMTCLK	$t_{c(GMTCLK)}$	See figure 39					8		ns
2	Pulse duration, GMTCLK high	$t_{w(GMTCLKH)}$						2.8		
3	Pulse duration, GMTCLK low	$t_{w(GMTCLKL)}$						2.8		
4	Transition time, GMTCLK	$t_{t(GMTCLK)}$							1	
Timing requirements for EMAC MII and GMII receive 10/100/1000 Mbits 57/						1000 Mbps		100/10 Mbps		
1	Setup time, receive selected signals valid before MRCLK high	$t_{su(MRXD-MRCLKH)}$	See figure 40			2		8		ns
2	Hold time, receive selected signals valid before MRCLK high	$t_{h(MRXD-MRCLKH)}$				0		8		
Switching characteristics for EMAC MII and GMII transmit 10/100 Mbit/s 58/								100/10 Mbps		
1	Delay time, MTCLK high to transmit selected signals valid	$t_{d(MTCLKH-MTXD)}$	See figure 41					5	25	ns
Switching characteristics for EMAC MII and GMII transmit 1000 Mbit/s 59/								1000 Mbps		
1	Delay time, GMTCLK high to transmit selected signals valid	$t_{d(GMTCLKH-MTXD)}$	See figure 42					0.5	5	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No.	Test	Symbol	Test condition 2/ Device types: All		Min	Max	Unit
	EMAC RMII ELECTRICAL DATA/TIMING						
Timing requirements for RMREFCLK – RMII operation							
1	Pulse duration, RMREFCLK high	$t_{w(RMREFCLKH)}$	See figure 43		7	13	ns
2	Pulse duration, RMREFCLK low	$t_{w(RMREFCLKL)}$			7	13	
3	Transition time, RMREFCLK	$t_{t(RMREFCLK)}$				2	
Switching characteristics for EMAC RMII transmit 10/100 Mbit/s 60/							
1	Delay time, RMREFCLK high to transmit selected signals valid	$t_{d(RMREFCLKH-MTXD)}$	See figure 44		3	10	ns
Timing requirements for EMAC RMII input receive for 100 Mbps 61/							
1	Setup time, receive selected signals valid before MREFCLK (at DSP) high/low	$t_{su(MRXD-MREFCLK)}$	See figure 45		4.0		ns
2	Hold time, receive selected signals valid after MREFCLK (at DSP) high/low	$t_{h(MREFCLK-MRXD)}$			3.0		
	EMAC RGMII ELECTRICAL DATA/TIMING						
Switching characteristics for EMAC RGREFCLK - RGMII							
1	Cycle time, RGREFCLK	$t_{c(RGREFCLK)}$	See figure 46		8-0.8	8+0.8	ns
2	Pulse duration, RGREFCLK high	$t_{w(RGREFCLK H)}$			3.2	4.8	
3	Pulse duration, RGREFCLK low	$t_{w(RGREFCLK L)}$			3.2	4.8	
4	Transition time, RGREFCLK	$t_{t(RGREFCLK))}$				0.75	
Timing requirements for RXC – RGMII operation							
1	Cycle time, RXC	$t_{c(RXC)}$	See figure 47	10 Mbps	360	440	ns
				100 Mbps	36	44	
				1000 Mbps	7.2	8.8	
2	Pulse duration, RXC high	$t_{w(RXCH)}$		10 Mbps	0.40* $t_{c(RXC)}$	0.60* $t_{c(RXC)}$	
				100 Mbps	0.40* $t_{c(RXC)}$	0.60* $t_{c(RXC)}$	
				1000 Mbps	0.45* $t_{c(RXC)}$	0.55* $t_{c(RXC)}$	
3	Pulse duration, RXC low	$t_{w(RXCL)}$		10 Mbps	0.40* $t_{c(RXC)}$	0.60* $t_{c(RXC)}$	
				100 Mbps	0.40* $t_{c(RXC)}$	0.60* $t_{c(RXC)}$	
				1000 Mbps	0.45* $t_{c(RXC)}$	0.55* $t_{c(RXC)}$	
4	Transition time, RXC	$t_{t(RXC)}$		10 Mbps		0.75	
				100 Mbps		0.75	
				1000 Mbps		0.75	
Timing requirements for EMAC RGMII input receive for 10/100/1000 Mbps 62/							
5	Setup time, receive selected signals valid before RXC (at DSP) high/low	$t_{su(RXD-RXCH)}$	See figure 47		1.0		ns
6	Hold time, receive selected signals valid after RXC (at DSP) high/low	$t_{h(RXCH-RXD)}$			1.0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No.	Test	Symbol	Test condition 2/ Device types: All		Min	Max	Unit
EMAC RGMII ELECTRICAL DATA/TIMING - Continued							
Switching characteristics for TXC – RGMII operation for 10/100/1000 Mbit/s							
1	Cycle time, TXC	$t_{c(TXC)}$	See figure 47	10 Mbps	360	440	ns
				100 Mbps	36	44	
				1000 Mbps	7.2	8.8	
2	Pulse duration, TXC high	$t_{w(TXCH)}$		10 Mbps	0.40* $t_{c(TXC)}$	0.60* $t_{c(TXC)}$	
				100 Mbps	0.40* $t_{c(TXC)}$	0.60* $t_{c(TXC)}$	
				1000 Mbps	0.45* $t_{c(TXC)}$	0.55* $t_{c(TXC)}$	
3	Pulse duration, TXC low	$t_{w(TXCL)}$		10 Mbps	0.40* $t_{c(TXC)}$	0.60* $t_{c(TXC)}$	
				100 Mbps	0.40* $t_{c(TXC)}$	0.60* $t_{c(TXC)}$	
				1000 Mbps	0.45* $t_{c(TXC)}$	0.55* $t_{c(TXC)}$	
4	Transition time, TXC	$t_{t(TXC)}$		10 Mbps		0.75	
				100 Mbps		0.75	
				1000 Mbps		0.75	
Switching characteristics for EMAC RGMII transmit 63/							
5	Setup time, transmit selected signals valid before TXC (at DSP) high/low	$t_{su(RXD-RXCH)}$	See figure 48		1.2		ns
6	Hold time, transmit selected signals valid after TXC (at DSP) high/low	$t_{h(RXCH-RXD)}$			1.2		
MDIO ELECTRICAL DATA/TIMING							
Timing requirements for MDIO input (R)(G)MII							
1	Cycle time, MDCLK	$t_{c(MDCLK)}$	See figure 49		400		ns
2a	Pulse duration, MDCLK high	$t_{w(MDCLKH)}$			180		
2b	Pulse duration, MDCLK low	$t_{w(MDCLKL)}$			180		
3	Transition time, MDCLK	$t_{w(MDCLKL)}$				5	
4	Setup time, MDIO data input valid before MDCLK high	$t_{su(MDIO-MDCLKH)}$			10		
5	Hold time, MDIO data input valid afterMDCLK high	$t_{h(MDCLKH-MDIO)}$			10		
Switching characteristics for MDIO output							
7	Delay time, MDCLK low to MDIO data output valid	$t_{d(MDCLKL-MDIO)}$	See figure 50			100	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test condition 2/ Device type: All	Limits		Unit
				Min	Max	
	TIMERS ELECTRICAL DATA TIMING					
Timing requirements for timers inputs 8/						
1	Pulse duration, TINPLx high	$t_{w(TINPH)}$	See figure 51	12P		ns
2	Pulse duration, TINPLx low	$t_{w(TINPL)}$		12P		
Switching characteristics for timer output 8/						
3	Pulse duration, TOUTLx high	$t_{w(TOUTH)}$	See figure 51	12P – 3		ns
4	Pulse duration, TOUTLx low	$t_{w(TOUTL)}$		12P - 3		
	UTOPIA ELECTRICAL DATA/TIMING					
Timing requirements for UXCLK 64/						
1	Cycle time, UXCLK	$t_{c(UXCK)}$	See figure 52	20		ns
2	Pulse duration, UXCLK high	$t_{w(UXCKH)}$		$0.4t_{c(UXCK)}$	$0.6t_{c(UXCK)}$	
3	Pulse duration, UXCLK low	$t_{w(UXCKIL)}$		$0.4t_{c(UXCK)}$	$0.6t_{c(UXCK)}$	
4	Transition time, UXCLK	$t_{t(UXCK)}$			2	
Timing requirements for URCLK 64/						
1	Cycle time, UXCLK	$t_{c(URCXK)}$	See figure 53	20		ns
2	Pulse duration, UXCLK high	$t_{w(URCKH)}$		$0.4t_{c(URCK)}$	$0.6t_{c(URCK)}$	
3	Pulse duration, UXCLK low	$t_{w(URCKIL)}$		$0.4t_{c(URCK)}$	$0.6t_{c(URCK)}$	
4	Transition time, UXCLK	$t_{t(URCK)}$			2	
Timing requirements for UTOPIA slave transmit						
2	Setup time, UXADDR valid before UXCLK high	$t_{su(UXAV-UXCH)}$	See figure 54	4		ns
3	Hold time, UXADDR valid after UXCLK high	$t_{h(UXCH-UXAV)}$		1		
8	Setup time, $\overline{UXENB}$ low before UXCLK high	$t_{su(UXENBL-UXCH)}$		4		
9	Hold time, $\overline{UXENB}$ low after UXCLK high	$t_{h(UXCH-UXENBL)}$		1		
Switching characteristics for UTOPIA slave transmit cycles						
1	Delay time, UXCLK high to UXDATA valid	$t_{d(UXCH-UXDV)}$	See figure 54	3	12	ns
4	Delay time, UXCLK high to UXCLAV driven active value	$t_{d(UXCH-UXCLAV)}$		3	12	
5	Delay time, UXCLK high to UXCLAV driven inactive value	$t_{d(UXCH-UXCLAVL)}$		3	12	
6	Delay time, UXCLK high to UXCLAV going Hi-Z	$t_{d(UXCH-UXCLAVHZ)}$		9	18.5	
7	Pulse duration (low), UXCLAV low to UXCLAV Hi-Z	$t_{w(UXCLAVL-UXCLAVHZ)}$		3		
10	Delay time, UXCLK high to UXSOC valid	$t_{d(UXCH-UXSV)}$		3	12	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

No	Test	Symbol	Test condition 2/ Device type: All	Limits		Unit
				Min	Max	
	TIMERS ELECTRICAL DATA TIMING (Continued)					
Timing requirements for UTOPIA slave receive						
1	Setup time, URDATA valid before URCLK high	$t_{su(URDV-URCH)}$	See figure 55	4		ns
2	Hold time, URADDR valid after URCLK high	$t_{h(URCH-URDV)}$		1		
3	Setup time, URADDR valid before URCLK high	$t_{su(URAV-URCH)}$		4		
4	Hold time, URADDR valid after URCLK high	$t_{h(URCH-URAV)}$		1		
9	Setup time, $\overline{\text{URENB}}$ valid before URCLK high	$t_{su(URENBL-URCH)}$		4		
10	Hold time, $\overline{\text{URENB}}$ valid after URCLK high	$t_{h(URCH-URENBL)}$		1		
11	Setup time, URSUOC high before URCLK high	$t_{su(URSH-URCH)}$		4		
12	Hold time, URSOC high after URCLK high	$t_{h(URCH-URSH)}$		1		
Switching characteristics for UTOPIA slave receive cycles						
5	Delay time, URCLK high to URCLAV driven active value	$t_{d(URCH-URCLAV)}$	See figure 55	3	12	ns
6	Delay time, URCLK high to URCLAV driven inactive value	$t_{d(URCH-URCLAV)}$		3	12	
7	Delay time, URCLK high to URCLAV going Hi-Z	$t_{d(URCH-URCLAV)}$		9	18.5	
8	Pulse duration (low), URCLAV low to URCLAV Hi-Z	$t_{w(URCLAV-URCLAVHZ)}$		3		
	GPIO ELECTRICAL DATA/TIMING					
Timing requirements for GPIO inputs 8/ 65/						
1	Pulse duration, GPIx high	$t_{w(GPIH)}$	See figure 56	12P		ns
2	Pulse duration, GPIx low	$t_{w(GPIL)}$		12P		
Switching characteristics for GPIO outputs 8/						
3	Pulse duration, GPOx high	$t_{w(GPOH)}$	See figure 56	36P-8 66/		ns
4	Pulse duration, GPOx low	$t_{w(GPOL)}$		36P-8 66/		
	JTAG TEST PORT TIMING					
Timing requirements for JTAG test port						
1	Cycle time, TCK	$t_{c(TCK)}$	See figure 57	35		ns
3	Setup time, TDI/TMS/ $\overline{\text{TRST}}$ valid before TCK high	$t_{su(TDIV-TCKH)}$		10		
4	Hold time, TDI/TMS/ $\overline{\text{TRST}}$ valid after TCK high	$t_{h(TCKH-TDIV)}$		9		
Switching characteristics for JTAG test portns						
2	Delay time, TCK low to TDO valid	$t_{d(TCKL-TDOV)}$	See figure 57	-3	18	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Over recommended ranges of supply voltage. Operating case temperature T_C = 0°C to +90°C for device type 01, 02, 04 and -40°C to +105°C for device type 03. For test condition shown as MIN, MAX, use appropriate value specified in the recommended operating condition in section 1.4. Unless otherwise noted.

3/ These rated numbers are from PCI specification. The DC specification and AC specification are defined in manufacturer data.

4/ I_I applies to input only pins and bi-directional pins. For input only pins, I_I indicates the input leakage current. For bi-directional pins, I_I includes input leakage current and off-state (hi-Z) output leakage current.

5/ PCI input leakage currents include Hi-Z output leakage for all bidirectional buffers with 3-state outputs.

6/ I_{OZ} applies to output only pins, indicating off state (hi-Z) output leakage current.

7/ Assumes the following conditions: 60% CPU utilization; DDR2 at 50% utilization (250 MHz), 50% writes, 32 bits, 50% bit switching; two 2-MHz McBSP at 100% utilization, 50% switching; two 75 MHz timers at 100% utilization; device configured for HPI32 mode with pull up resistor on HPI pins; room temperature (25°C). The actual current draw is highly application dependent. For more details on core and I/O activity, see manufacturer data.

8/ P = 1/CPU clock frequency in ns. For example, when running parts at 1000 MHz, use P = 1 ns.

9/ C = 1/CLKIN1 clock frequency in ns.

10/ D = 1/CLKIN2 clock frequency in ns.

11/ P = 1/CPU clock frequency in ns. Note that after power-on reset, warm reset, and max reset the CPU frequency is equal to the CLKIN1 frequency divided by three doe to the PLL1 controller being reset. See manufacturer data for more information.

12/ If CLKIN2 is not used, $t_{w(POR)}$ must be measured in terms of CLKIN1 cycles; otherwise, use CLKIN2 cycles.

13/ AEAS[19:0], ABA[1:0], and PCI_EN are the boot configuration pins during device reset. Note: if a configuration pin must be routed out from the device and 3-stated (not driven), the internal pullup/pulldown (IPU/IPD) resistor should not be relied upon; The manufacturer recommends the use of an external pullup/pulldown resistor. See manufacturer for more data.

14/ The reference points for the rise and fall transactions are measured at 3.3 V V_{IL} Max and V_{IH} Min.

15/ For more details on the PLL multiplier factors (x1[BYPASS], x 15, x20, x25, x30, x32), see manufacturer data.

16/ The PLL1 multiplier factors (x1[BYPASS], x 15, x20, x25, x30, x32) further limit Min and Max values for $t_{c(CLKIN1)}$. See manufacturer for more data.

17/ PLL modes: x1(Bypass), x15, x20, x25, x30, x32

18/ Only applies when the PLL1 controller is set to PLL mode (PLLEN = 1 in the PLLCTL register).

19/ SYSCLK1 restriction applies only when the EMAC is enabled and the RGMII modes are used. SYSCLK1 must be programmed to 125 MHz when the GMII mode is used and to 50 MHz when the RGMII mode is used.

20/ C = CLKIN2 cycle time in ns. For example, when CLKIN2 frequency is 25 MHz, use C = 40 ns.

21/ If EMAC is enabled with RGMII, CLKIN2 cycle time must be 40 ns (25 MHz).

22/ E = the EMIF input clock (AECLKIN or SYSCLK4) period in ns for EMIFA.

23/ Minimum AECLKIN cycle times must be met, even when AECLKIN is generated by an internal clock source. Minimum AECLKIN times are based on internal logic speed; the maximum useable speed of the EMIF may be lower due to AC timing requirements.

24/ This timing is only applies when AECLKIN is used for EMIFA.

25/ The reference points for the rise and fall transactions are measured at V_{OL} Max and V_{OH} min

26/ EH is the high period of E (EMIF input clock period) in ns and EL is the low period of E (EMIF input clock period) in ns for EMIFA.

27/ E = AECLKOUT period in ns for EMIFA.

28/ To ensure data setup time, simply program the strobe width wide enough.

29/ AARDY is internally synchronized. To use AARDY as an asynchronous input, the pulse width of the AARDY signal should be at least 2E to ensure setup and hold time is met.

TABLE I. Electrical performance characteristics - Continued.

30/ RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold. These parameters are programmed via EMIFA CE configuration registers (CEnCFG).

31/ Select signals for EMIFA include: $\overline{\text{ACEx}}$, $\overline{\text{ABE[7:0]}}$, AEA[19:0], ABA[1:0]; and for EMIFA writes, also include AR/$\overline{\text{W}}$, AED[63:0].

32/ The following parameters are programmable via the EMIFA CE configuration registers (CEnCFG):
- Read latency (R_LTNCY):0-, 1-, 2-, or 3-cycle read latency
- Write latency (W_LTNCY):0-, 1-, 2-, or 3-cycle write latency
- $\overline{\text{ACEx}}$ assertion length (CE_EXT): For standard SBSRAM or ZBT SRAM interface, $\overline{\text{ACEx}}$ goes inactive after final command has been issued (CE_EXT = 0). For synchronous FIFO interface with glue, $\overline{\text{ACEx}}$ is active when $\overline{\text{ASOE}}$ is active (CE_EXT = 1)
- Function of $\overline{\text{ASADS}}$ / $\overline{\text{ASRE}}$ (R_ENABLE): For standard SBSRAM or ZBT SRAM interface, $\overline{\text{ASADS}}$ / $\overline{\text{ASRE}}$ acts as $\overline{\text{ASADS}}$ with deselect cycles (R_ENABLE = 0). For FIFO interface, $\overline{\text{ASADS}}$ / $\overline{\text{ASRE}}$ acts as $\overline{\text{ASRE}}$ with NO deselect cycles (R_ENABLE = 1).

33/ E = the EMIF input clock (ECLKIN) period in ns for EMIFA.

34/ EMIFA bus consists of: $\overline{\text{ACE[5:2]}}$, $\overline{\text{ABE[7:0]}}$, AED[63:0], AEA[19:0], ABA[1:0], AR/$\overline{\text{W}}$, $\overline{\text{ASADS}}$ / $\overline{\text{ASRE}}$, $\overline{\text{AAOE}}$ / $\overline{\text{ASOE}}$, and $\overline{\text{AAWE}}$ / $\overline{\text{ASWE}}$.

35/ All pending EMIF transactions are allowed to complete before $\overline{\text{HOLDA}}$ is asserted. If no bus transactions are occurring, then the minimum delay time can be achieved.

36/ The I^2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.

37/ A fast mode I^2C bus device can be used in a standard mode I_2C bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r max + $t_{su(SDA-SCLH)}$ = 1000 + 250 = 1250 ns (according to the standard mode I^2C bus specification) before the SCL line is released.

38/ A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL

39/ The maximum $t_{h(SDA-SCLL)}$ has only to be met if the device does not stretch the low period [$t_{w(SCLL)}$] of the SCL signal.

40/ C_b = total capacitance of one bus line in pF. If mixed with HS mode devices, faster fall time are allowed.

41/ $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$:[NOT($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{HCS}}$.

42/ m = sysclk3 PERIOD = 6/cpu CLOCK FREQUENCY IN NS. For example, when running parts at 1000 MHz, use M = 6 ns.

43/ Select signals include: HCNTL[1:0] and HR/$\overline{\text{W}}$. For HPI16 mode only, select signals also include HHWIL

44/ CLKRP = CLKXP = FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

45/ Use whichever value is greater. Minimum CLKR/X cycle times must be met, even when CLKR/X is generated by an internal clock source. Minimum CLRK/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.

46/ This parameter applies to the maximum McBSP frequency. Operate serial clock (CLKR/X) in the reasonable range of 40/60 duty cycle.

47/ Minimum delay times also represent minimum output hold times.

48/ The CLKS signal is shared by both McBSP0 and McBSP1 on this device.

49/ Minimum CLKR/X cycle times must be met, even when CLKR/X is generated by an internal clock source. Minimum CLRK/X cycle times are based on internal logic speed; the maximum usable speed may be lower due to EDMA limitations and AC timing requirements.

50/ Use whichever value is greater.

51/ C = H or L
S = Sample rate generator input clock = 6P if CLKSM = 1 (P = 1/CPU clock frequency)
= Sample rate generator input clock = P_clks if CLKSM = 0 (P_clks = CLKS period)
T = CLKX period = (1 + CLKGDV) * S
H = CLKX high pulse width = (CLKGDV/2 + 1) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd
L = CLKX low pulse width = (CLKGDV/2) * S if CLKGDV is even
= (CLKGDV + 1)/2 * S if CLKGDV is odd
CLKGDV should be set appropriately to ensure the McBSP bit rate does not exceed the maximum limit (see 49/ above).

52/ Extra delay from CLKX high to DX valid applies only to the first data bit of a device, if and only if DXENA = 1 in SPCR.
If DXENA = 0, then D1 = D2 = 0
If DXENA = 1, then D1 = 6P, D2 = 12P

53/ Extra delay from FSX high to DX valid applies only to the first data bit of a device, if and only if DXENA = 1 in SPCR.
If DXENA = 0, then D1 = D2 = 0
If DXENA = 1, then D1 = 6P, D2 = 12P

54/ For all SPI Slave mode, CLKG is programmed as ¼ of the CPU clock by setting CLKSM = CLKGDV = 1

55/ FSRP = FSXP = 1. As a SPI Master, FSX is inverted to provide active low slave enable output. As a Slave, the active low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for Master McBSP
CLKXM = CLKRM =FSXM = FSRM = 0 for Slave McBSP

56/ FSX should be low before the rising edge of clock to enable Slave devices and then begin a SPI transfer at the rising edge of the Master clock (CLKX).

57/ For MII, receive selected signals include: MRXD[3:0], MRXDV, and MRXER. For GMII, receive selected signals include: MRXD[7:0], MRXDV, and MRXER.

58/ For MII, transmit selected signals include: MTXD[3:0] and MTXEN. For GMII, transmit selected signals include: GMTXD[7:0], and MTXEN.

59/ For GMII, transmit selected signals include: GMTXD[7:0], and MTXEN.

60/ For RMII, transmit selected signals include: MTXD[1:0] and MTXEN.

61/ For RMII, receive selected signals include: MRXD[1:0], MRXER, and MCRSDV.

62/ For RGMII, receive selected signals include: RXD[3:0], and MXCTL.

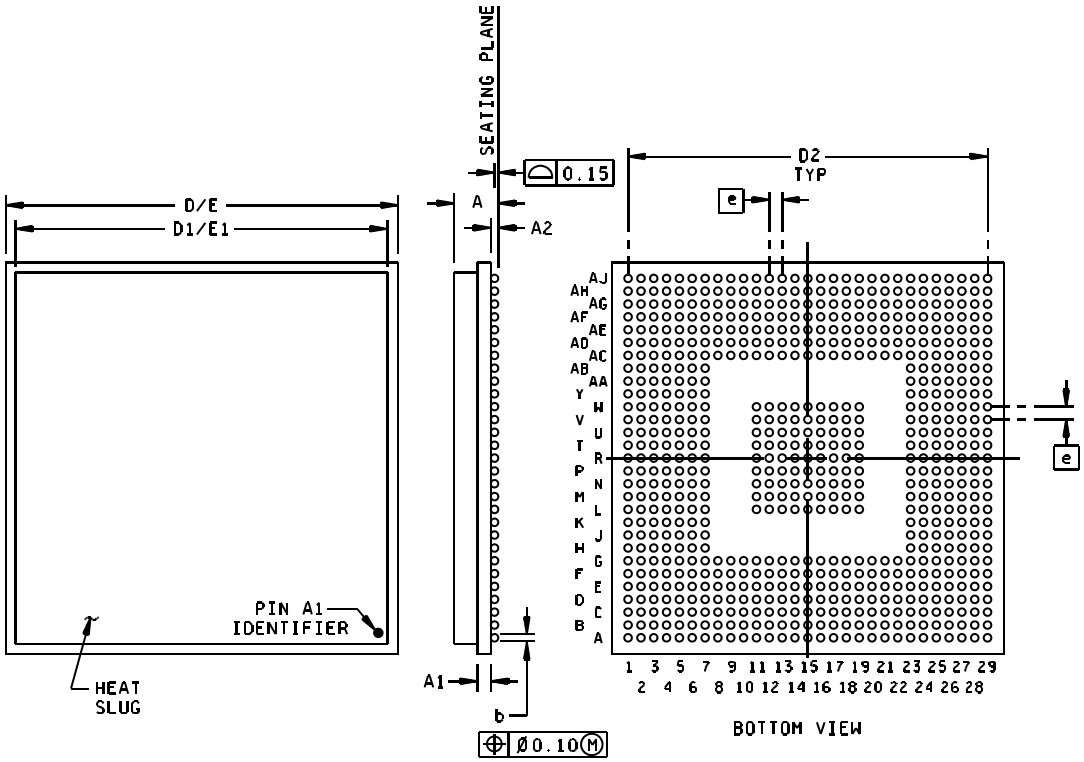
63/ For RGMII, transmit selected signals include: TXD[3:0], and TXCTL.

64/ The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.

65/ The pulse width given is sufficient to generate a CPU interrupt or an EDMA event. However, if a user wants to have DSP recognize the GPIx changes through software poliing of the HGPIO register, the GPIx duration must be extended to at least 24P to allow DSP enough time to access the GPIO register through CFGBUS.

66/ This parameter value should not be used as a maximum performance specification. Actual performance of back-to-back accesses of the GPIO is dependent upon internal bus activity.

Case X



Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		3.10	D/E	23.90	24.10
A1	1.09 NOM		D1	22.40 TYP	
A2	0.35	0.45	e	0.80 BSC	
b	0.45	0.55			

Notes:
1. This drawing is subject to change without notice.
2. Thermally enhanced plastic package with heat slug (HSL).
3. Flip chip application only.

FIGURE 1. Case outline.

Case X

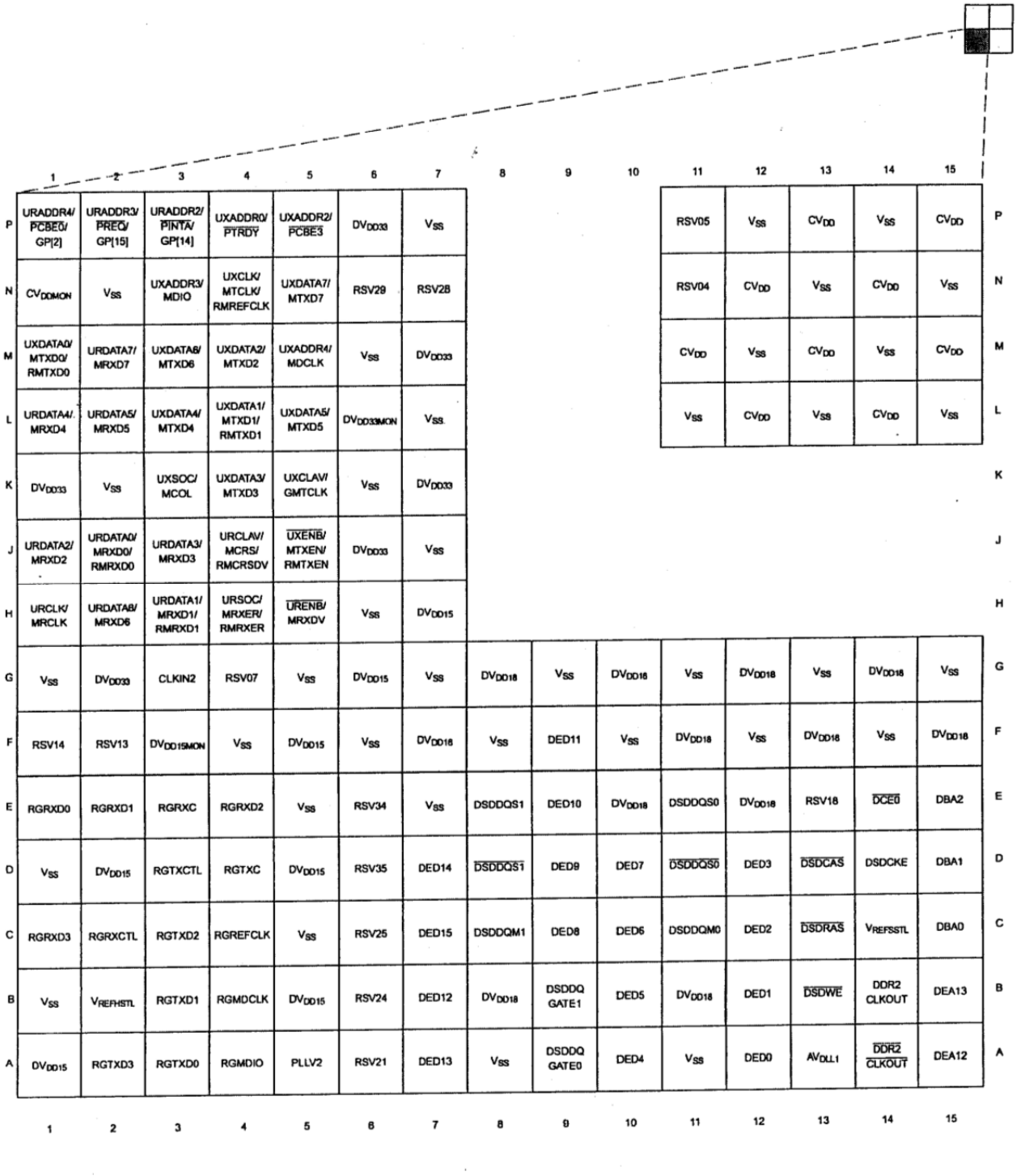


FIGURE 2. Terminal connections.

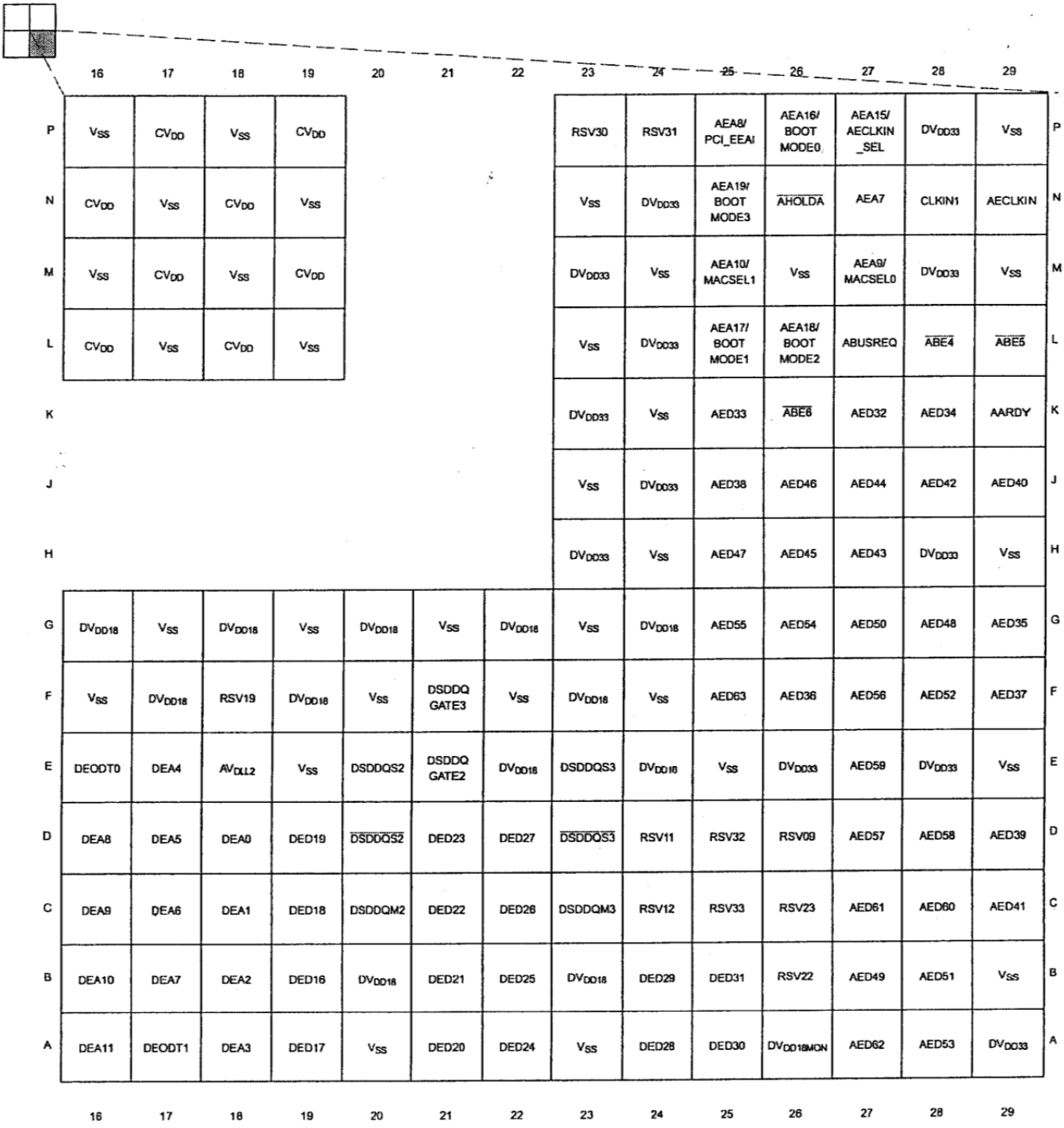


FIGURE 2. Terminal connections - Continued.

Case X

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
AJ	DV_{DD33}	GP[5]	FSX0	CLKS	DR0	TINPL1	DV_{DD33}	V_{SS}	TCK	TMS	RSV26	RSV40	SYSCLK4/ GP[1]	V_{SS}	DV_{DD33}	AJ
AH	V_{SS}	GP[4]	FSR0	NMI	DR1/ GP[8]	TINPL0	$\overline{TRST}$	TDO	TDI	EMU17	RSV27	EMU16	EMU9	DV_{DD33}	V_{SS}	AH
AG	CLKR0	GP[7]	GP[6]	FSX1/ GP[11]	DX1/ GP[9]	CLKX0	TOUTL1	EMU6	EMU2	RSV38	RSV39	DV_{DD33}	V_{SS}	$\overline{RESET}$	$\overline{RIOCLK}$	AG
AF	DV_{DD33}	V_{SS}	HD11/ AD11	CLKR1/ GP[0]	CLKX1/ GP[3]	DX0	EMU0	TOUTL0	EMU4	EMU3	EMU8	EMU7	EMU14	$\overline{POR}$	RIOCLK	AF
AE	HD22/ AD22	HD0/ AD0	HD10/ AD10	V_{SS}	FSR1/ GP[10]	DV_{DD33}	V_{SS}	DV_{DD33}	EMU15	EMU12	EMU1	EMU5	EMU18	$\overline{RESETSTAT}$	DV_{DD33}	AE
AD	HD21/ AD21	HD25/ AD25	HD5/ AD5	HD3/ AD3	DV_{DD33}	V_{SS}	DV_{DD33}	EMU13	RSV37	EMU10	RSV36	EMU11	V_{SS}	DV_{DD33}	V_{SS}	AD
AC	HD19/ AD19	HD13/ AD13	HD23/ AD23	HD29/ AD29	HD27/ AD27	DV_{DD33}	V_{SS}	V_{SS}	DV_{DD33}	V_{SS}	DV_{DD33}	V_{SS}	DV_{DD33}	V_{SS}	AV_{DDA}	AC
AB	HD17/ AD17	HD15/ AD15	HD9/ AD9	HD7/ AD7	HD1/ AD1	V_{SS}	DV_{DD33}									AB
AA	DV_{DD33}	V_{SS}	HD31/ AD31	HD28/ AD28	HD30/ AD30	DV_{DD33}	V_{SS}									AA
Y	HD26/ AD26	HD18/ AD18	HD16/ AD16	HD6/ AD6	HD4/ AD4	V_{SS}	DV_{DD33}									Y
W	HD24/ AD24	HD20/ AD20	RSV03	HD14/ AD14	HD8/ AD8	HD2/ AD2	V_{SS}				V_{SS}	CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	W
V	DV_{DD33}	V_{SS}	HHWIL/ PCLK	HD12/ AD12	RSV02	V_{SS}	DV_{DD33}				CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	DV_{DDRM}	V
U	$\overline{HDS2}$/ $\overline{PCBE1}$	$\overline{HDS1}$/ $\overline{PSERR}$	$\overline{HINT}$/ $\overline{PFRAME}$	HCNTL1/ $\overline{PDEVSEL}$	HCNTL0/ $\overline{PSTOP}$	$\overline{HCS}$/ $\overline{PPERR}$	V_{SS}				V_{SS}	CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	U
T	RSV15	RSV16	$\overline{HAS}$/ PPAR	$\overline{HRDY}$/ $\overline{PIRDY}$	HR/$\overline{W}$/ $\overline{PCBE2}$	V_{SS}	DV_{DD33}				CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	CV_{DD}	T
R	DV_{DD33}	V_{SS}	UXADDR1/ PIDSEL	URADDR0/ $\overline{PGNT}$/ GP[12]	URADDR1/ $\overline{PRST}$/ GP[13]	DV_{DD33}	V_{SS}				V_{SS}	CV_{DD}	V_{SS}	CV_{DD}	V_{SS}	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

FIGURE 2. Terminal connections - Continued.

Case X

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
AJ	V_{SS}	AV_{DDT}	RIORX2	$\overline{RIORX2}$	V_{SS}	$\overline{RIORX1}$	RIORX1	AV_{DDT}	V_{SS}	DV_{DD33}	AED5	AED6	AED20	DV_{DD33}	AJ
AH	DV_{DD33}	$\overline{RIORX3}$	RIORX3	V_{SS}	AV_{DDT}	V_{SS}	RIORX0	$\overline{RIORX0}$	DV_{DD33}	V_{SS}	AED14	AED2	AED18	V_{SS}	AH
AG	V_{SS}	DV_{DD33}	RIOTX2	$\overline{RIOTX2}$	V_{SS}	$\overline{RIOTX1}$	RIOTX1	DV_{DD33}	V_{SS}	AED3	SCL	AED9	AED16	AED30	AG
AF	DV_{DD33}	RIOTX3	$\overline{RIOTX3}$	V_{SS}	AV_{DDT}	V_{SS}	$\overline{RIOTX0}$	RIOTX0	DV_{DD33}	AED1	SDA	AED10	AED15	AED19	AF
AE	V_{SS}	AV_{DDT}	V_{SS}	AV_{DDT}	V_{SS}	RSV17	V_{SS}	AV_{DDT}	V_{SS}	AED7	AED12	AED4	AED13	AED17	AE
AD	AV_{DDA}	V_{SS}	DV_{DD33}	V_{SS}	DV_{DDR}	V_{SS}	DV_{DD33}	V_{SS}	DV_{DD33}	AED0	AED11	AED8	AED22	AED21	AD
AC	V_{SS}	AV_{DDA}	V_{SS}	DV_{DD33}	V_{SS}	DV_{DD33}	V_{SS}	DV_{DD33}	V_{SS}	AED24	AED26	AED28	V_{SS}	DV_{DD33}	AC
AB								V_{SS}	DV_{DD33}	$\overline{AAWE}$/ $\overline{ASWE}$	AED23	AED25	AED27	AED29	AB
AA								DV_{DD33}	V_{SS}	$\overline{ABE1}$	$\overline{ABE0}$	AED31	$\overline{ABE2}$	$\overline{ABE3}$	AA
Y								V_{SS}	DV_{DD33}	RSV43	RSV42	RSV44	$\overline{AAOE}$/ $\overline{ASOE}$	PCI_EN	Y
W	DV_{DD12}	V_{SS}	DV_{DD12}	V_{SS}				DV_{DD33}	V_{SS}	AR/$\overline{W}$	$\overline{ACE3}$	$\overline{ACE2}$	RSV41	$\overline{ABE7}$	W
V	V_{SS}	DV_{DDRM}	V_{SS}	CV_{DD}				V_{SS}	DV_{DD33}	ABA1/ EMIFA_EN	ABA0/ DDR2_EN	$\overline{ACE5}$	$\overline{ACE4}$	AECLKOUT	V
U	DV_{DDRM}	V_{SS}	CV_{DD}	V_{SS}				DV_{DD33}	V_{SS}	AEA0/ CFGGP0	AEA1/ CFGGP1	AEA6/ PCI66	AEA5/ MCBSP1 _EN	RSV20	U
T	V_{SS}	CV_{DD}	V_{SS}	CV_{DD}				V_{SS}	DV_{DD33}	AEA11	AEA2/ CFGGP2	AEA3	AEA4/ SYSCLKOUT _EN	PLLV1	T
R	CV_{DD}	V_{SS}	CV_{DD}	V_{SS}				DV_{DD33}	V_{SS}	AEA14/ HPI_ WIDTH	$\overline{ASADS}$/ $\overline{ASRE}$	AEA13/ LENDIAN	AEA12/ UTOPIA_EN	$\overline{AHOLD}$	R
	16	17	18	19	20	21	22	23	24	25	26	27	28	29	

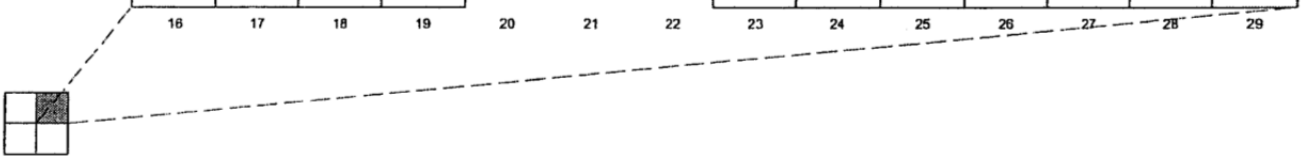
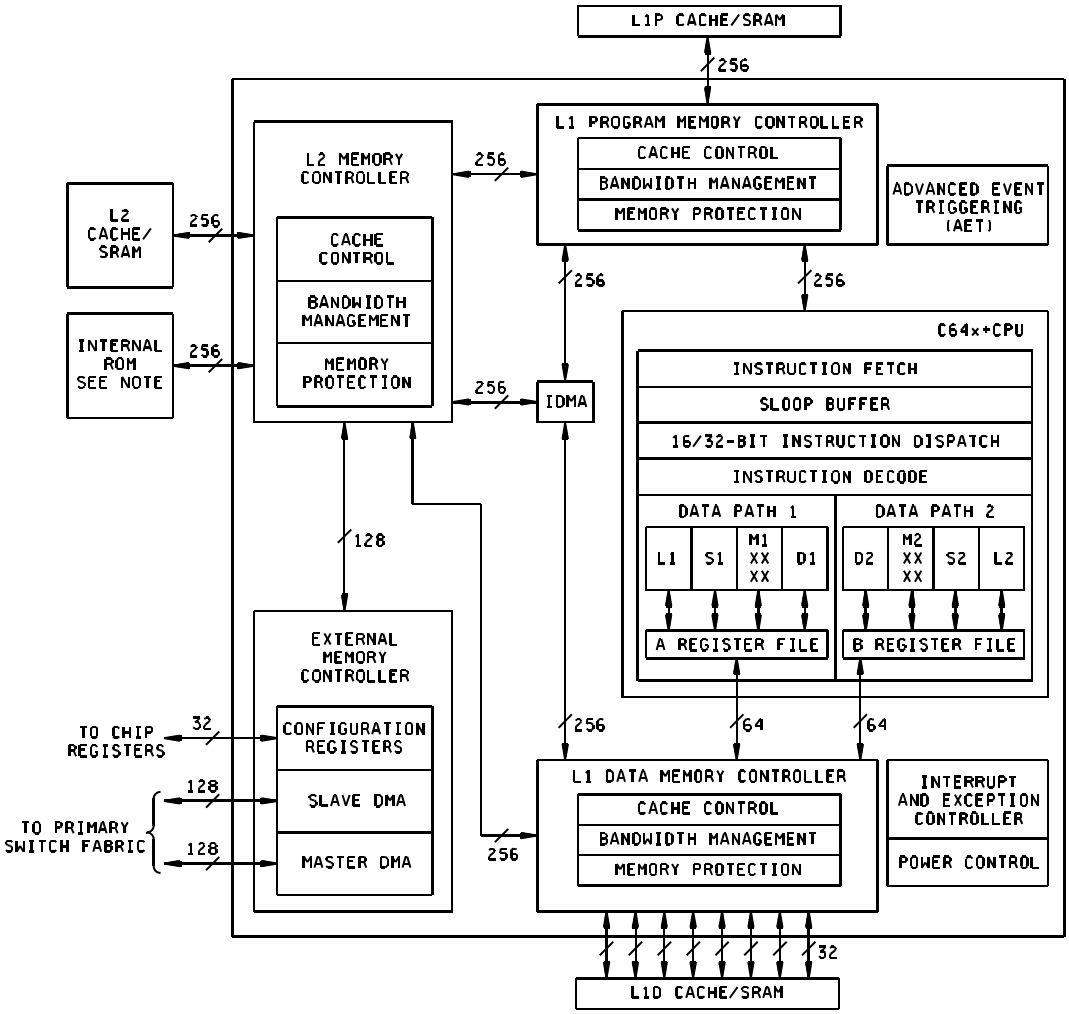
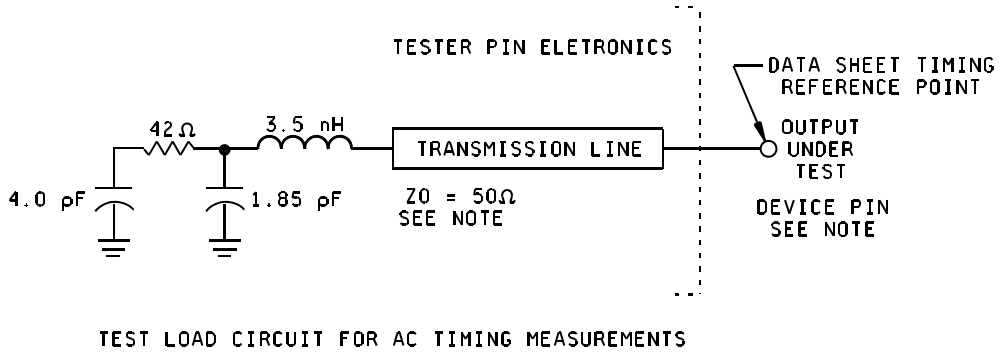


FIGURE 2. Terminal connections - Continued.



Notes:
1. McBSPs: Framing Chips – H.100, MVIP, SCSA, T1, E1; AC97 Devices; SPI Devices; Codecs.

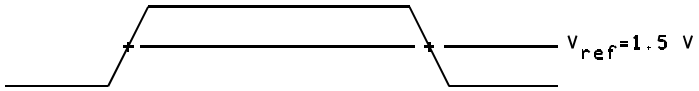
FIGURE 3. Block diagram - Continued.



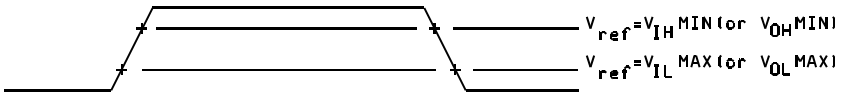
TEST LOAD CIRCUIT FOR AC TIMING MEASUREMENTS

Notes:

1. The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timings.
   Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond ($ V/ns) at the device pin.

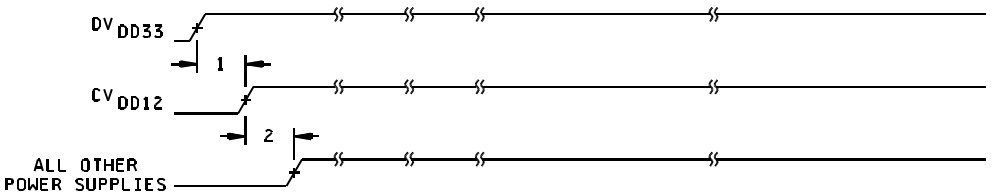


INPUT AND OUTPUT VOLTAGE REFERENCE LEVELS FOR AC TIMING MEASUREMENTS



RISE AND FALL TRANSITION TIME VOLTAGE REFERENCE LEVELS

FIGURE 4. Test load circuit for AC timing measurements.



POWER-SUPPLY SEQUENCE

FIGURE 5. Timing waveforms.

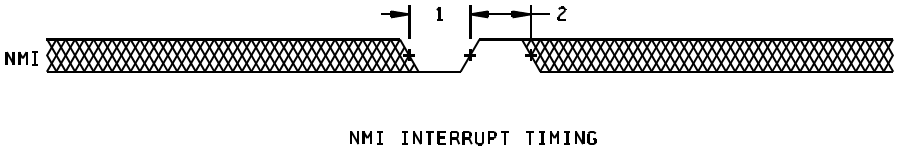
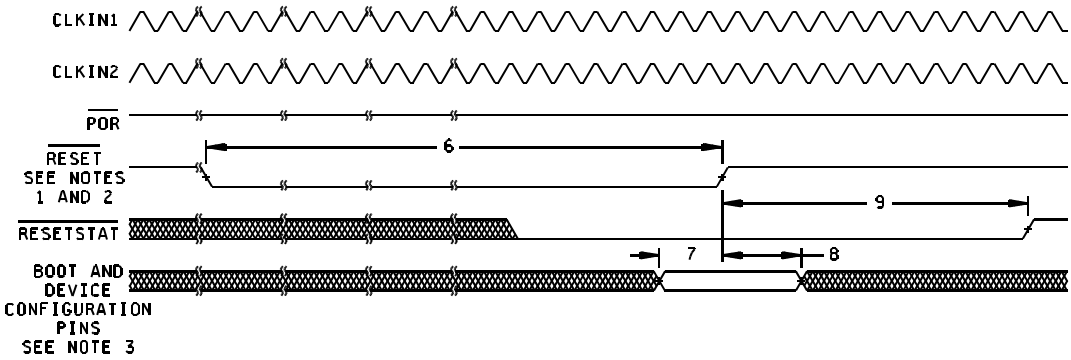


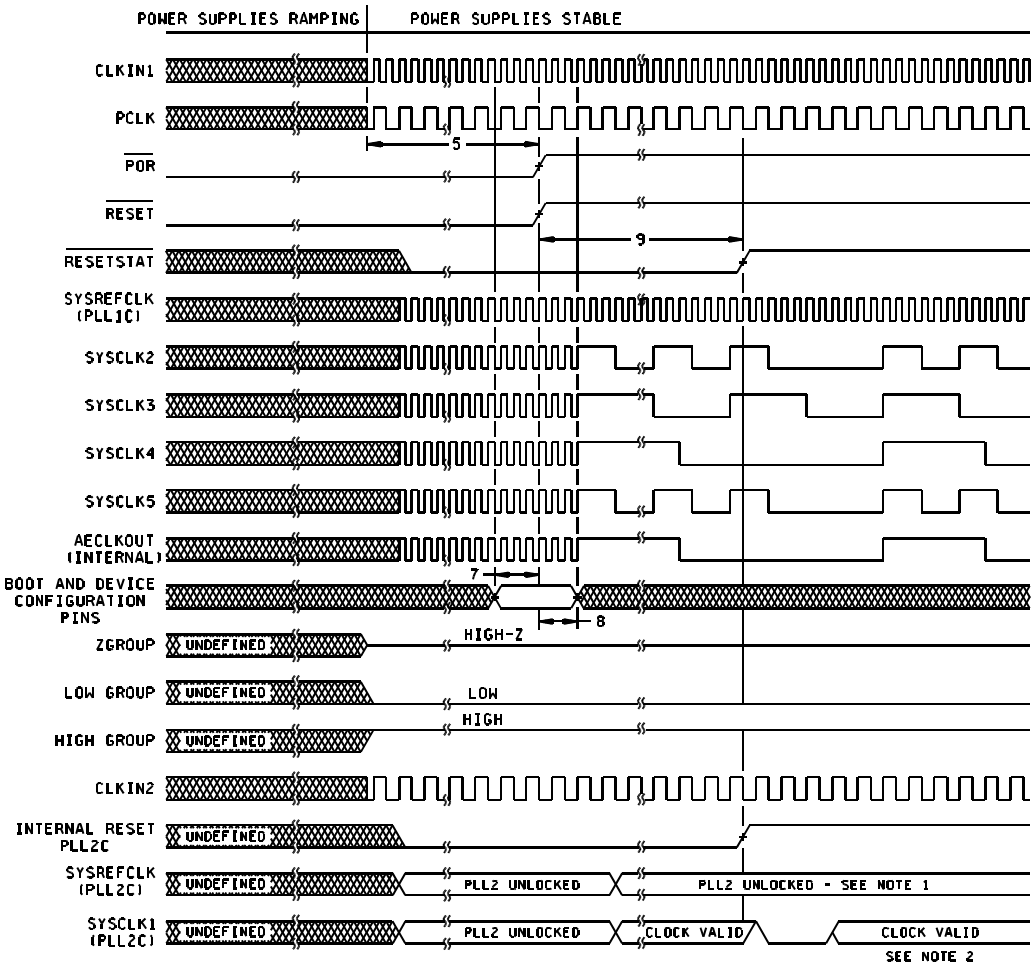
FIGURE 6. Timing waveforms.



Notes:

1. $\overline{\text{RESET}}$ should only be used after device has been powered up. For more details on the use of the $\overline{\text{RESET}}$ pin, see manufacturer data.
2. A reset signal internally during a Warm Reset. This internal reset signal ha s the same effect as the $\overline{\text{RESET}}$ pin during a Warm Reset.
3. Boot and device configurations Inputs (during reset) include: AEA[19:0], ABA[1:0], and PCI_EN.

FIGURE 7. Timing waveforms.

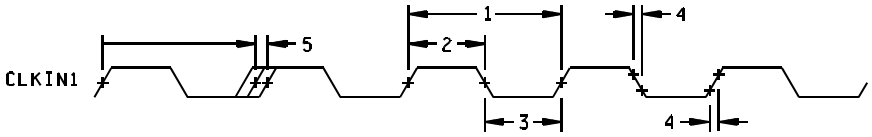


POWER-UP TIMING

Notes:

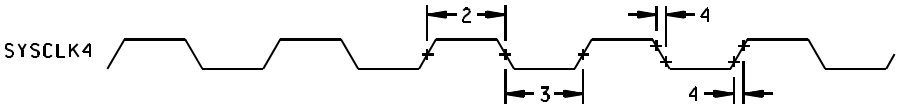
1. SYSREFCLK of the PLL2 controller runs at CLKIN2 x10.
2. SYSCLK1 of PLL2 controller runs at SYSREFCLK/2 (default).
3. Power supplies, CLKIN1, CLKIN2 (if used), and PCLK (if used) must be stable before the start of $t_{w(POR)}$.
4. Do not tie the $\overline{\text{RESET}}$ and $\overline{\text{POR}}$ pins together.
5. The $\overline{\text{RESET}}$ pin can be brought high after $\overline{\text{POR}}$ pin has been brought high. In this case, the $\overline{\text{RESET}}$ pin must be held low for a minimum of $t_{w(RESET)}$ after the $\overline{\text{POR}}$ pin has been brought high.

FIGURE 8. Timing waveforms.



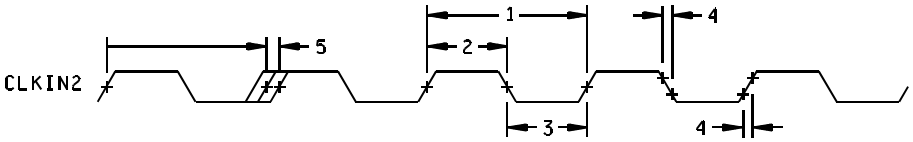
CLKIN1 TIMING

FIGURE 9. Timing waveforms.



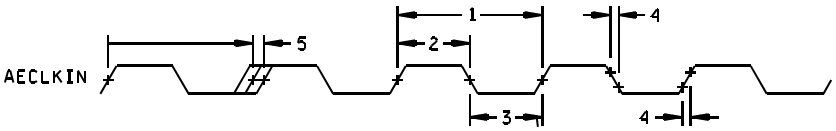
SYSCLK4 TIMING

FIGURE 10. Timing waveforms.



CLKIN2 TIMING

FIGURE 11. Timing waveforms.



AECLKIN TIMING FOR EMIFA

FIGURE 12. Timing waveforms.

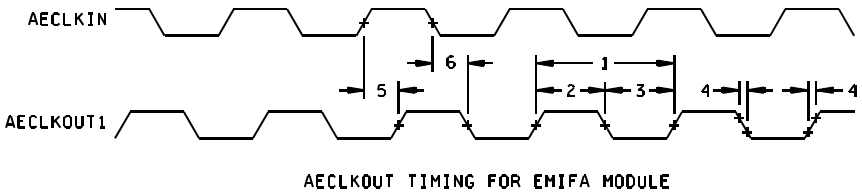
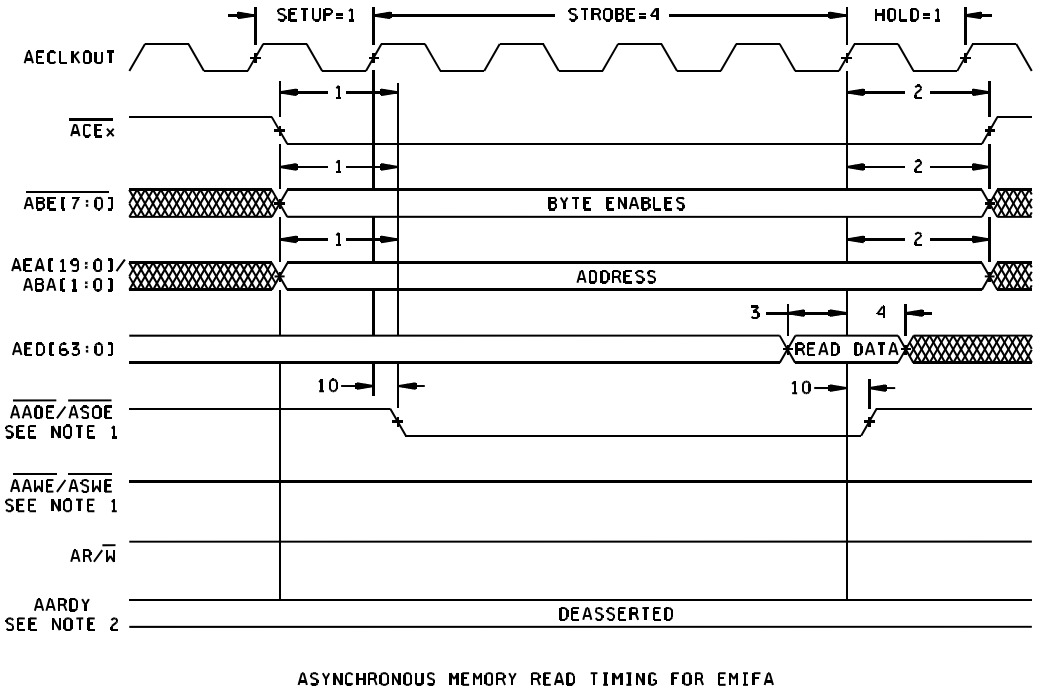


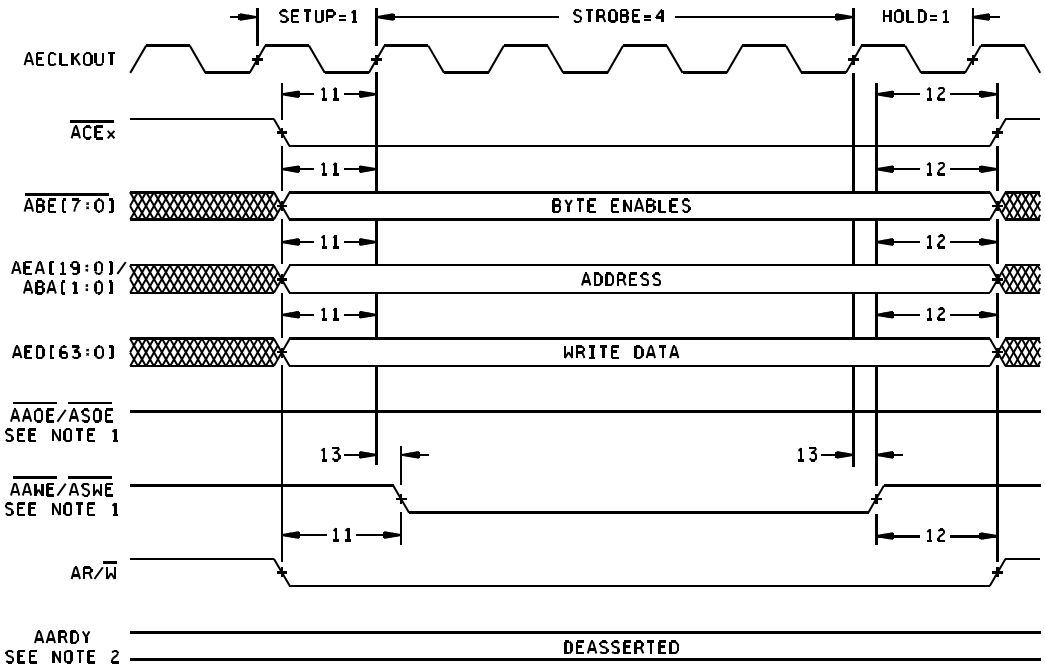
FIGURE 13. Timing waveforms.



Notes:

1. $\overline{\text{AAOE}}$ / $\overline{\text{ASOE}}$ and $\overline{\text{AAWE}}$ / $\overline{\text{ASWE}}$ operate as $\overline{\text{AAOE}}$ (identified under select signals) and $\overline{\text{AAWE}}$, respectively, during asynchronous memory accesses.
2. Polarity of the AARDY signal is programmable through the AP field of the EMIFA Async Wait Cycle Configuration register (AWCC).

FIGURE 14. Timing waveforms.

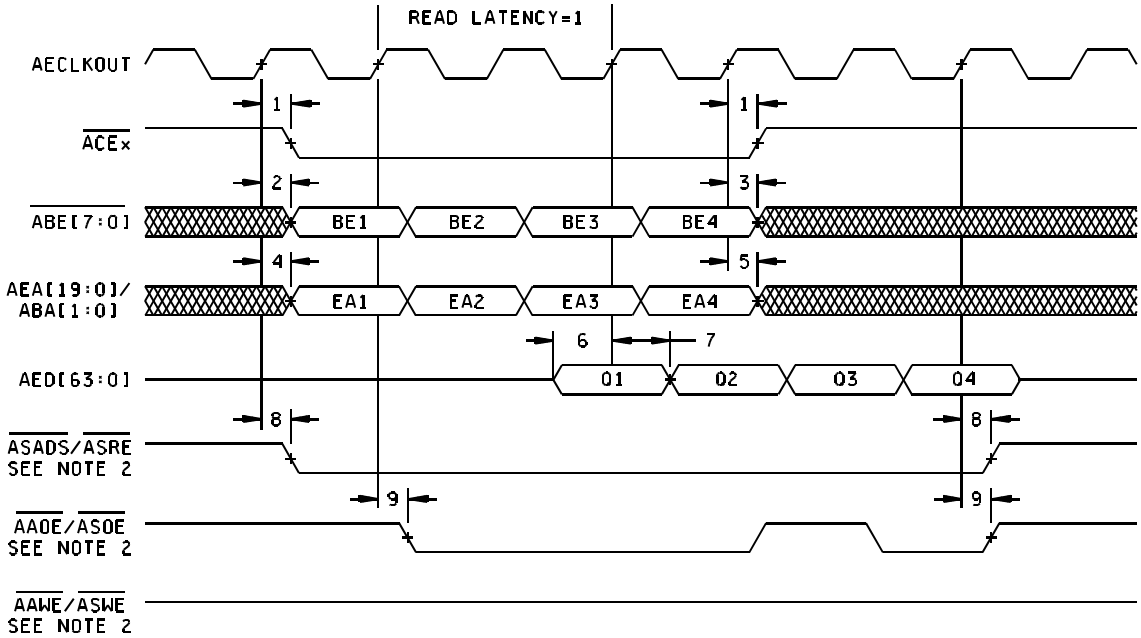


ASYNCHRONOUS MEMORY WRITE TIMING FOR EMIFA

Notes:

1. $\overline{\text{AAOE}}$ / $\overline{\text{ASOE}}$ and $\overline{\text{AAWE}}$ / $\overline{\text{ASWE}}$ operate as $\overline{\text{AAOE}}$ (identified under select signals) and $\overline{\text{AAWE}}$, respectively, during asynchronous memory accesses.
2. Polarity of the AARDY signal is programmable through the AP field of the EMIFA Async Wait Cycle Configuration register (AWCC).

FIGURE 15. Timing waveforms.

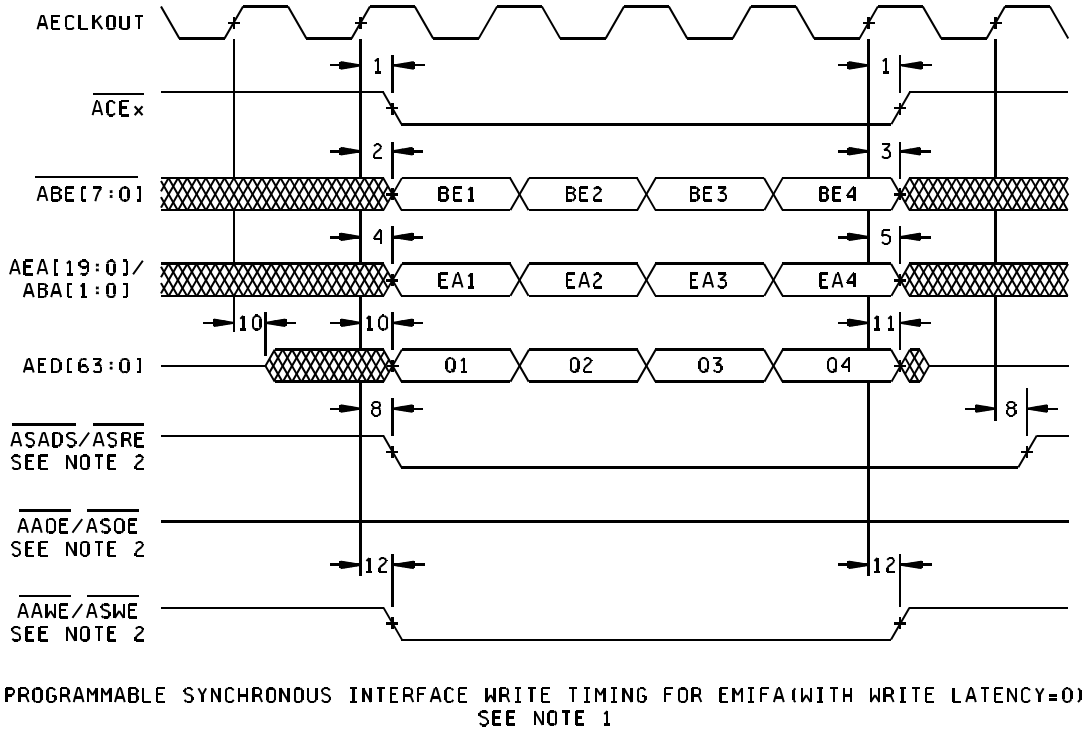


PROGRAMMABLE SYNCHRONOUS INTERFACE READ TIMING FOR EMIFA(WITH READ LATENCY=2)
SEE NOTE 1

Notes:

1. The following parameters are programmable via the EMIFA Chip Select n Configuration Register (CESECn):
   - Read latency(R_LTNCY): 1-, 2-, or 3-cycle read latency.
   - Write latency (W-LTNCY): 0-, 1-, 2-, or 3-cycle write latency
   - $\overline{\text{ACEx}}$ assertion length (CE_EXT): For standard SBSRAM or ZBT SRAM interface, $\overline{\text{ACEx}}$ goes inactive after the final command has been issue (CE_EXT = 0). For synchronous FIFO interface, $\overline{\text{ACEx}}$ is active when $\overline{\text{ASOE}}$ is active (CE_EXT = 1).
   - Function of $\overline{\text{ASADS}}$ / $\overline{\text{ASRE}}$ (R_ENABLE): For standard SBSRAM or ZBT SRAM interface, $\overline{\text{ASADS}}$ / $\overline{\text{ASRE}}$ act as $\overline{\text{ASADS}}$ with deselect cycle (R_ENABLE = 0). For FIFO interface $\overline{\text{ASADS}}$ / $\overline{\text{ASRE}}$ acts as $\overline{\text{SRE}}$ with NO deselect cycles (R_ENABLE = 1).
   - In this figure R_LTNCY = 2, CE_EXT = 0, R_ENABLE = 0 and SSEL = 1.
2. $\overline{\text{AAOE}}$ / $\overline{\text{ASOE}}$ and $\overline{\text{AAWE}}$ / $\overline{\text{ASWE}}$ operate as $\overline{\text{ASOE}}$, and $\overline{\text{ASWE}}$, respectively, during programmable synchronous interface accesses.

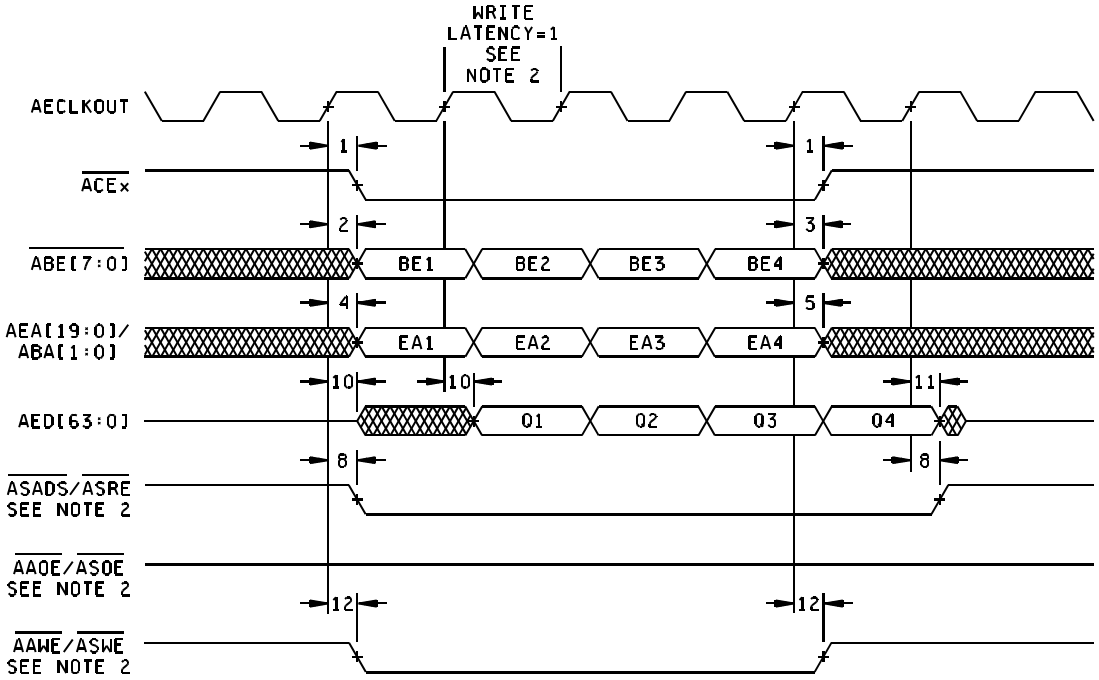
FIGURE 16. Timing waveforms.



Notes:

1. The following parameters are programmable via the EMIFA Chip Select n Configuration Register (CESECn):
   - Read latency(R_LTNCY): 1-, 2-, or 3-cycle read latency.
   - Write latency (W-LTNCY): 0-, 1-, 2-, or 3-cycle write latency
   - $\overline{\text{ACEx}}$ assertion length (CE_EXT): For standard SBSRAM or ZBT SRAM interface, $\overline{\text{ACEx}}$ goes inactive after the final command has been issue (CE_EXT = 0). For synchronous FIFO interface, $\overline{\text{ACEx}}$ is active when $\overline{\text{ASOE}}$ is active (CE_EXT = 1).
   - Function of $\overline{\text{ASADS}}$ / $\overline{\text{ASRE}}$ (R_ENABLE): For standard SBSRAM or ZBT SRAM interface, $\overline{\text{ASADS}}$ / $\overline{\text{ASRE}}$ act as $\overline{\text{ASADS}}$ with deselect cycle (R_ENABLE = 0). For FIFO interface $\overline{\text{ASADS}}$ / $\overline{\text{ASRE}}$ acts as $\overline{\text{SRE}}$ with NO deselect cycles (R_ENABLE = 1).
   - In this figure W_LTNCY = 0, CE_EXT = 0, R_ENABLE = 0 and SSEL = 1.
2. $\overline{\text{AAOE}}$ / $\overline{\text{ASOE}}$ and $\overline{\text{AAWE}}$ / $\overline{\text{ASWE}}$ operate as $\overline{\text{ASOE}}$, and $\overline{\text{ASWE}}$, respectively, during programmable synchronous interface accesses.

FIGURE 17. Timing waveforms.

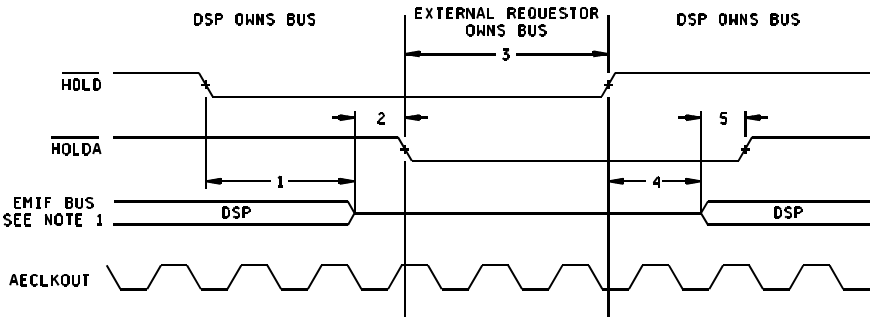


PROGRAMMABLE SYNCHRONOUS INTERFACE WRITE TIMING FOR EMIFA(WITH WRITE LATENCY=1)
SEE NOTE 1

Notes:

1. The following parameters are programmable via the EMIFA Chip Select n Configuration Register (CESECn):
   - Read latency(R_LTNCY): 1-, 2-, or 3-cycle read latency.
   - Write latency (W-LTNCY): 0-, 1-, 2-, or 3-cycle write latency
   - $\overline{\text{ACEx}}$ assertion length (CE_EXT): For standard SBSRAM or ZBT SRAM interface, $\overline{\text{ACEx}}$ goes inactive after the final command has been issue (CE_EXT = 0). For synchronous FIFO interface, $\overline{\text{ACEx}}$ is active when $\overline{\text{ASOE}}$ is active (CE_EXT = 1).
   - Function of $\overline{\text{ASADS}}$ / $\overline{\text{ASRE}}$ (R_ENABLE): For standard SBSRAM or ZBT SRAM interface, $\overline{\text{ASADS}}$ / $\overline{\text{ASRE}}$ act as $\overline{\text{ASADS}}$ with deselect cycle (R_ENABLE = 0). For FIFO interface $\overline{\text{ASADS}}$ / $\overline{\text{ASRE}}$ acts as $\overline{\text{SRE}}$ with NO deselect cycles (R_ENABLE = 1).
   - In this figure W_LTNCY = 1, CE_EXT = 0, R_ENABLE = 0 and SSEL = 1.
2. $\overline{\text{AAOE}}$ / $\overline{\text{ASOE}}$ and $\overline{\text{AAWE}}$ / $\overline{\text{ASWE}}$ operate as $\overline{\text{ASOE}}$, and $\overline{\text{ASWE}}$, respectively, during programmable synchronous interface accesses.

FIGURE 18. Timing waveforms.

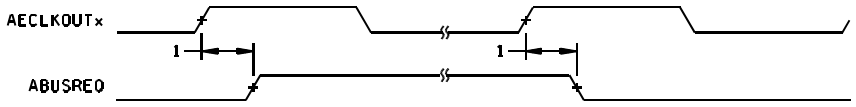


HOLD/HOLDA TIMING FOR EMIFA

Notes:

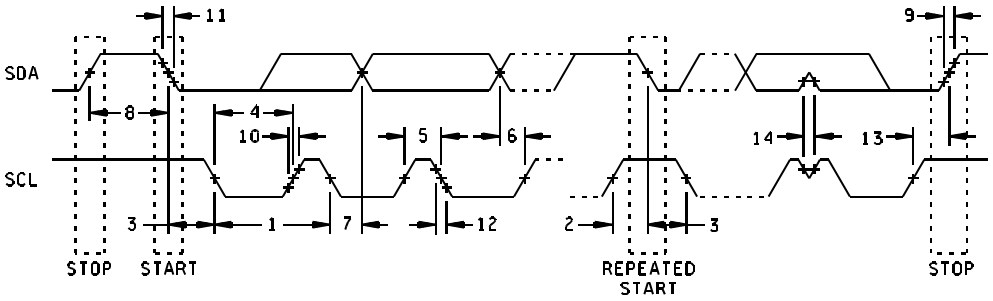
1. EMIFA Bus consists of: ACE[5 : 2] , ABE[7 : 0] , AED[63:0], AEA[19:0], ABA[1:0], AR/ W , ASADS / ASRE , AAOE / ASOE , and AAWE / ASWE .

FIGURE 19. Timing waveforms.



BUSREQ TIMING FOR EMIFA

FIGURE 20. Timing waveforms.



I2C RECEIVE TIMING

FIGURE 21. Timing waveforms.

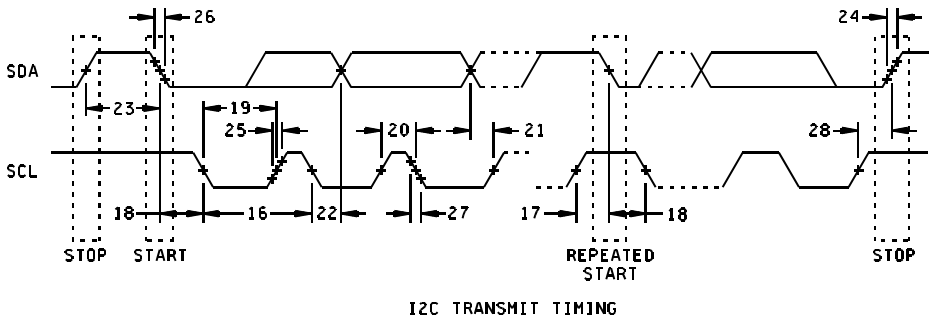
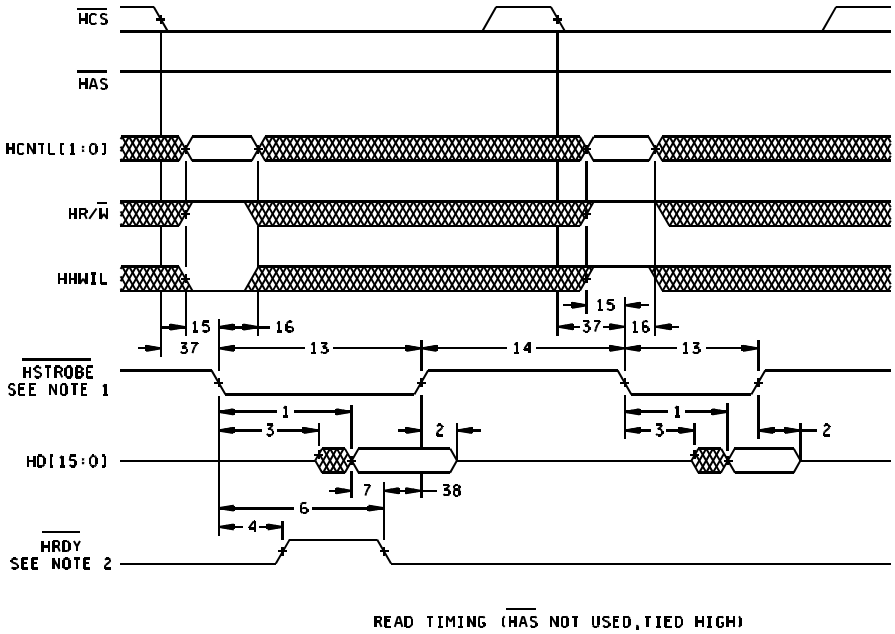


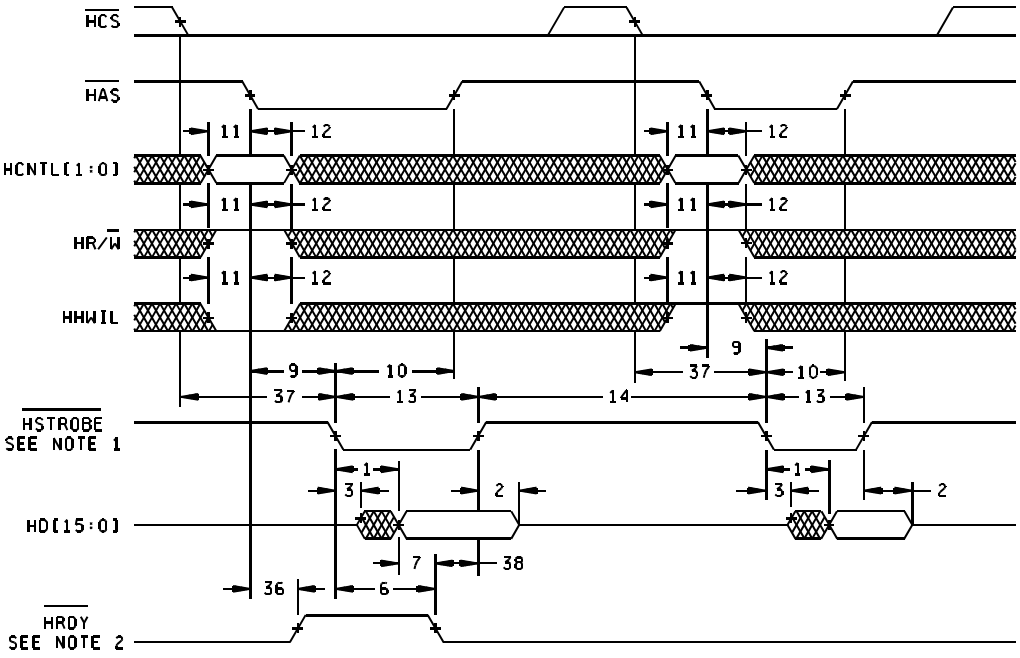
FIGURE 22. Timing waveforms.



Note:

1. HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT (HDS1 XOR HDS2)] OR HCS.
2. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on HRDY may or may not occur. For more detailed see manufacturer data.

FIGURE 23. Timing waveforms.

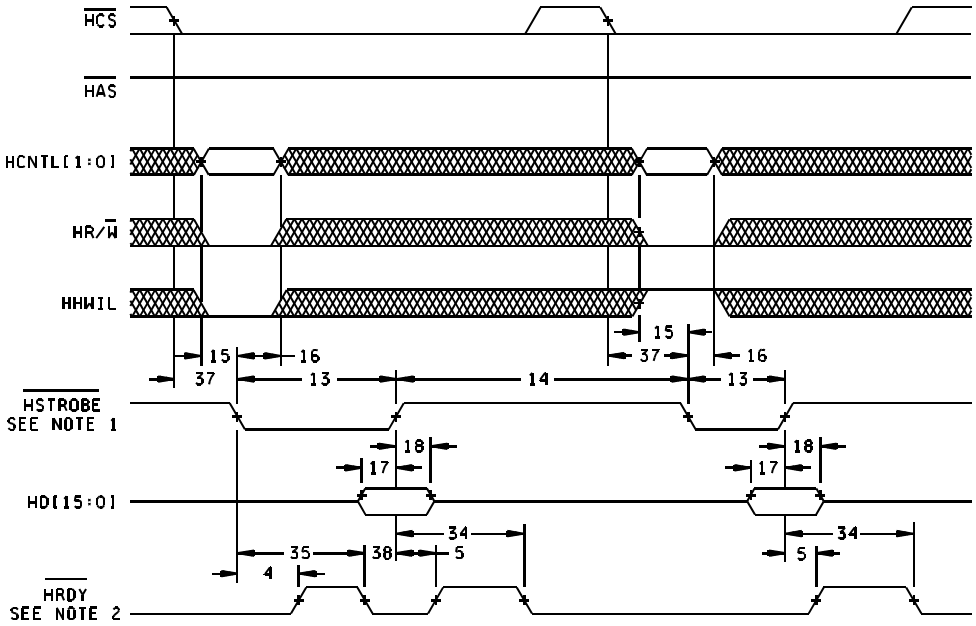


READ TIMING (HAS USED)

Note:

1. HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT (HDS1 XOR HDS2)] OR HCS.
2. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on HRDY may or may not occur. For more detailed see manufacturer data.

FIGURE 24. Timing waveforms.

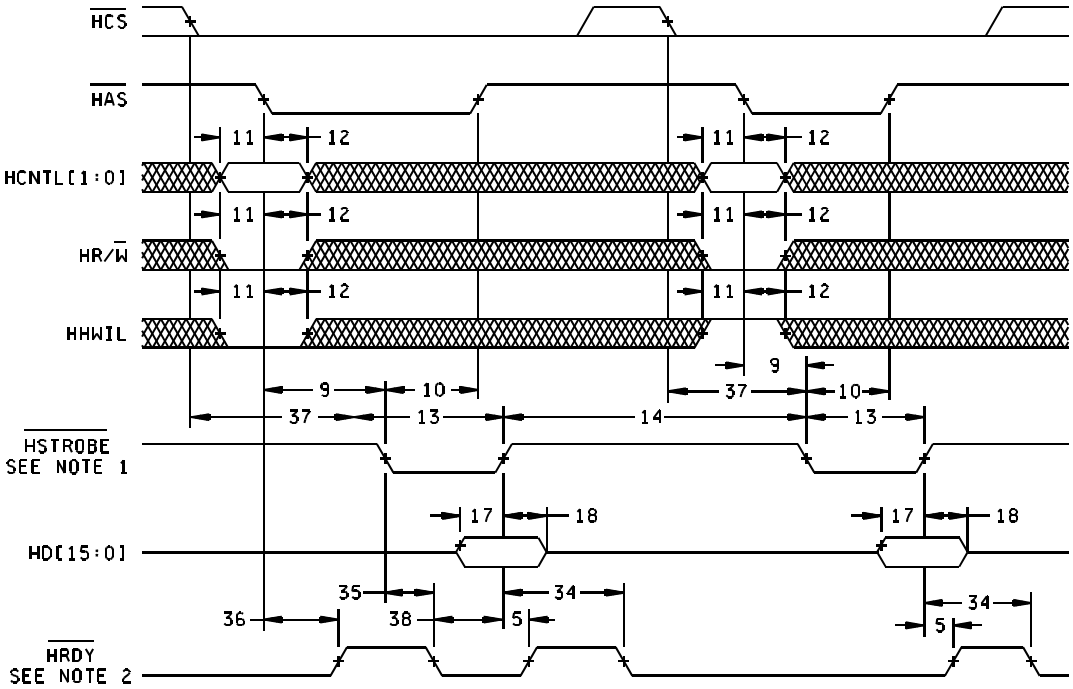


WRITE TIMING (HAS NOT USED,TIED HIGH)

Note:

1. HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT (HDS1 XOR HDS2)] OR HCS.
2. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on HRDY may or may not occur. For more detailed see manufacturer data.

FIGURE 25. Timing waveforms.

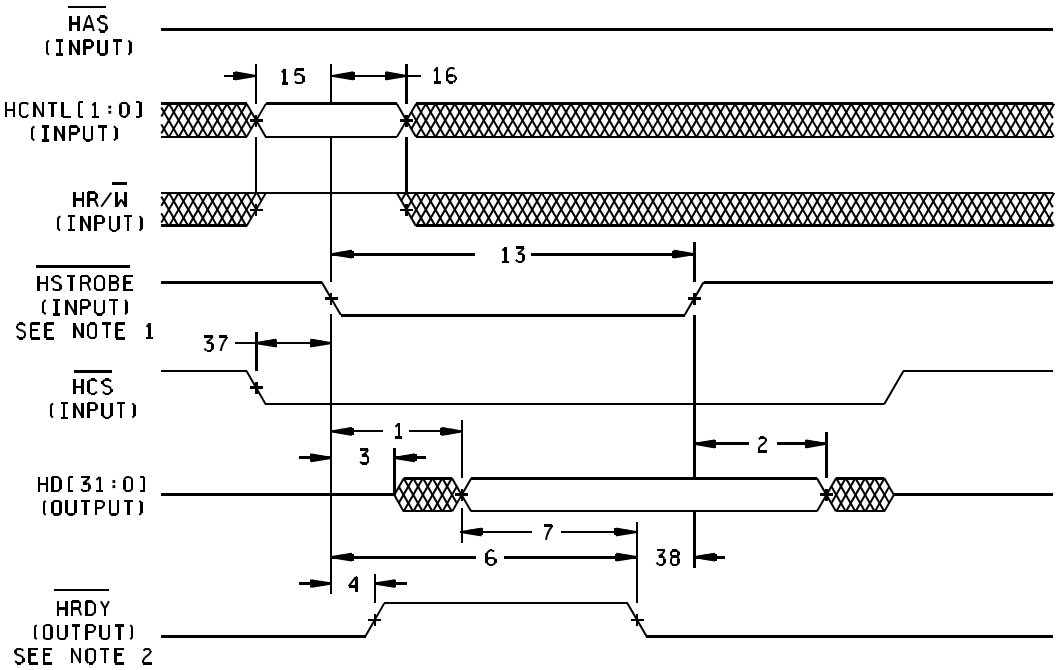


WRITE TIMING (HAS USED)

Note:

1. HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT (HDS1 XOR HDS2)] OR HCS.
2. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on HRDY may or may not occur. For more detailed see manufacturer data.

FIGURE 26. Timing waveforms.

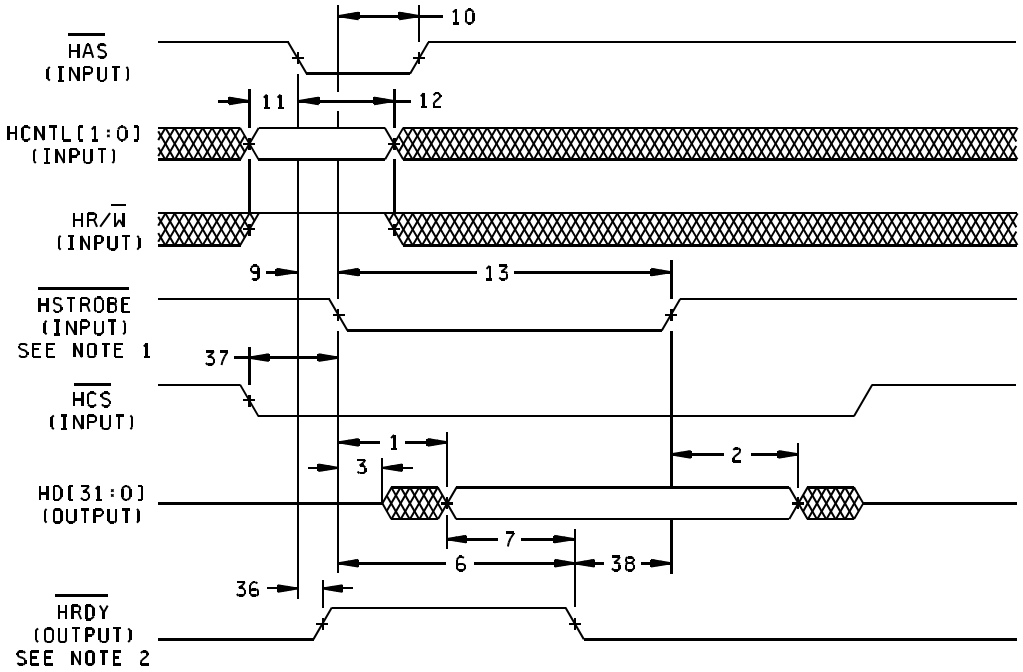


HPI32 READ TIMING (HAS NOT USED,TIED HIGH)

Note:

1. HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT (HDS1 XOR HDS2)] OR HCS.
2. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on HRDY may or may not occur. For more detailed see manufacturer data.
3. The timing $t_{w(HSTBH)}$, HSTROBE high pulse duration, must be met between consecutive HPI accesses in HPI32 mode.

FIGURE 27. Timing waveforms.

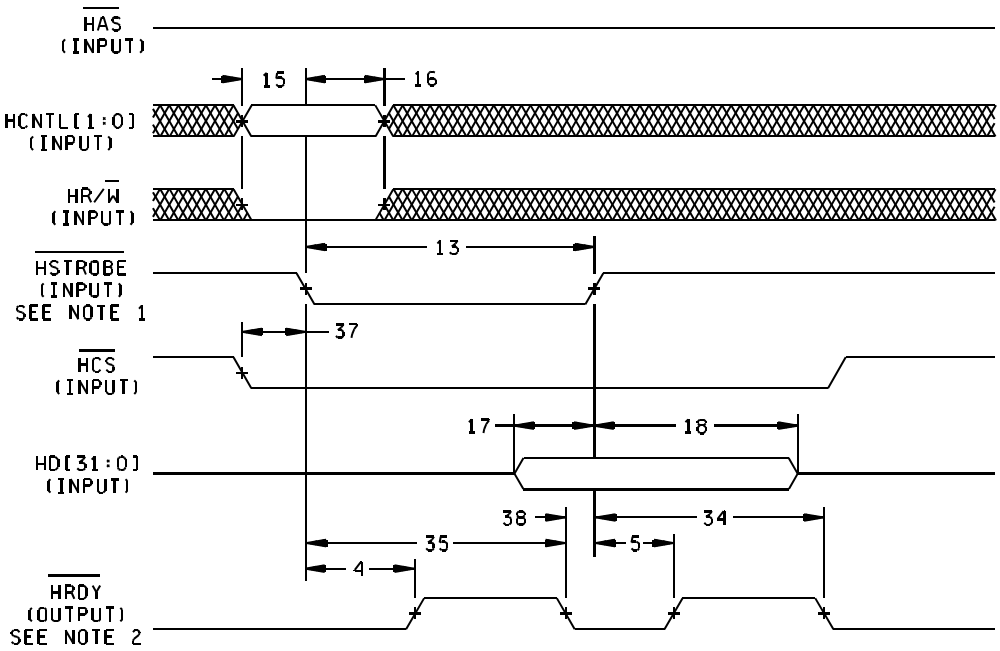


HPI32 READ TIMING ($\overline{\text{HAS}}$ USED)

Note:

1. $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: [NOT ($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{HCS}}$.
2. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on $\overline{\text{HRDY}}$ may or may not occur. For more detailed see manufacturer data.
3. The timing $t_{w(HSTBH)}$, $\overline{\text{HSTROBE}}$ high pulse duration, must be met between consecutive HPI accesses in HPI32 mode.

FIGURE 28. Timing waveforms.

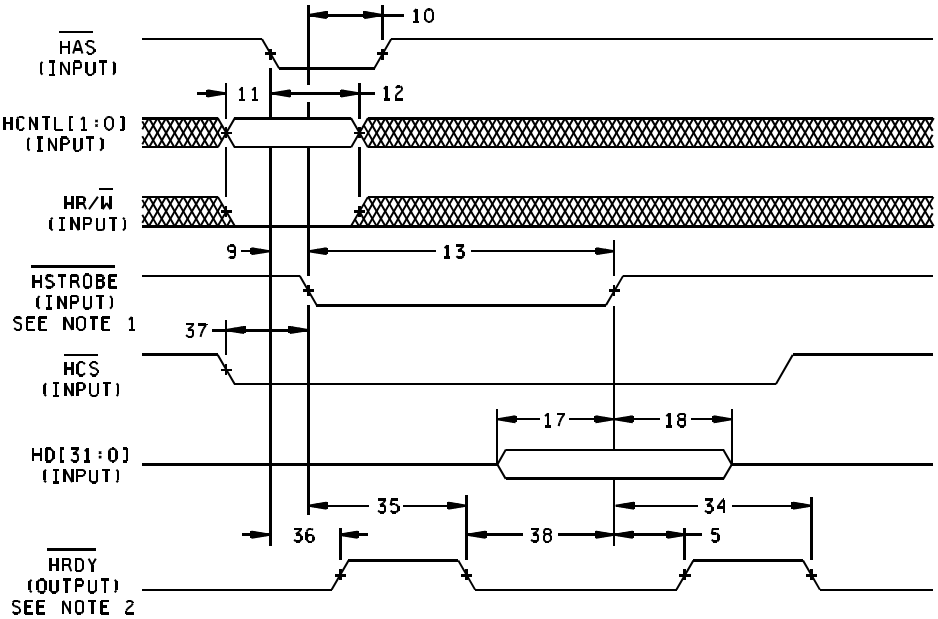


HPI32 WRITE TIMING ($\overline{\text{HAS}}$ NOT USED,TIED HIGH)

Note:

1. $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: [NOT ($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{HCS}}$.
2. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on $\overline{\text{HRDY}}$ may or may not occur. For more detailed see manufacturer data.
3. The timing $t_{w(HSTBH)}$, $\overline{\text{HSTROBE}}$ high pulse duration, must be met between consecutive HPI accesses in HPI32 mode.

FIGURE 29. Timing waveforms.

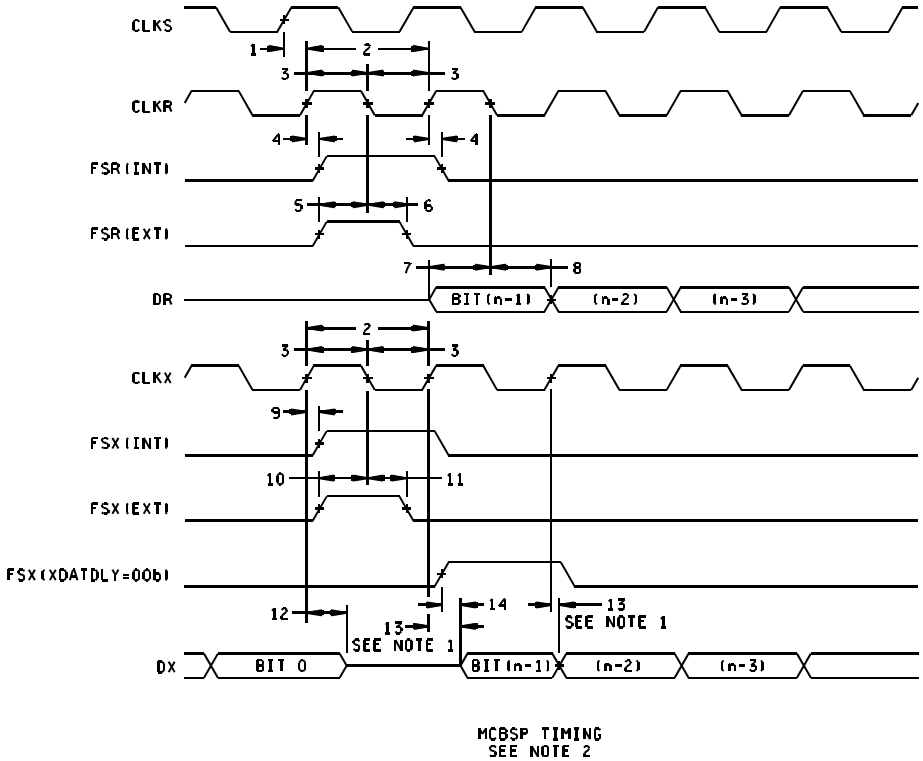


HPI32 WRITE TIMING (HAS USED)

Note:

1. HSTROBE refers to the following logical operation on HCS, HDS1, and HDS2: [NOT (HDS1 XOR HDS2)] OR HCS.
2. Depending on the type of write or read operation (HPID without auto-incrementing; HPIA, HPIC, or HPID with auto-incrementing) and the state of the FIFO, transitions on HRDY may or may not occur. For more detailed see manufacturer data.
3. The timing $t_{w(HSTBH)}$, HSTROBE high pulse duration, must be met between consecutive HPI accesses in HPI32 mode.

FIGURE 30. Timing waveforms.



Note:
1. Parameter No. 13 applies to the first data bit only when XDATDLY ≠ 0.
2. The CLKS signal is shared by both McBSP0 and McBSP1 on this device.

FIGURE 31. Timing waveforms.

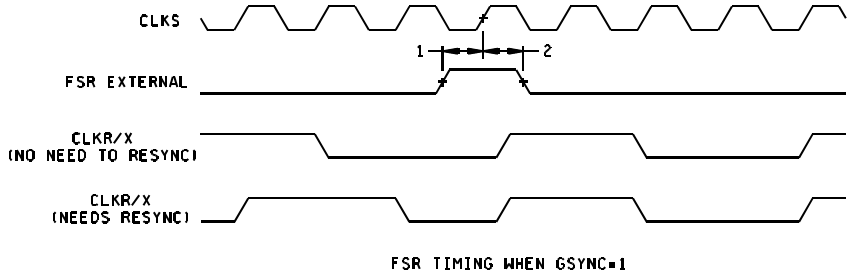


FIGURE 32. Timing waveforms.

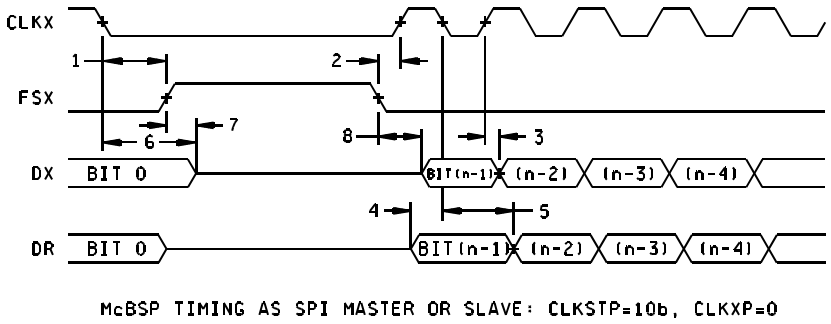


FIGURE 33. Timing waveforms.

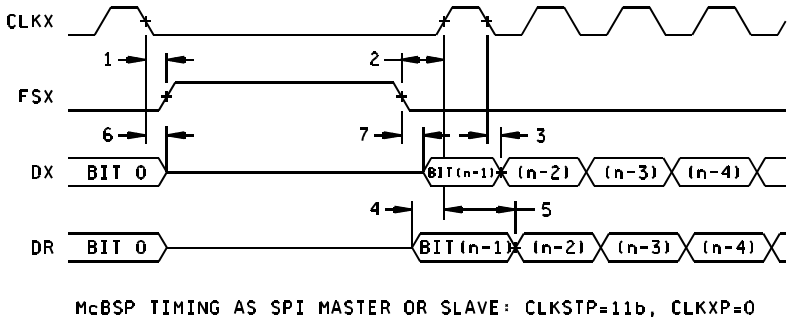


FIGURE 34. Timing waveforms.

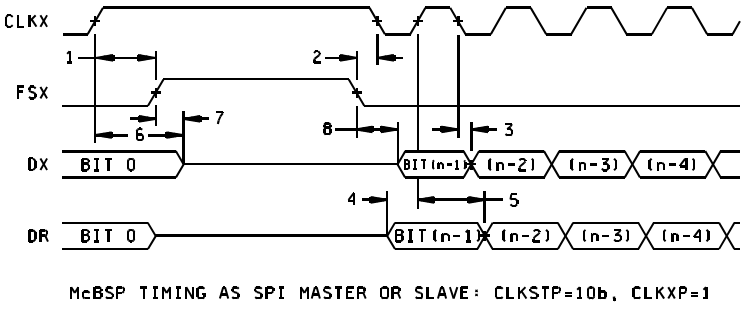


FIGURE 35. Timing waveforms.

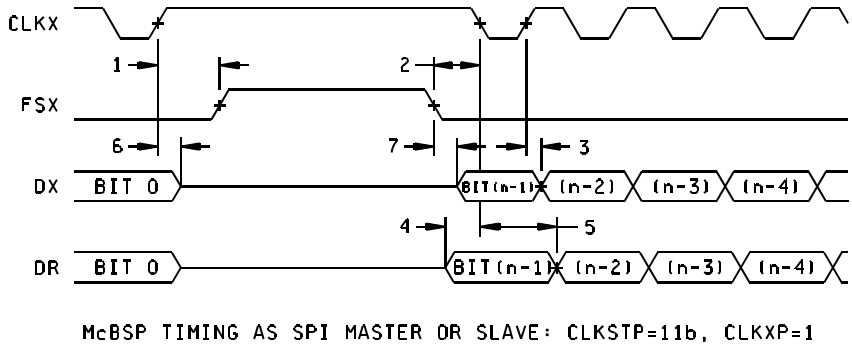


FIGURE 36. Timing waveforms.

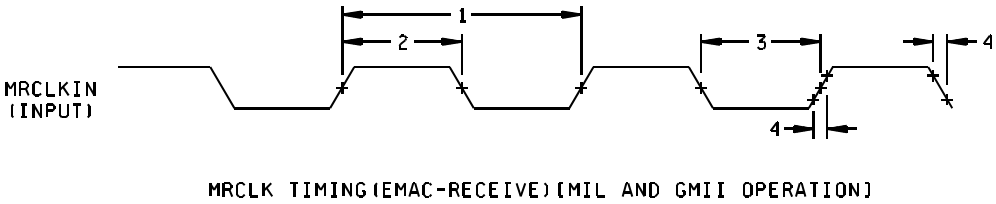


FIGURE 37. Timing waveforms.

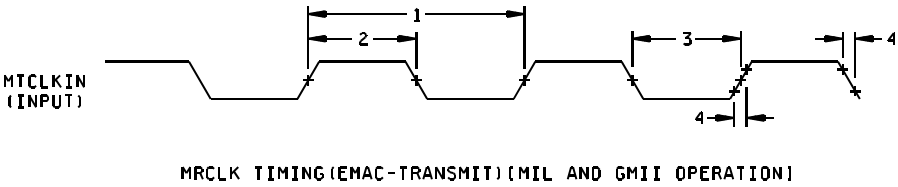


FIGURE 38. Timing waveforms.

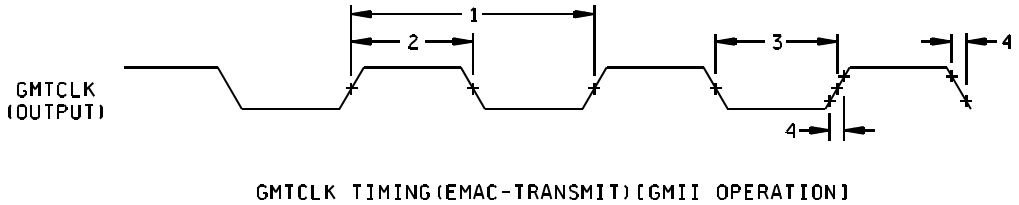


FIGURE 39. Timing waveforms.

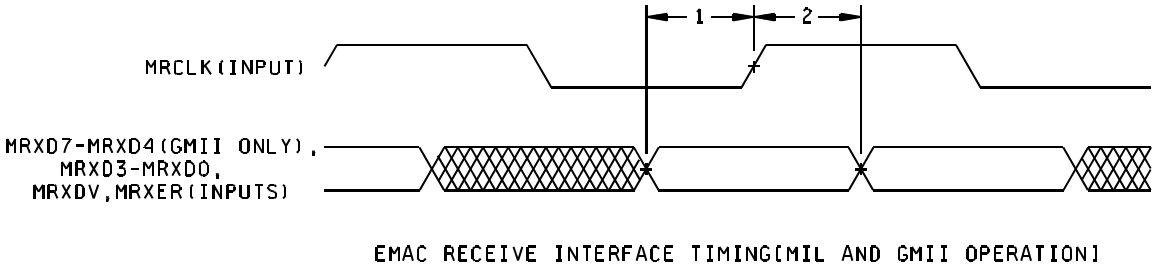


FIGURE 40. Timing waveforms.

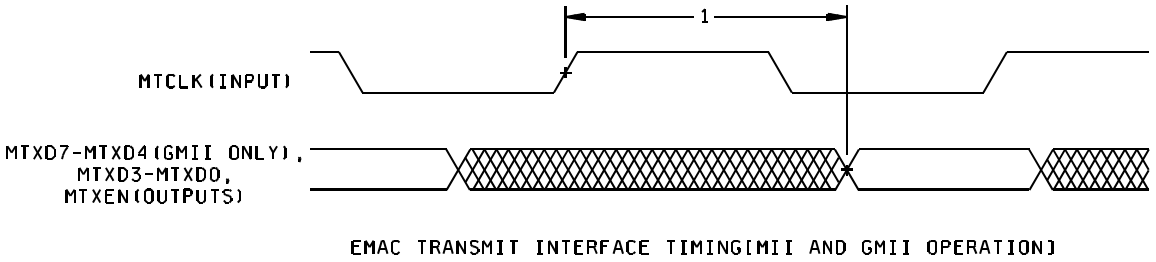


FIGURE 41. Timing waveforms.

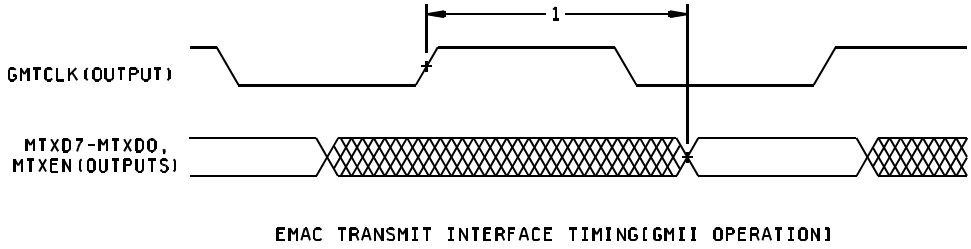


FIGURE 42. Timing waveforms.

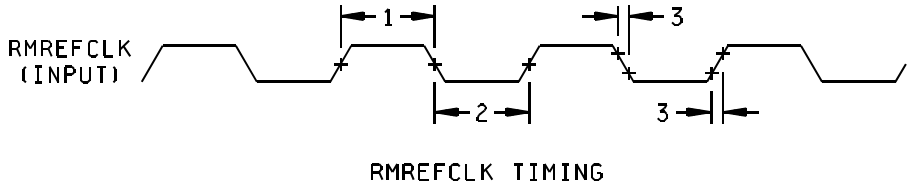


FIGURE 43. Timing waveforms.

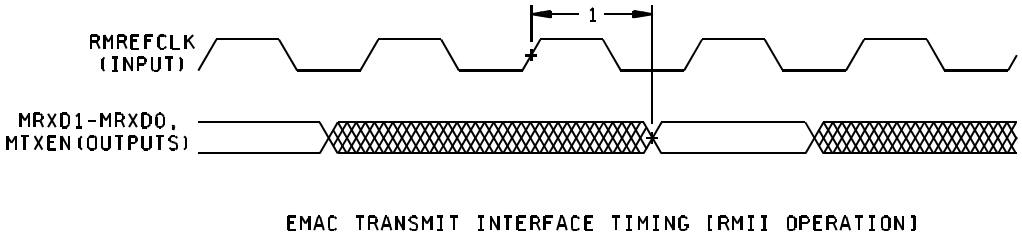
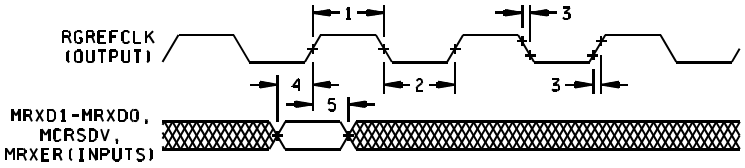
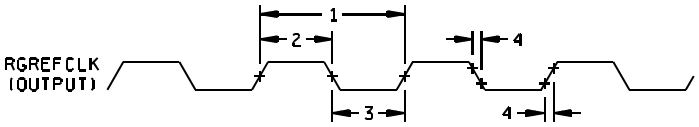


FIGURE 44. Timing waveforms.



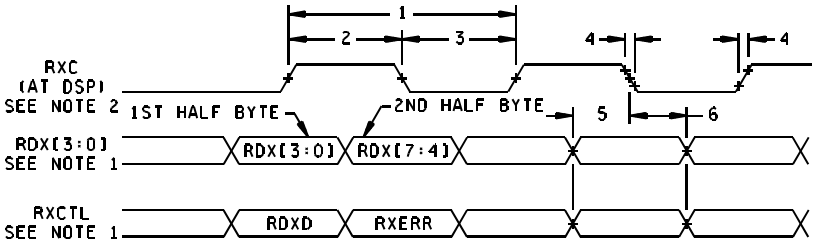
EMAC RECEIVE INTERFACE TIMING(RMII OPERATION)

FIGURE 45. Timing waveforms.



RGREFCLK TIMING

FIGURE 46. Timing waveforms.

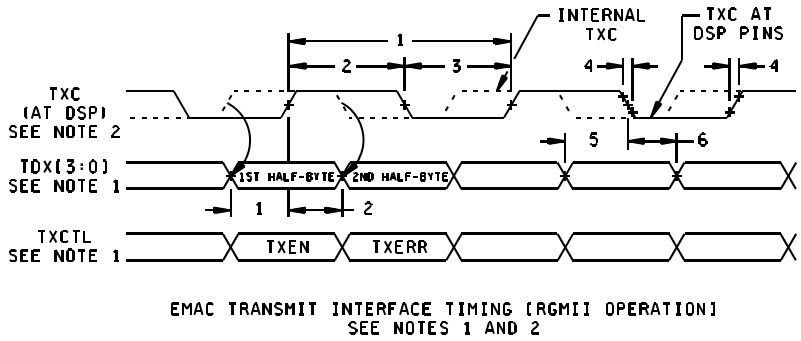


EMAC RECEIVE INTERFACE TIMING (RGMII OPERATION)
SEE NOTES 1 AND 2

Note:

1. Data and control information is received using both edges of the clocks. RXD[3:0] carries data bits 3-0 on the rising edge of RXC and data bits 7-4 on the falling edge of RXC. Similarly, RXCTL carries RXDV on rising edge of RXC and RXERR on falling edge.
2. RXC must be externally delayed relative to the data and control pins.

FIGURE 47. Timing waveforms.



Note:

1. Data and control information is transmitted using both edges of the clocks. TXD[3:0] carries data bits 3-0 on the rising edge of TXC and data bits 7-4 on the falling edge of TXC. Similarly, TX_CTL carries TXEN on rising edge of TXC and TXERR on falling edge.
2. RTC delayed internally before being driven to the TXC pin..

FIGURE 48. Timing waveforms.

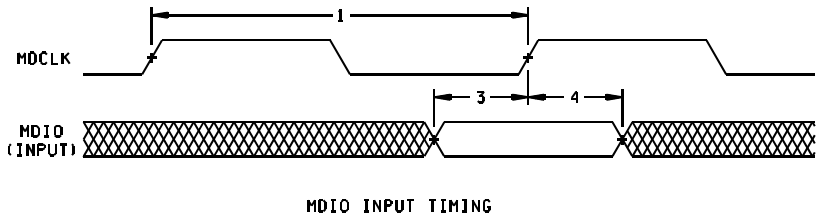


FIGURE 49. Timing waveforms.

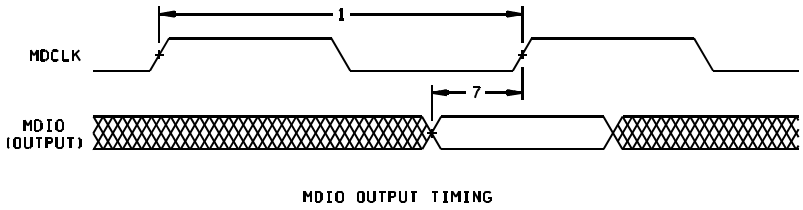


FIGURE 50. Timing waveforms.

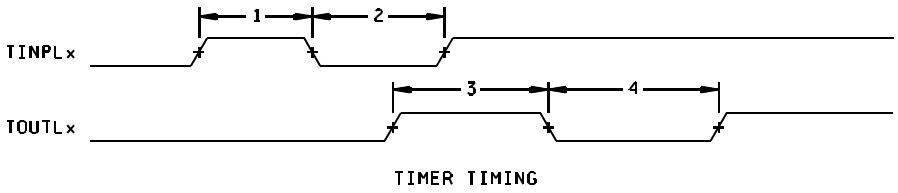


FIGURE 51. Timing waveforms.

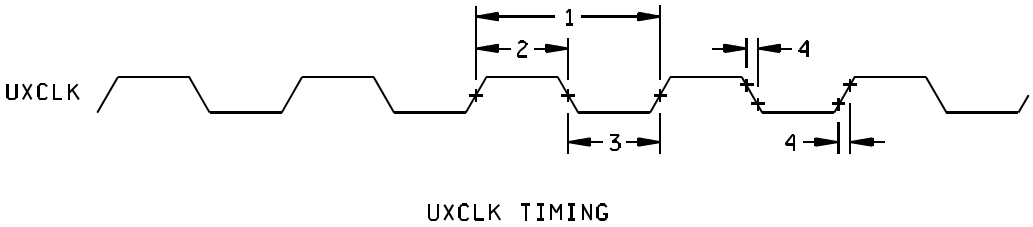


FIGURE 52. Timing waveforms.

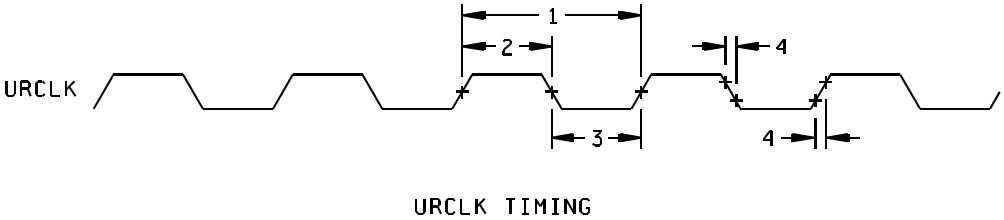
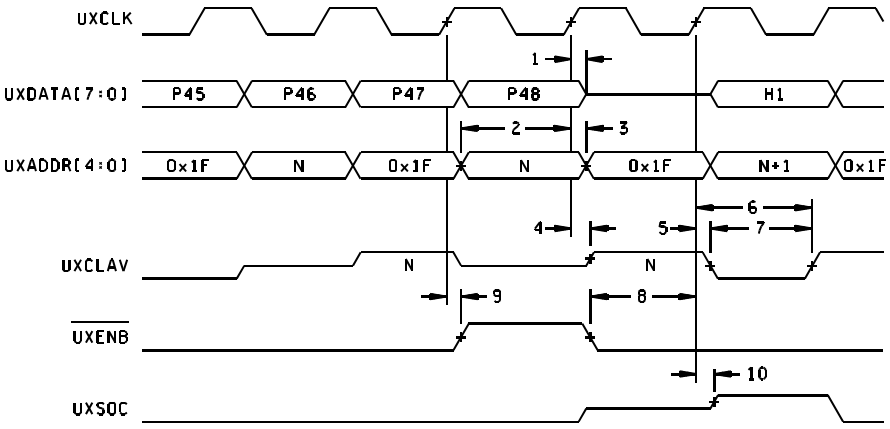


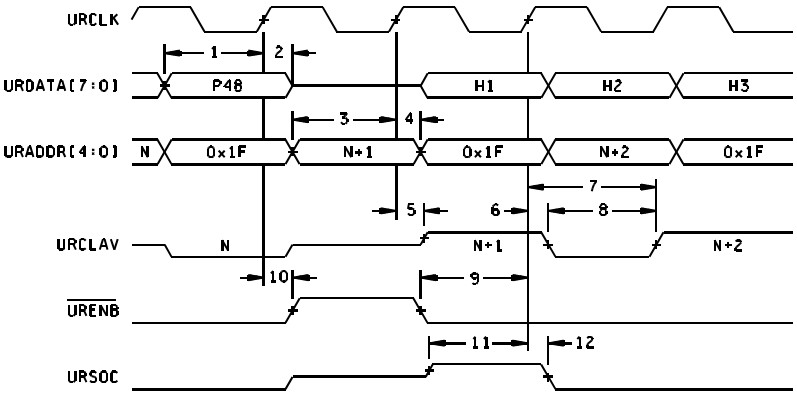
FIGURE 53. Timing waveforms.



UTOPIA SLAVE TRANSMIT TIMING
SEE NOTE

Note:
1. The UTOPIA slave module has signals that are middle-level signals indicating a high-impedance state (i.e., the UXCLAV and UXSOC signals).

FIGURE 54. Timing waveforms.



UTOPIA SLAVE RECEIVE TIMING
SEE NOTE

Note:
1. The UTOPIA slave module has signals that are middle-level signals indicating a high-impedance state (i.e., the URCLAV and URSOC signals).

FIGURE 55. Timing waveforms.

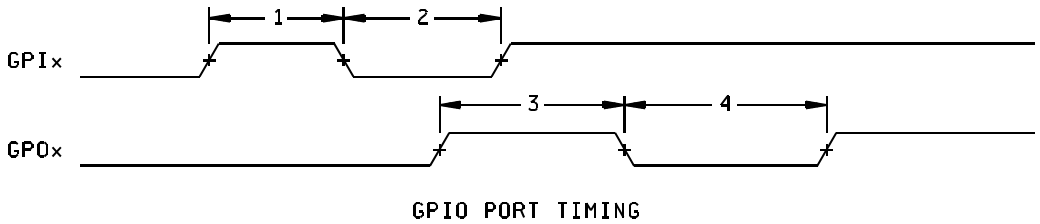


FIGURE 56. Timing waveforms.

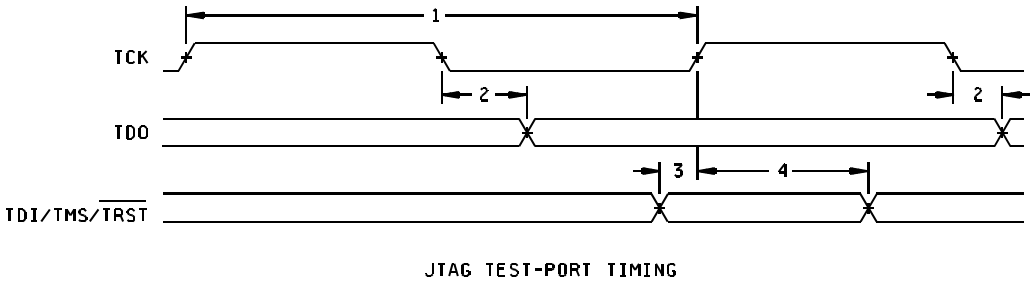


FIGURE 57. Timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/07649-01XA	01295	SM320C6455BGTZEP
V62/07649-02XA	01295	SM320C6455BGTZSEP
V62/07649-03XA	2/	SM320C6455BGTZAEP
V62/07649-04XA	2/	SM320C6455BGTZ7EP
V62/07649-05XA	2/	SM320C6455BGTZ8EP
V62/07649-06XA	2/	SM320C6455BGTZ2EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Not yet available from a source of supplied.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493