REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	15-06-11	Thomas M. Hess
B	Make clarification to notes 2 and 3 as specified under figure 1. Update document paragraphs to current requirements. - ro	20-09-22	James R. Eschmeyer

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	**REV**			B	B	B	B	B	B	B	B	B	B	B	B	B	B					
	PAGE			1	2	3	4	5	6	7	8	9	10	11	12	13	14					

PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 08-02-26	**CHECKED BY** RAJESH PITHADIA	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, QUAD, DIFFERENTIAL LINE RECEIVER, MONOLITHIC SILICON
	APPROVED BY ROBERT M. HEBER	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/07648**
	REV **B**	**PAGE** 1 **OF** 14

AMSC N/A

5962-V074-20

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance quad differential line receiver microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/07648	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	26C32-EP	Quad differential line receiver

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	MS-012-AC	Plastic surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{CC})	+7 V maximum 2/
Input voltage range (V_I):	
A or B inputs	-11 V to 14 V
G or $\overline{G}$ inputs	-0.5 V to V_{CC} + 0.5 V
Differential input voltage range (V_{ID})	-14 V to 14 V
Output voltage range (V_O)	-0.5 V to V_{CC} + 0.5 V
Output current (I_O)	±25 mA
Package thermal impedance (θ_{JA})	73°C/W 3/ 4/
Operating virtual junction temperature range (T_J)	+150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	+260°C
Storage temperature range	-65°C to +150°C

1.4 Recommended operating conditions. 5/

Supply voltage range (V_{CC})	4.5 V to 5.5 V
High level input voltage (V_{IH})	2 V minimum
Low level input voltage (V_{IL})	0.8 V maximum
Common mode input voltage (V_{IC})	±7 V maximum
High level output current (I_{OH})	-6 mA maximum
Low level output current (I_{OL})	+6 mA maximum
Operating free-air temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ All voltage values, except differential output voltage (V_{OD}) are with respect to network GND. Currents into the device are positive and current out of the device are negative.

3/ Maximum power dissipation is a function of T_J (max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A) / \theta_{JA}$. Operating at the absolute maximum T_J at +150°C can affect reliability.

4/ The package thermal impedance is calculated in accordance with JESD 51-7.

5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuits. The timing waveforms and test circuit shall be as shown in figures 5 and 6.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Differential input high threshold voltage	V_{IT+}	V_{IC} = -7 V to +7 V, $V_O = V_{OH}$(min), I_{OH} = -440 μA	-55°C to +125°C	01		0.2	V
		V_{IC} = 0 V to +5.5 V, $V_O = V_{OH}$(min), I_{OH} = -440 μA				0.1	
Differential input low threshold voltage	V_{IT-}	V_{IC} = -7 V to +7 V, V_O = 0.45 V, I_{OL} = 8 mA	-55°C to +125°C	01	-0.2 3/		V
		V_{IC} = 0 V to +5.5 V, V_O = 0.45 V, I_{OL} = 8 mA			-0.1 3/		
Hysteresis voltage (V_{IT+} - V_{IT-})	V_{hys}	V_{CC} = 5 V, V_{IC} = 0 V	+25°C	01	60 typical		mV
Enable input clamp voltage	V_{IK}	V_{CC} = 4.5 V, I_I = -18 mA	-55°C to +125°C	01		-1.5	V
High level output voltage	V_{OH}	V_{ID} = 200 mV, I_{OH} = -6 mA	-55°C to +125°C	01	3.8		V
Low level output voltage	V_{OL}	V_{ID} = -200 mV, I_{OL} = 6 mA	-55°C to +125°C	01		0.3	V
Offset state (high impedance state) output current	I_{OZ}	$V_O = V_{CC}$ or GND	-55°C to +125°C	01		±5	μA
Line input current	I_I	V_I = 10 V, other input at 0 V	-55°C to +125°C	01		1.5	mA
		V_I = -10 V, other input at 0 V				-2.5	
High level enable current	I_{IH}	V_I = 2.7 V	-55°C to +125°C	01		20	μA
Low level enable current	I_{IL}	V_I = 0.4 V	-55°C to +125°C	01		-100	μA
Input resistance	r_i	One input to ground	-55°C to +125°C	01	12		kΩ
Supply current	I_{CC}	V_{CC} = 5.5 V	-55°C to +125°C	01		15	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Switching characteristics section.		Unless otherwise specified, C_L = 50 pF.					
Propagation delay time, low to high level output	t_{PLH}	See figure 5	-55°C to +125°C	01	9	27	ns
Propagation delay time, high to low level output	t_{PHL}	See figure 5	-55°C to +125°C	01	9	27	ns
Output transition time, low to high output	t_{TLH}	See figure 5	-55°C to +125°C	01		10	ns
Output transition time, high to low output	t_{THL}	See figure 5	-55°C to +125°C	01		9	ns
Output enable time to high level	t_{PZH}	See figure 6	-55°C to +125°C	01		22	ns
Output enable time to low level	t_{PZL}	See figure 6	-55°C to +125°C	01		22	ns
Output disable time from high level	t_{PHZ}	See figure 6	-55°C to +125°C	01		26	ns
Output disable time from low level	t_{PLZ}	See figure 6	-55°C to +125°C	01		25	ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{CC} = 4.5 V to 5.5 V and V_{IC} = ±7 V.

3/ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage.

Case X

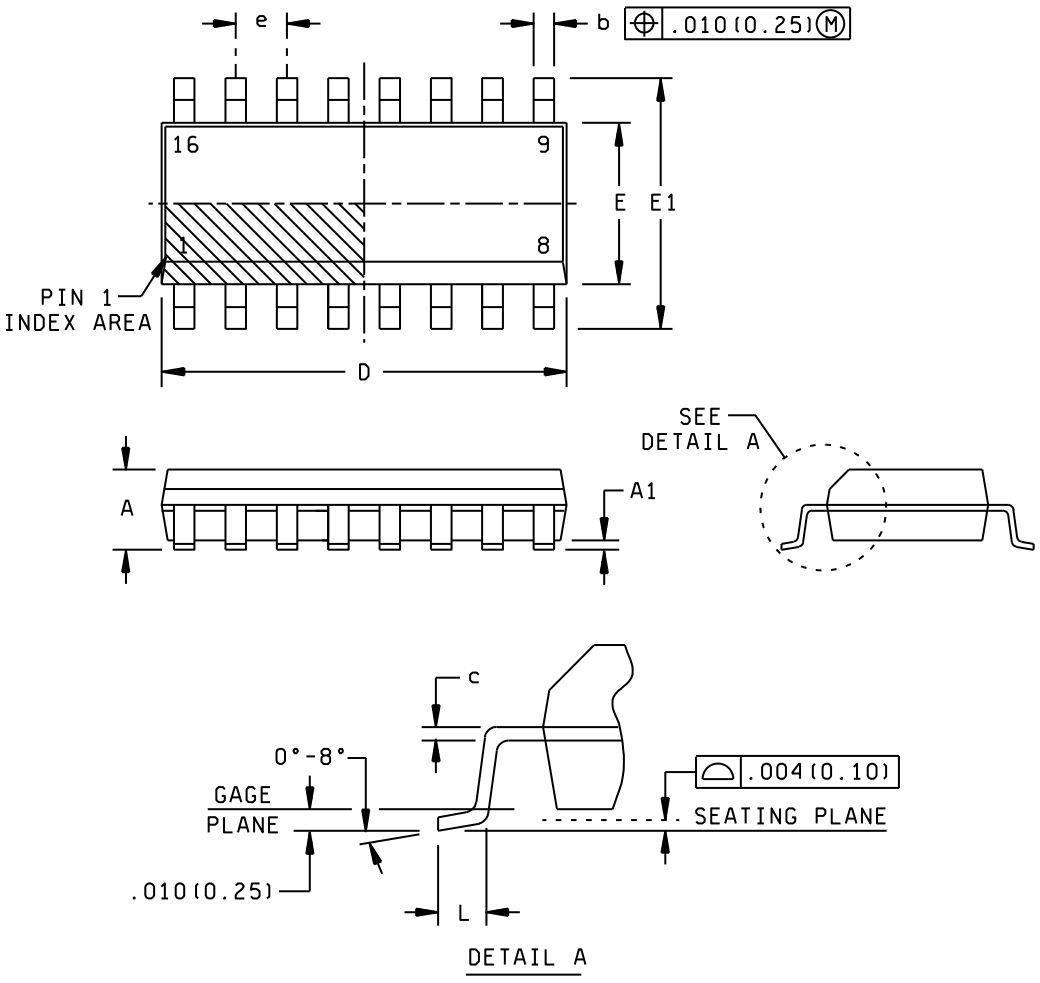


FIGURE 1. Case outline.

Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.069	---	1.75
A1	0.004	0.010	0.10	0.25
b	0.012	0.020	0.31	0.51
c	0.007	0.010	0.17	0.25
D	0.386	0.394	9.80	10.00
E	0.150	0.157	3.80	4.00
E1	0.228	0.244	5.80	6.20
e	0.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27

NOTES:

1. All linear dimensions are in inches (millimeters).
2. Dimension D body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch (0.15 mm) per side.
3. Dimension E body width does not include interlead flash. Interlead flash shall not exceed .017 inch (0.43 mm) each side.
4. Falls within JEDEC MS-012 variation AC.

FIGURE 1. Case outline - Continued.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	1B
2	1A
3	1Y
4	G
5	2Y
6	2A
7	2B
8	GND
9	3B
10	3A
11	3Y
12	$\overline{G}$
13	4Y
14	4A
15	4B
16	V_{CC}

FIGURE 2. Terminal connections.

Differential input	Enables		Output
	G	$\overline{G}$	Y
$V_{ID} \geq V_{IT+}$	H	X	H
	X	L	H
$V_{IT-} < V_{ID} < V_{IT+}$	H	X	?
	X	L	?
$V_{ID} \leq V_{IT-}$	H	X	L
	X	L	L
X	L	H	Z

FIGURE 3. Truth table.

POSITIVE LOGIC

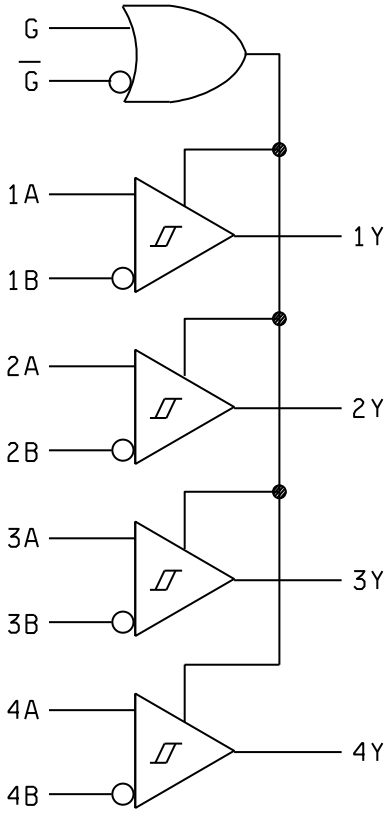
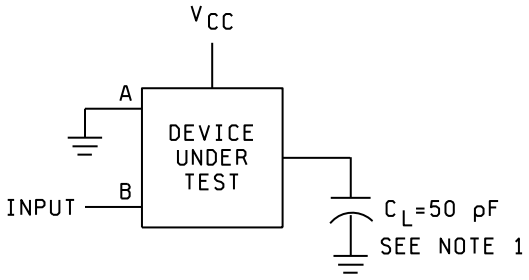
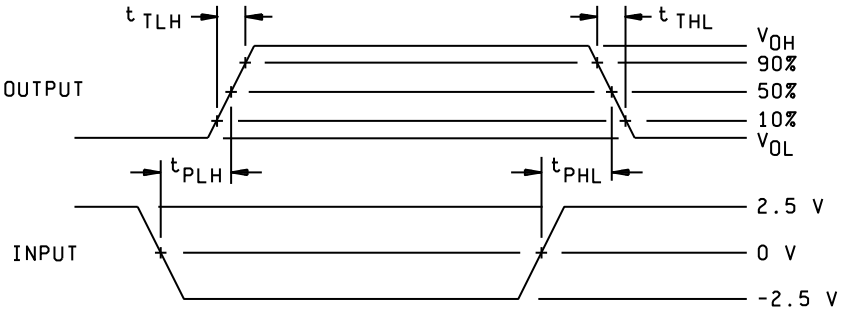


FIGURE 4. Logic diagram.

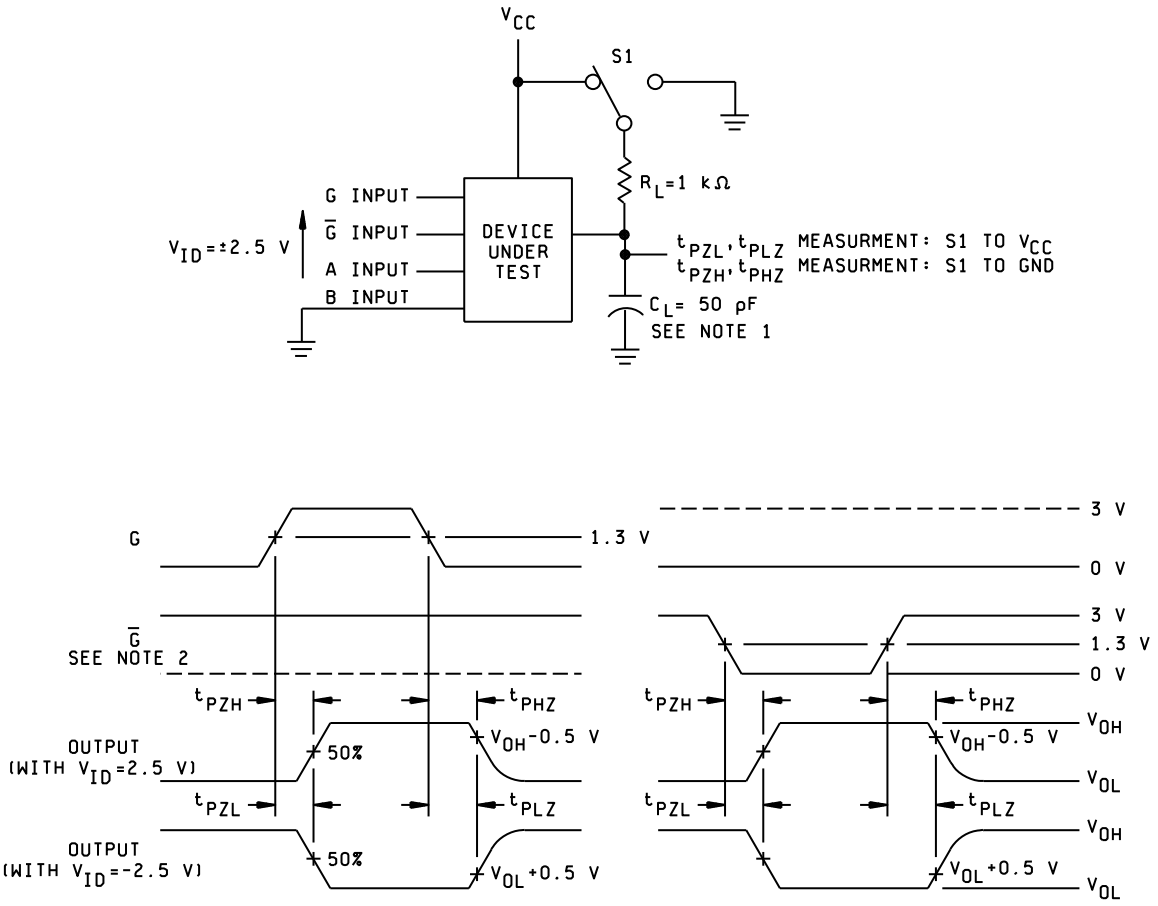




NOTE:

1. C_L includes probe and jig capacitance.

FIGURE 5. Timing waveforms and test circuit.



NOTES:

1. C_L includes probe and jig capacitance.
2. The input is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50 %, t_r = t_f = 6 ns.

FIGURE 6. Enable / disable time test circuit and output voltage waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Package 2/	Top side marking	Vendor part number
V62/07648-01XE	01295	Reel of 2500	26C32EP	AM26C32MDREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's datasheet.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243