REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	15-06-11	Thomas M. Hess
B	Make change to the dimension c minimum limit from 0.007 inch to 0.005 inch and make clarification to notes 2 and 3 as specified under figure 1. Update document paragraphs to current requirements. - ro	20-09-17	James R. Eschmeyer

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	**REV**			B	B	B	B	B	B	B	B	B	B	B	B	B	B	B		
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PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 08-02-26	**CHECKED BY** RAJESH PITHADIA	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, QUAD, DIFFERENTIAL LINE DRIVER, MONOLITHIC SILICON
	APPROVED BY ROBERT M. HEBER	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/07647**
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AMSC N/A

5962-V073-20

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance quad differential line driver microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/07647	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	26C31-EP	Quad differential line driver

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	MS-012-AC	Plastic surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to +7 V 2/
Input voltage range (V_I)	-0.5 V to V_{CC} + 0.5 V
Differential input voltage range (V_{ID})	-14 V to 14 V
Output voltage range (V_O)	-0.5 V to +7 V
Input or output clamp current (I_{IK} or I_{OK})	±20 mA
Output current (I_O)	±150 mA
V_{CC} current	200 mA
GND current	-200 mA
Package thermal impedance (θ_{JA})	73°C/W 3/ 4/
Operating virtual junction temperature range (T_J)	+150°C
Storage temperature range	-65°C to +150°C

1.4 Recommended operating conditions. 5/

Supply voltage range (V_{CC})	4.5 V to 5.5 V
Differential input voltage (V_{ID})	±7 V nominal
High level input voltage (V_{IH})	2 V minimum
Low level input voltage (V_{IL})	0.8 V maximum
High level output current (I_{OH})	-20 mA maximum
Low level output current (I_{OL})	+20 mA maximum
Operating free-air temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ All voltage values, except differential output voltage (V_{OD}) are with respect to network ground terminal.

3/ Maximum power dissipation is a function of T_J (max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A) / \theta_{JA}$. Operating at the absolute maximum T_J at +150°C can affect reliability.

4/ The package thermal impedance is calculated in accordance with JESD 51-7.

5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JESD 51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JEDEC PUB 95	–	Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuits. The timing waveforms and test circuits shall be as shown in figures 5, 6, 7, and 8.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	I_O = -20 mA	-55°C to +125°C	01	2.2		V
Low level output voltage	V_{OL}	I_O = 20 mA	-55°C to +125°C	01		0.4	V
Differential output voltage magnitude	$\|V_{OD}\|$	R_L = 100 Ω, see figure 5	-55°C to +125°C	01	2		V
Change in magnitude of differential output voltage	$\Delta\|V_{OD}\|$	R_L = 100 Ω, see figure 5 3/	-55°C to +125°C	01		±0.4	V
Common mode output voltage	V_{OC}	R_L = 100 Ω, see figure 5	-55°C to +125°C	01		3	V
Change in magnitude of common mode output voltage	$\Delta\|V_{OC}\|$	R_L = 100 Ω, see figure 5 3/	-55°C to +125°C	01		±0.4	V
Input current	I_I	V_I = V_{CC} or GND	-55°C to +125°C	01		±1	µA
Driver output current with power off	$I_{O(off)}$	V_O = 6 V, V_{CC} = 0 V	-55°C to +125°C	01		100	µA
		V_O = -0.25 V, V_{CC} = 0 V				-100	
Driver output short circuit current	I_{OS}	V_O = 0 V	-55°C to +125°C	01		-170	mA
High impedance off state output current	I_{OZ}	V_O = 2.5 V	-55°C to +125°C	01		20	µA
		V_O = 0.5 V				-20	
Quiescent supply current	I_{CC}	V_I = 0 V or 5 V, I_O = 0	-55°C to +125°C	01		100	µA
		V_I = 2.4 V or 0.5 V, I_O = 0 4/				3.2	mA
Input capacitance	C_I	V_{CC} = 5 V	+25°C	01	6 typical		pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Switching characteristics section.		Unless otherwise specified, C_L = 50 pF.					
Propagation delay time, low to high level output	t_{PLH}	S1 is open, see figure 6	-55°C to +125°C	01		12	ns
Propagation delay time, high to low level output	t_{PHL}	S1 is open, see figure 6	-55°C to +125°C	01		12	ns
Pulse skew time ($\|t_{PLH} - t_{PHL}\|$)	$t_{sk(p)}$	S1 is open, see figure 6	-55°C to +125°C	01		4	ns
Differential output rise and fall times	$t_{r(OD)}$, $t_{f(OD)}$	S1 is open, see figure 7	-55°C to +125°C	01		12	ns
Output enable time to high level	t_{PZH}	S1 is closed, see figure 8	-55°C to +125°C	01		19	ns
Output enable time to low level	t_{PZL}	S1 is closed, see figure 8	-55°C to +125°C	01		19	ns
Output disable time from high level	t_{PHZ}	S1 is closed, see figure 8	-55°C to +125°C	01		16	ns
Output disable time from low level	t_{PLZ}	S1 is closed, see figure 8	-55°C to +125°C	01		16	ns
Power dissipation 5/ capacitance (each driver)	C_{pd}	S1 is open, see figure 6, V_{CC} = 5 V	+25°C	01	100 typical		pF

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{CC} = 4.5 V to 5.5 V.

3/ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

4/ This parameter is measured per input. All other inputs are at 0 V or 5 V.

5/ C_{pd} is used to estimate the switching losses according to $P_D = C_{pd} \times V_{CC}^2 \times f$, where f is the switching frequency.

Case X

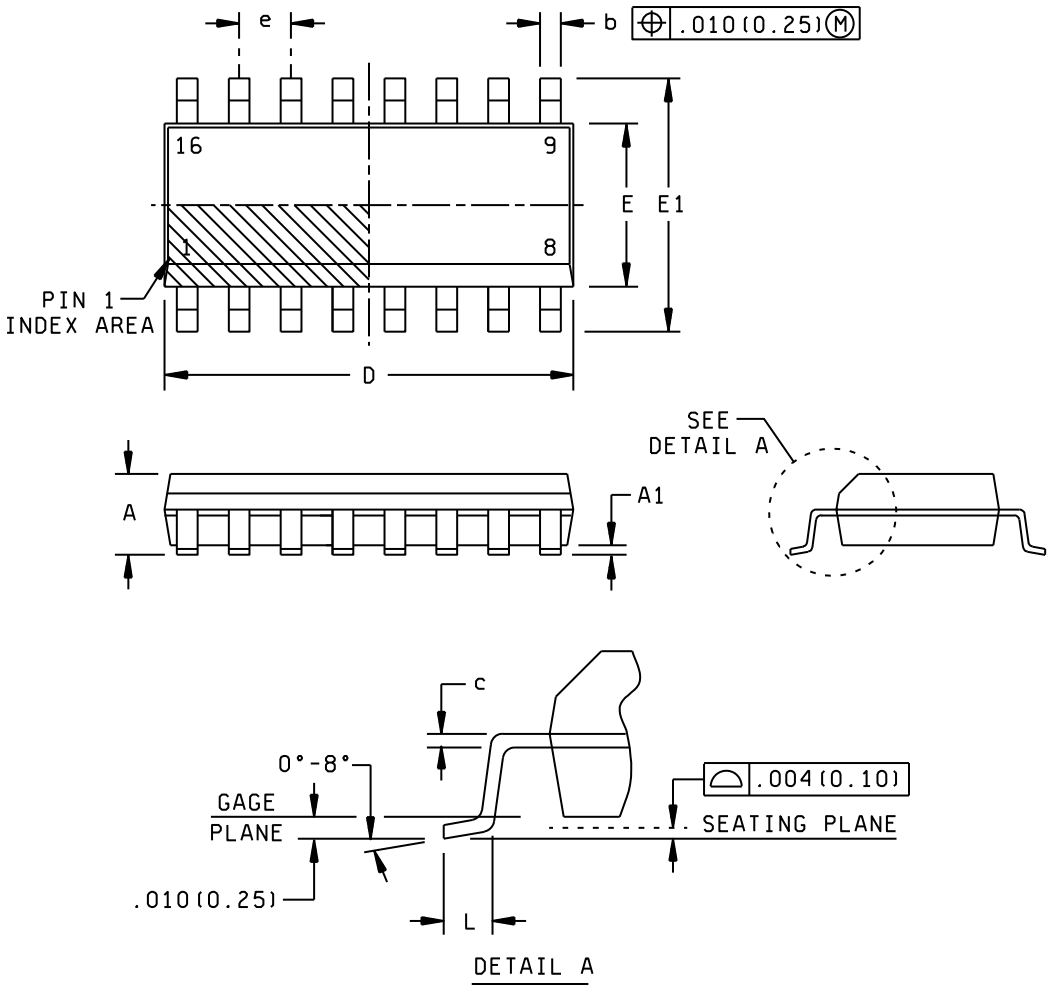

FIGURE 1. Case outline.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/07647
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Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.069	---	1.75
A1	0.004	0.010	0.10	0.25
b	0.012	0.020	0.31	0.51
c	0.005	0.010	0.13	0.25
D	0.386	0.394	9.80	10.00
E	0.150	0.157	3.80	4.00
E1	0.228	0.244	5.80	6.20
e	0.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27

NOTES:

1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) per end.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) per side.
4. Falls within reference to JEDEC MS-012-AC.

FIGURE 1. Case outline - Continued.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	1A
2	1Y
3	1Z
4	G
5	2Z
6	2Y
7	2A
8	GND
9	3A
10	3Y
11	3Z
12	$\overline{G}$
13	4Z
14	4Y
15	4A
16	V_{CC}

FIGURE 2. Terminal connections.

(Each driver)

Input	Enables		Output	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

FIGURE 3. Truth table.

POSITIVE LOGIC

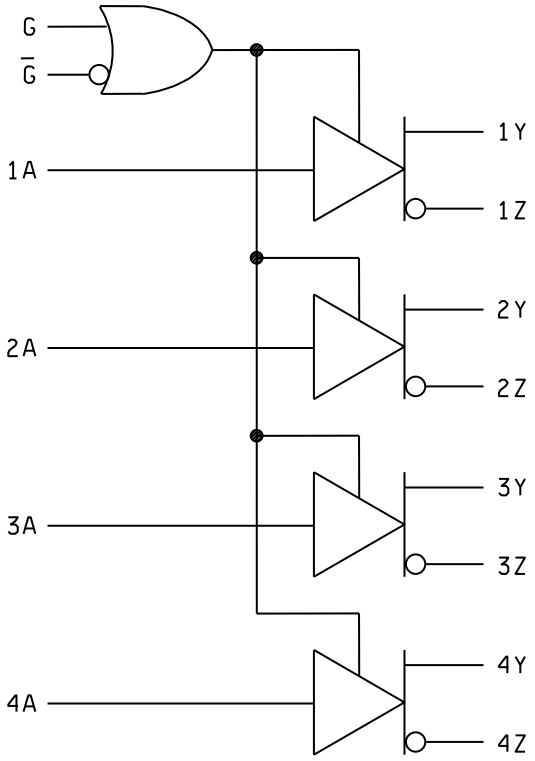


FIGURE 4. Logic diagram.

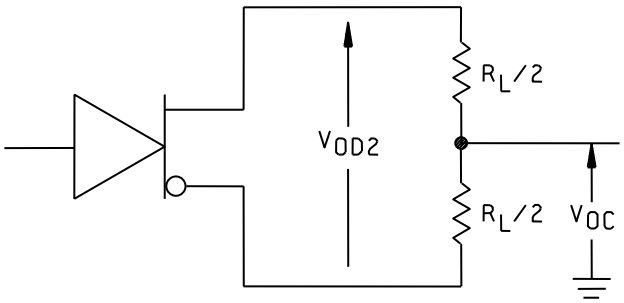
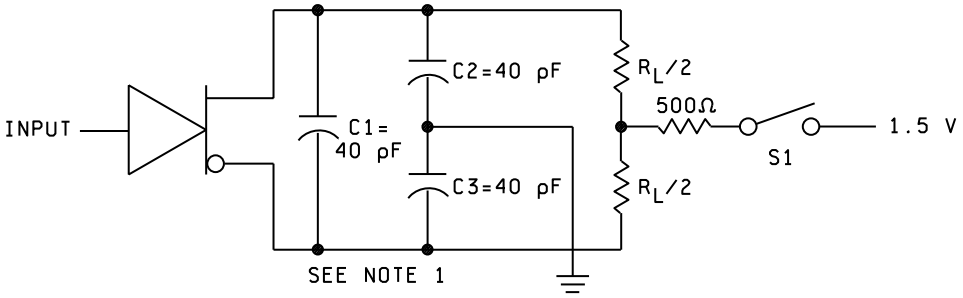
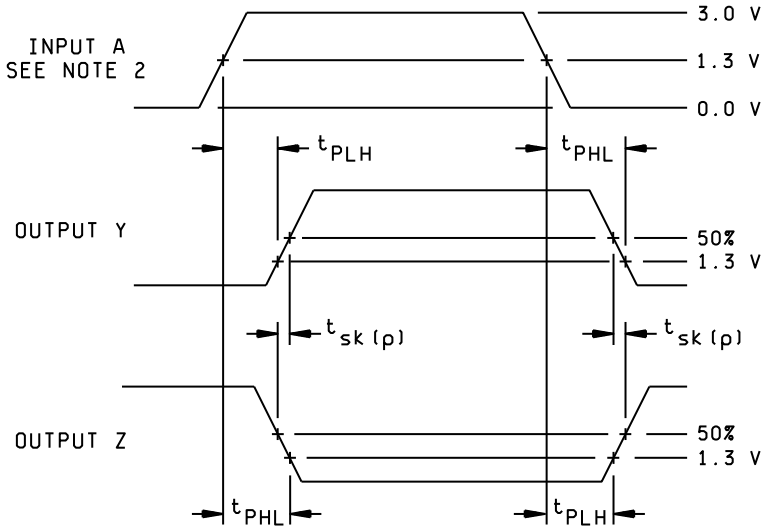


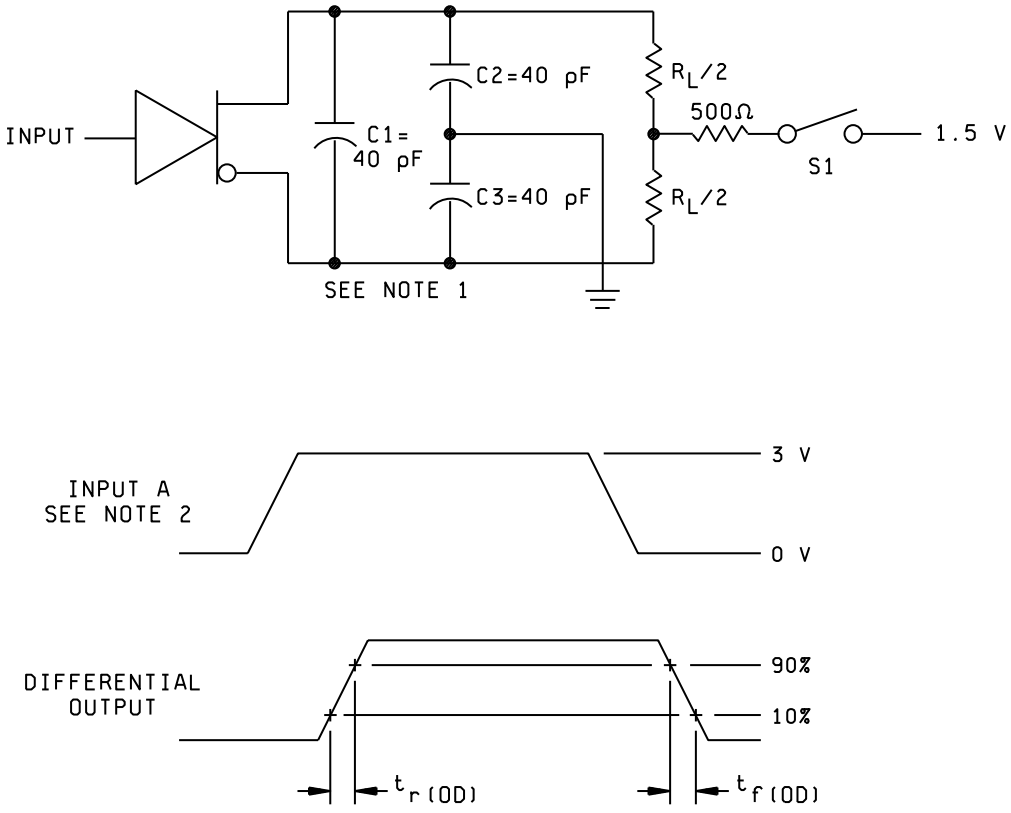
FIGURE 5. Differential and common mode output voltages.





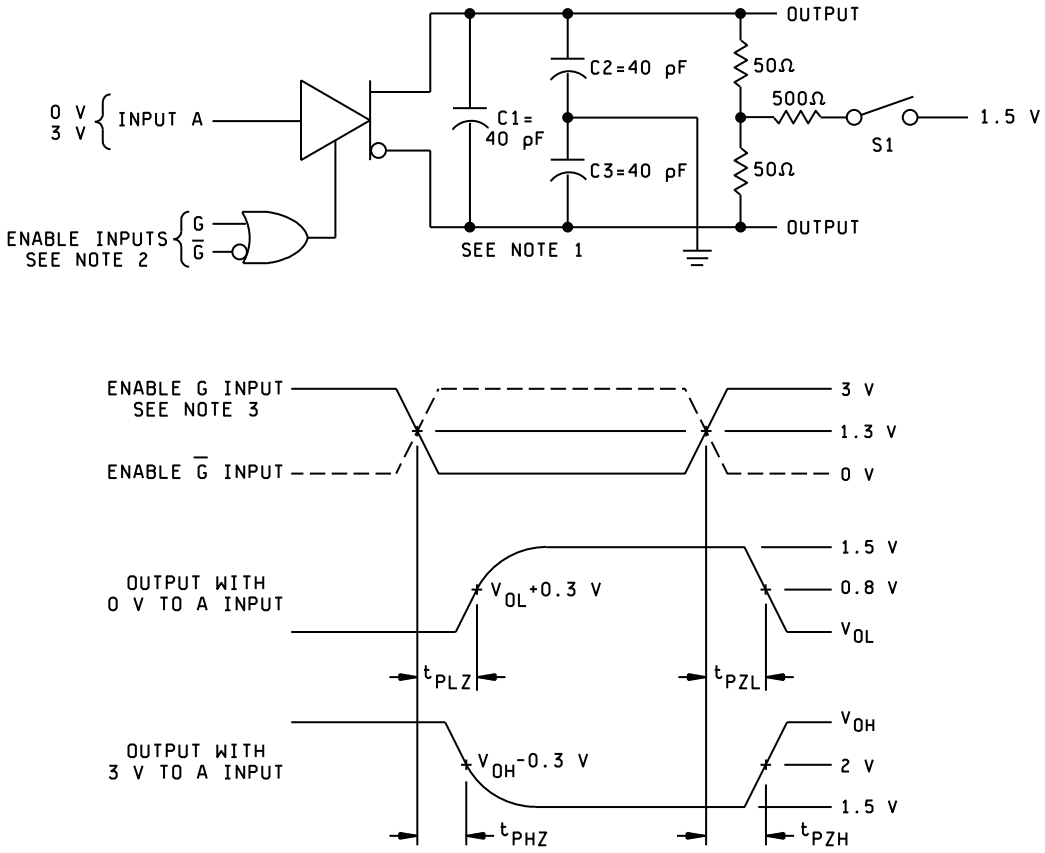
NOTES:
1. C1, C2, C3 include probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics:
   PRR ≤ 1 MHz, duty cycle ≤ 50 %, tr , tf ≤ 6 ns.

FIGURE 6. Propagation delay time and skew waveforms and test circuit.



NOTES:
1. C1, C2, C3 include probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics:
   PRR ≤ 1 MHz, duty cycle ≤ 50 %, t_r , t_f ≤ 6 ns.

FIGURE 7. Differential output rise and fall time waveforms and test circuit.



NOTES:

1. C1, C2, C3 include probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics:
   PRR ≤ 1 MHz, duty cycle ≤ 50 %, t_r < 6 ns, and t_f < 6 ns.
3. Each enable is tested separately.

FIGURE 8. Output enable and disable time waveforms and test circuit.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Package 2/	Top side marking	Vendor part number
V62/07647-01XE	01295	Reel of 2500	26C31EP	AM26C31MDREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's datasheet.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243