



1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance single buffer / driver with open drain output microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/07645</u> Drawing number	-	<u>01</u> Device type (See 1.2.1)	<u>X</u> Case outline (See 1.2.2)	<u>E</u> Lead finish (See 1.2.3)
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1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74LVC1G07-EP	Single buffer / driver with open drain output

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	5	MO-203-AA	Plastic surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range ( $V_{CC}$ ).....	-0.5 V to 6.5 V
Input voltage range ( $V_I$ ) .....	-0.5 V to 6.5 V 2/
Voltage range applied to any output in the high impedance or power off state ( $V_O$ ) .....	-0.5 V to 6.5 V 2/
Voltage range applied to any output in the high or low state ( $V_O$ ) .....	-0.5 V to 6.5 V 2/ 3/
Input clamp current ( $I_{IK}$ ) ( $V_I < 0$ ) .....	-50 mA maximum
Output clamp current ( $I_{OK}$ ) ( $V_O < 0$ ) .....	-50 mA maximum
Continuous output current ( $I_O$ ) .....	50 mA maximum
Continuous current through $V_{CC}$ or GND .....	100 mA
Junction temperature ( $T_J$ ) .....	+132°C
Storage temperature range ( $T_{STG}$ ).....	-65°C to 150°C
Package thermal impedance ( $\theta_{JA}$ ) .....	252°C/W 4/

1.4 Recommended operating conditions. 5/ 6/

Supply voltage range ( $V_{CC}$ ):	
Operating .....	1.65 V to 5.5 V
Data retention only .....	1.5 V minimum
High level input voltage ( $V_{IH}$ ):	
$V_{CC} = 1.65$ V to 1.95 V .....	0.65 x $V_{CC}$ minimum
$V_{CC} = 2.3$ V to 2.7 V .....	1.7 V minimum
$V_{CC} = 3$ V to 3.6 V .....	2 V minimum
$V_{CC} = 4.5$ V to 5.5 V .....	0.7 x $V_{CC}$ minimum
Low level input voltage ( $V_{IL}$ ):	
$V_{CC} = 1.65$ V to 1.95 V .....	0.35 x $V_{CC}$ maximum
$V_{CC} = 2.3$ V to 2.7 V .....	0.7 V maximum
$V_{CC} = 3$ V to 3.6 V .....	0.8 V maximum
$V_{CC} = 4.5$ V to 5.5 V .....	0.3 x $V_{CC}$ maximum
Input voltage ( $V_I$ ) .....	0 V to 5.5 V
Output voltage ( $V_O$ ) .....	0 V to 5.5 V

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ The input and output negative voltage ratings may be exceeded if the input and output current ratings are observed.

3/ This value of  $V_{CC}$  is provided in the recommended operating conditions stable.

4/ The package thermal impedance is calculated in accordance with JESD 51-7.

5/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

6/ All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the manufacturer’s application report, implication of slow or floating CMOS inputs, literature number SCBA004.

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1.4 Recommended operating conditions - continued. 5/ 6/

Low level output current ( I<sub>OL</sub> ):

V <sub>CC</sub> = 1.65 V .....	4 mA maximum
V <sub>CC</sub> = 2.3 V .....	8 mA maximum
V <sub>CC</sub> = 3 V .....	16 mA maximum
V <sub>CC</sub> = 3 V .....	24 mA maximum
V <sub>CC</sub> = 4.5 V .....	32 mA maximum

Input transition rise or fall rate (Δt / ΔV) :

V <sub>CC</sub> = 1.8 V ±0.15 V, 2.5 V ±0.2 V .....	20 ns/V
V <sub>CC</sub> = 3.3 V ±0.3 V .....	10 ns/V
V <sub>CC</sub> = 5 V ±0.5 V .....	5 ns/V

Operating free-air temperature range ( T<sub>A</sub> )..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

- JEDEC 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <http://www.jedec.org> or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function table. The function table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Load circuit and timing waveforms. The load circuit and timing waveforms shall be as shown in figure 5.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	Temperature, T <sub>A</sub>	Device type	Limits		Unit
					Min	Max	
Low level output voltage	V <sub>OL</sub>	V <sub>CC</sub> = 1.65 to 5.5 V, I <sub>OL</sub> = 100 μA	-55°C to +125°C	01		0.1	V
		V <sub>CC</sub> = 1.65 V, I <sub>OL</sub> = 4 mA				0.45	
		V <sub>CC</sub> = 2.3 V, I <sub>OL</sub> = 8 mA				0.3	
		V <sub>CC</sub> = 3 V, I <sub>OL</sub> = 16 mA				0.4	
		V <sub>CC</sub> = 3 V, I <sub>OL</sub> = 24 mA				0.55	
		V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 32 mA				0.55	
Input current (A input)	I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	-55°C to +125°C	01		±5	μA
Off current	I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5 V, V <sub>CC</sub> = 0 V	-55°C to +125°C	01		±10	μA
Supply current	I <sub>CC</sub>	V <sub>I</sub> = 5.5 or GND, I <sub>O</sub> = 0, V <sub>CC</sub> = 1.65 V to 5.5 V	-55°C to +125°C	01		10	μA
Quiescent supply current delta	ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, other inputs at V <sub>CC</sub> or GND, V <sub>CC</sub> = 3 V to 5.5 V	-55°C to +125°C	01		500	μA
Input capacitance	C <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>CC</sub> = 3.3 V	+25°C	01	4.0 typical		pF
Output capacitance	C <sub>O</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND, V <sub>CC</sub> = 3.3 V	+25°C	01	5 typical		pF
Power dissipation capacitance	C <sub>pd</sub>	f = 10 MHz, V <sub>CC</sub> = 3.3 V	+25°C	01	4 typical		pF
		f = 10 MHz, V <sub>CC</sub> = 5 V			6 typical		
Propagation delay from input A to output Y	t <sub>pd</sub>	V <sub>CC</sub> = 3.3 V ±0.3 V	-55°C to +125°C	01	1.5	5.7	ns
		V <sub>CC</sub> = 5 V ±0.5 V			1	4.9	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

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Case X

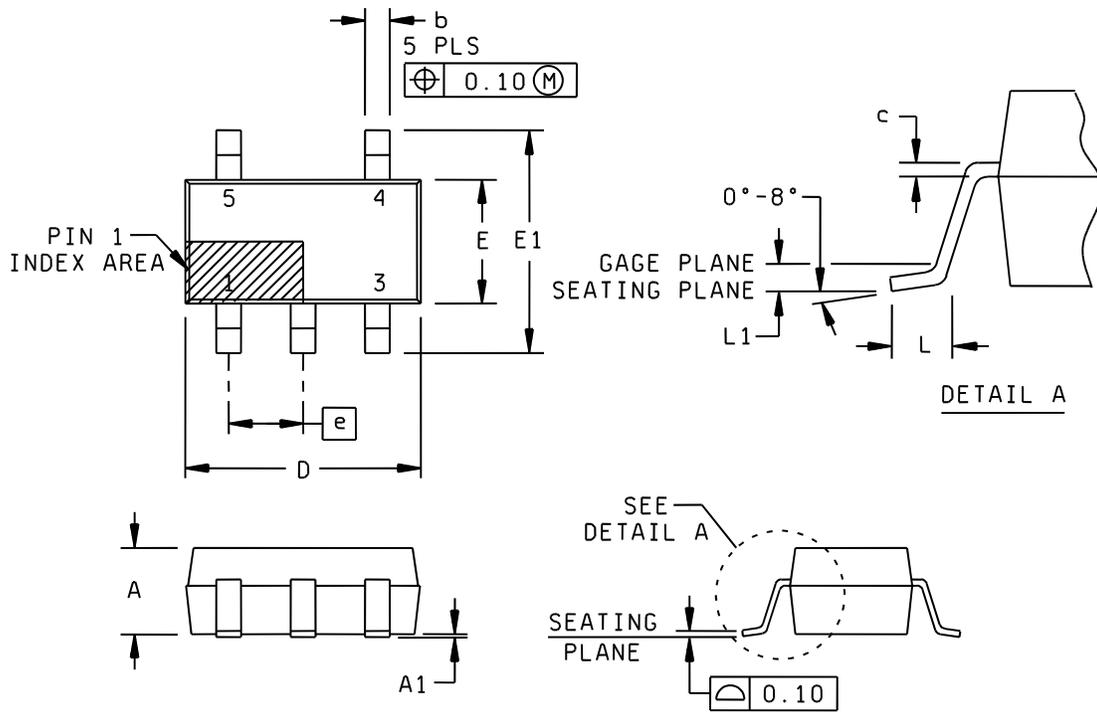


FIGURE 1. Case outline.

<p><b>DEFENSE SUPPLY CENTER, COLUMBUS</b>  <b>COLUMBUS, OHIO</b></p>	<p>SIZE  <b>A</b></p>	<p>CODE IDENT NO.  <b>16236</b></p>	<p>DWG NO.  <b>V62/07645</b></p>
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Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.031	.043	0.80	1.10
A1	.000	.003	0.00	0.10
b	.005	.011	0.15	0.30
c	.003	.008	0.08	0.22
D	.072	.084	1.85	2.15
E	.043	.055	1.10	1.40
E1	.070	.094	1.80	2.40
e	.025 BSC		0.65 BSC	
L	.010	.018	0.26	0.46
L1	.005 BSC		0.15 BSC	

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 mm (0.005 inch) per side.
3. Falls within JEDEC MO-203-AA.

FIGURE 1. Case outline - Continued.

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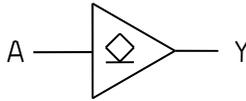
Device type	01
Case outline	X
Terminal number	Terminal symbol
1	NC
2	A
3	GND
4	Y
5	V <sub>CC</sub>

FIGURE 2. Terminal connections.

Inputs	Output
A	Y
H	H
L	L

H = High voltage level  
L = Low voltage level

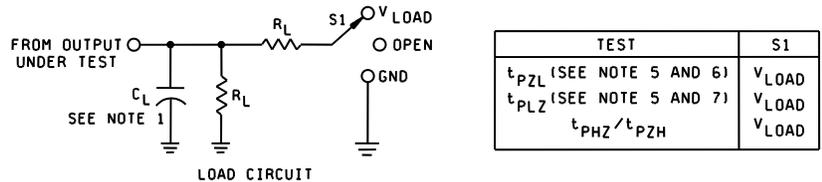
FIGURE 3. Functional table.



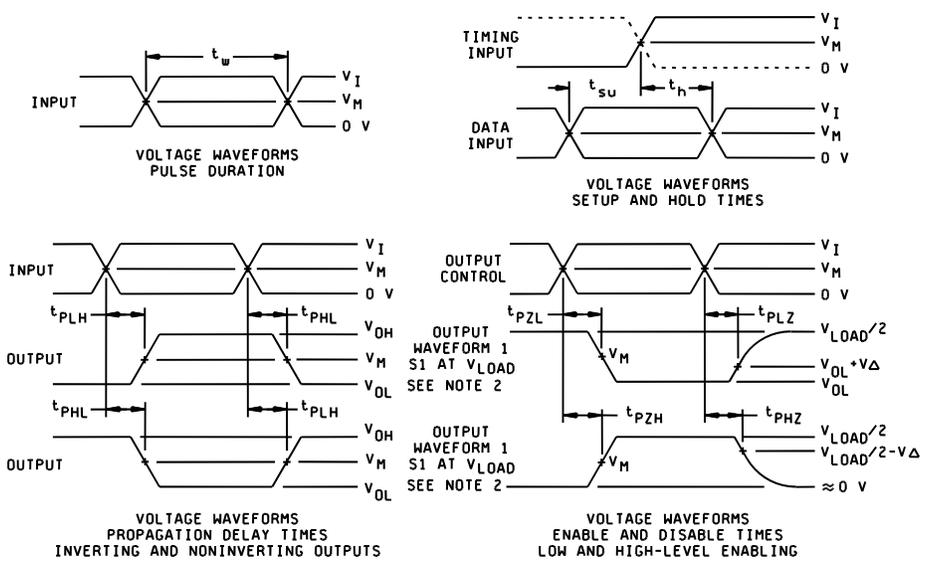
Positive logic

FIGURE 4. Logic diagram.

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$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$3.3\text{ V} \pm 0.3\text{ V}$ $5\text{ V} \pm 0.5\text{ V}$	$3\text{ V}$ $V_{CC}$	$\leq 2.5\text{ ns}$ $\leq 2.5\text{ ns}$	$1.5\text{ V}$ $V_{CC}/2$	$6\text{ V}$ $2 \times V_{CC}$	$50\text{ pF}$ $50\text{ pF}$	$500\Omega$ $500\Omega$	$0.3\text{ V}$ $0.3\text{ V}$



NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
- Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
- The outputs are measured one at a time with one input transition per measurement.
- Since this device has open drain outputs,  $t_{PLZ}$  and  $t_{PZL}$  are the same as  $t_{pd}$ .
- $t_{PZL}$  is measured at  $V_M$ .
- $t_{PLZ}$  is measured at  $V_{OL} + V_{\Delta}$ .
- All parameters and waveforms are not applicable to all devices.

FIGURE 5. Timing waveforms and test circuit.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Package	Top side marking	Vendor part number
V62/07645-01XE	01295	Reel of 3000	CVK	SN74LVC1G07MDCKREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.  
 Semiconductor Group  
 8505 Forest Lane  
 P.O. Box 660199  
 Dallas, TX 75243  
 Point of contact: U.S. Highway 75 South  
 P.O. Box 84, M/S 853  
 Sherman, TX 75090-9493

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