REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Update document paragraphs to current requirements. - ro	14-08-20	C. SAFFLE

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
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REV STATUS OF PAGES	**REV**		A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A		
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PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990**
Original date of drawing YY-MM-DD 07-07-31	**CHECKED BY** RAJESH PITHADIA	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, 24-BIT, 216 kHz SAMPLING, FOUR CHANNEL AUDIO DIGITAL TO ANALOG CONVERTER, MONOLITHIC SILICON
	APPROVED BY ROBERT M. HEBER	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/07643**
	REV **A**	**PAGE** 1 **OF** 17

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 24 bit, 216 kHz sampling, four channel audio digital to analog converter microcircuit, with an operating temperature range of -40°C to +85°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/07643	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	PCM4104-EP	24 bit, 216 kHz sampling, four channel audio digital to analog converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	48	MS-026	Plastic quad flat pack

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range:
- V_{CC} ..... 6.0 V
- V_{DD} ..... 3.6 V

Ground voltage difference:
- Any AGND to AGND and AGND to DGND ..... ±0.1 V

Digital input voltage:
- FSO, FS1, FMT0, FMT1, FMT2, CDOUT, CDIN, CCLK, $\overline{CS}$, DATA0, DATA1, BCK, LRCK, SCKI, SUB, DEM0, DEM1, MUTE, $\overline{RST}$, and MODE pins ..... -0.3 V to (V_{DD} + 0.3 V)

Input current (any pin except supplies) ..... ±10 mA

Storage temperature range (T_{STG}) ..... -65°C to +150°C

Junction temperature range (T_J) ..... 150°C

Thermal resistance, junction to case (θ_{JC}) ..... 19.6°C/W

Thermal resistance, junction to ambient (θ_{JA}) ..... 97.5°C/W

1.4 Recommended operating conditions. 2/

Supply voltage range:
- V_{CC} ..... 5.0 V
- V_{DD} ..... 3.3 V

Operating free-air temperature range (T_A) ..... -40°C to +85°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagrams. The block diagrams shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Resolution			25°C	01	24 typical		Bits
Data format section							
Audio data formats			25°C	01	Left or right justified, inter integrated circuit sound serial bus, and time division multiplexing (TDM)		
Audio data word length			25°C	01	16	24	Bits
Binary data format			25°C	01	Two's complement binary, MSB first		
Clock rates and timing section							
System clock frequency	f_{SCKI}	Single rate sampling mode	25°C	01	6.144	36.864	MHz
		Dual rate sampling mode			13.824	36.864	
		Quad rate sampling mode			13.824	36.864	
Sampling frequency	f_S	Single rate sampling mode	25°C	01	24	54	kHz
		Dual rate sampling mode			54	108	
		Quad rate sampling mode			108	216	
Serial peripheral interface (SPI) port data clock	f_{CCLK}		25°C	01		24	MHz
Serial peripheral interface (SPI) port data clock high time	f_{CCLKH}		25°C	01	15		ns
Serial peripheral interface (SPI) port data clock low time	f_{CCLKL}		25°C	01	15		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Digital input/output section							
Input logic level	V_{IH}		25°C	01	2.0		V
	V_{IL}					0.8	
Input logic current	I_{IH}	V_{IN} = 2.64 V	-40°C to +85°C	01		10	µA
	I_{IL}	V_{IN} = 0.66 V				-10	
Output logic level	V_{OH}	I_{OH} = -2 mA	-40°C to +85°C	01	2.4		V
	V_{OL}	I_{OL} = +2 mA				0.4	
Analog outputs section							
Full scale output voltage, differential		R_L = 600 Ω	25°C	01	6.15 typical		V_{PP}
Bipolar zero voltage			25°C	01	2.5 typical		V
Output impedance			25°C	01	5 typical		Ω
Switched capacitor filter frequency response		f = 20 kHz, all sampling modes	25°C	01	-0.2 typical		dB
Gain error			25°C	01	0.5 typical		%FSR
Gain mismatch, channel to channel			25°C	01	0.6 typical		%FSR
Bipolar zero error			25°C	01	1 typical		mV
$V_{COM}1$ and $V_{COM}2$ output voltage		V_{CC} = 5 V	25°C	01	2.5 typical		V
$V_{COM}1$ and $V_{COM}2$ output current			25°C	01		200	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Dynamic performance with 24 bit data 3/							
f_S = 48 kHz section							
Total harmonic distortion + noise	THD+N	f = 1 kHz at 0 dBFS	25°C	01		-94	dB
			-40°C to +85°C			-91	
		f = 1 kHz at -60 dBFS	25°C		-56 typical		
Dynamic range, A-weighted		f = 1 kHz at -60 dBFS	25°C	01	112		dB
			-40°C to +85°C		109		
Idle channel signal to noise ratio (SNR), A-weighted		All zero input data	25°C	01	119 typical		dB
Idle channel signal to noise ratio (SNR), unweighted		All zero input data	25°C	01	116 typical		dB
Channel separation		f = 1 kHz at 0 dBFS for active channel	25°C	01	100		dB
			-40°C to +85°C		98		
f_S = 96 kHz section							
Total harmonic distortion + noise	THD+N	f = 1 kHz at 0 dBFS, BW = 10 Hz to 40 kHz	25°C	01	-100 typical		dB
		f = 1 kHz at -60 dBFS, BW = 10 Hz to 40 kHz			-53 typical		
Dynamic range, A-weighted		f = 1 kHz at -60 dBFS	25°C	01	118 typical		dB
Idle channel signal to noise ratio (SNR), A-weighted		All zero input data	25°C	01	119 typical		dB
Idle channel signal to noise ratio (SNR), unweighted		All zero input data, BW = 10 Hz to 40 kHz	25°C	01	113 typical		dB
Channel separation		f = 1 kHz at 0 dBFS for active channel	25°C	01	110 typical		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Dynamic performance with 24 bit data – continued. 3/							
f_S = 192 kHz section							
Total harmonic distortion + noise	THD+N	f = 1 kHz at 0 dBFS, BW = 10 Hz to 40 kHz	25°C	01	-97 typical		dB
		f = 1 kHz at -60 dBFS, BW = 10 Hz to 40 kHz			-53 typical		
Dynamic range, A-weighted		f = 1 kHz at -60 dBFS	25°C	01	118 typical		dB
Idle channel signal to noise ratio (SNR), A-weighted		All zero input data	25°C	01	118 typical		dB
Idle channel signal to noise ratio (SNR), unweighted		All zero input data, BW = 10 Hz to 40 kHz	25°C	01	113 typical		dB
Channel separation		f = 1 kHz at 0 dBFS for active channel	25°C	01	110 typical		dB
Dynamic performance with 16 bit data							
f_S = 44.1 kHz section							
Total harmonic distortion + noise	THD+N	f = 1 kHz at 0 dBFS	25°C	01	-92 typical		dB
		f = 1 kHz at -60 dBFS			-33 typical		
Dynamic range, A-weighted		f = 1 kHz at -60 dBFS	25°C	01	96 typical		dB
Idle channel signal to noise ratio (SNR), A-weighted		All zero input data 4/	25°C	01	118 typical		dB
Idle channel signal to noise ratio (SNR), unweighted		All zero input data 4/	25°C	01	115 typical		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Digital filters section							
Passband		±0.002 dB	25°C	01		$0.454f_S$	Hz
		- 3 dB				$0.487f_S$	
Stop band			25°C	01	$0.546f_S$		Hz
Passband ripple			25°C	01		±0.002	dB
Stopband attenuation		$0.546f_S$	25°C	01	-75		dB
		$0.567f_S$			-82		
Group delay			25°C	01	$29/f_S$ typical		sec
De-emphasis filter error			25°C	01		0.1	dB
Power supply							
Supply range section							
Analog supply	V_{CC}		25°C	01	4.75	5.25	V
Digital supply	V_{DD}		25°C	01	3.0	3.6	V
Power down current section		V_{CC} = 5 V, V_{DD} = 3.3 V					
Power down supply current	I_{CC} + I_{DD}	$\overline{RST}$ = low, system and audio clocks off	25°C	01	1 typical		mA
Quiescent current section		System and audio clocks applied, all 0s data					
Analog supply	I_{CC}	V_{CC} = 5 V, f_S = 48 kHz	-40°C to +85°C	01		45	mA
		V_{CC} = 5 V, f_S = 96 kHz	25°C		32 typical		
		V_{CC} = 5 V, f_S = 192 kHz	25°C		32 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Quiescent current section		System and audio clocks applied, all 0s data					
Digital supply	I_{DD}	V_{DD} = 3.3 V, f_S = 48 kHz	-40°C to +85°C	01		17	mA
		V_{DD} = 3.3 V, f_S = 96 kHz	25°C		18 typical		
		V_{DD} = 3.3 V, f_S = 192 kHz	25°C		23 typical		
Total power dissipation	P_D	f_S = 48 kHz, V_{CC} = 5 V, V_{DD} = 3.3 V	-40°C to +85°C	01		286	mW
		f_S = 96 kHz, V_{CC} = 5 V, V_{DD} = 3.3 V	25°C		220 typical		
		f_S = 192 kHz, V_{CC} = 5 V, V_{DD} = 3.3 V	25°C		236 typical		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{CC} = 5 V, V_{DD} = 3.3 V, and a measurement bandwidth from 10 Hz to 20 kHz.
System clock frequency is equal to 256 f_S for single and dual rate sampling modes, and 128 f_S for quad rate sampling mode.

3/ Dynamic performance parameters are measured using an audio precision system two cascade or cascade plus test system. Input data word length is 24 bits with triangular probability density function (PDF) dither (noise) added for dynamic range and THD+N tests. Idle channel SNR is measured with both the soft zero data mute functions disabled and 0% full scale input data with no dither (noise) applied.
The measurement bandwidth is limited by using the audio precision 10 Hz high pass filter in combination with either the AES17 20 kHz low pass filter or AES17 40 kHz low pass filter. All A-weighted measurements are performed using the audio precision A-weighting filter in combination with either the 22 kHz or 80 kHz low pass filter. Measurement mode is set to RMS for all parameters. The average measurement mode will yield better typical performance numbers.

4/ Idle channel signal to noise ratio (SNR) is not limited by word length.

Case X

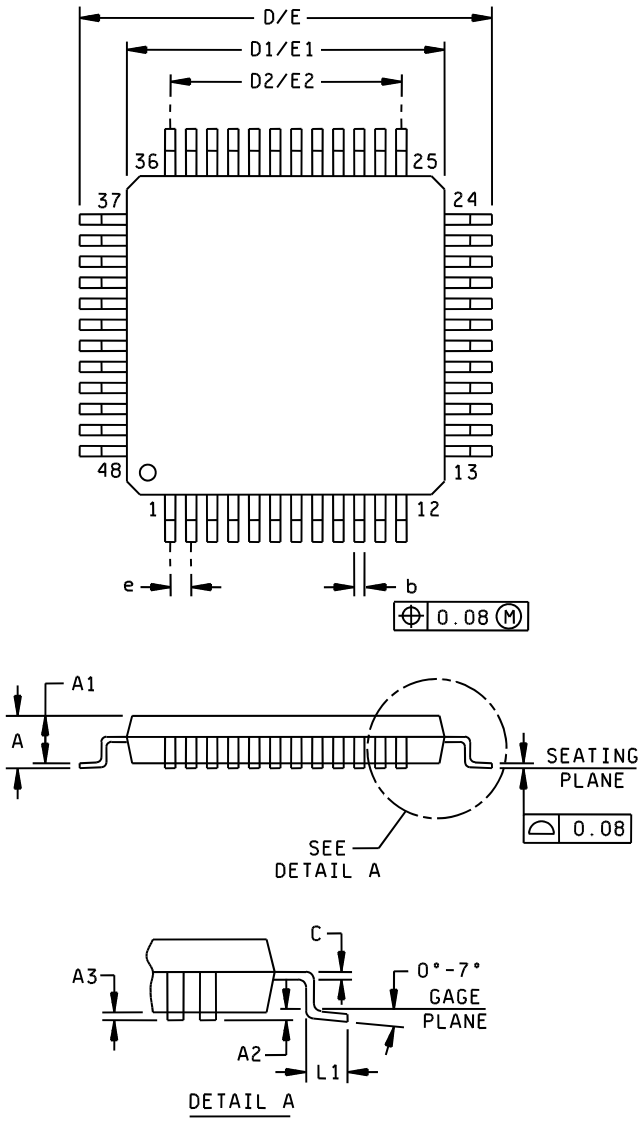

FIGURE 1. Case outline.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/07643
		REV A	PAGE 11

Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.047	---	1.20
A1	0.037	0.041	0.95	1.05
A2	0.009	---	0.25	---
A3	0.001	---	0.05	---
b	0.006	0.010	0.17	0.27
c	0.005 NOM		0.13 NOM	
D/E	0.346	0.362	8.80	9.20
D1/E1	0.267	0.283	6.80	7.20
D2/E2	0.216	---	5.50	---
e	0.019 BSC		0.50 BSC	
L	0.017	0.029	0.45	0.75

NOTES:
1. All linear dimensions are in millimeters, inch equivalents are given for general information only.
2. Fall within JEDEC MS-026.

FIGURE 1. Case outline – continued.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	I/O	Description
1	$V_{OUT}1+$	Output	Channel 1 analog output, noninverted
2	$V_{OUT}1-$	Output	Channel 1 analog output, inverted
3	AGND1	Ground	Analog ground
4	$V_{REF}1-$	Input	Channel 1 low reference voltage, connect to AGND
5	$V_{REF}1+$	Input	Channel 1 high reference voltage, connect to V_{CC}
6	NC	---	No internal connection
7	NC	---	No internal connection
8	MODE	Input	Operating mode (0 = standlone, 1 = software controlled)
9	$\overline{RST}$	Input	Reset / power down (active low)
10	MUTE	Input	All channel soft mute (active high)
11	DEM1	Input	Digital de-emphasis filter configuration
12	DEM0	Input	Digital de-emphasis filter configuration
13	SUB	Input	Subframe assignment (time division multiplexing (TDM) formats only)
14	SCKI	Input	System clock
15	BCK	Input	Audio bit (or data) clock
16	LRCK	Input	Audio left / right (or word) clock
17	DATA0	Input	Audio data for channels 1 and 2 (inter integrated circuit sound serial bus, left/right justified formats) or audio data for channels 1 through 4 for time division multiplexing (TDM) formats
18	DATA1	Input	Audio data for channels 3 and 4 (inter integrated circuit sound serial bus, left/right justified formats)
19	V_{DD}	Power	Digital power supply, 3.3 V
20	DGND	Ground	Digital ground
21	$\overline{CS}$	Input	Serial peripheral interface (SPI) chip select (active low)
22	CCLK	Input	Serial peripheral interface (SPI) data clock
23	CDIN	Input	Serial peripheral interface (SPI) data input
24	CDOUT	Output	Serial peripheral interface (SPI) data output

FIGURE 2. Terminal connections.

Device type	01		
Case outline	X		
Terminal number	Terminal symbol	I/O	Description
25	FMT0	Input	Audio data format configuration
26	FMT1	Input	Audio data format configuration
27	FMT2	Input	Audio data format configuration
28	FS0	Input	Sampling mode configuration
29	FS1	Input	Sampling mode configuration
30	NC	---	No internal connection
31	NC	---	No internal connection
32	$V_{REF}4+$	Input	Channel 4 high reference voltage; connect to V_{CC}
33	$V_{REF}4-$	Input	Channel 4 low reference voltage; connect to AGND
34	AGND2	Ground	Analog ground
35	$V_{OUT}4-$	Output	Channel 4 analog output, inverted
36	$V_{OUT}4+$	Output	Channel 4 analog output, noninverted
37	$V_{COM}2$	Output	DC common mode voltage for channels 3 and 4, 2.5 V nominal
38	$V_{OUT}3+$	Output	Channel 3 analog output, noninverted
39	$V_{OUT}3-$	Output	Channel 3 analog output, inverted
40	$V_{CC}2$	Power	Analog power supply, 5 V
41	$V_{REF}3+$	Input	Channel 3 high reference voltage; connect to V_{CC}
42	$V_{REF}3-$	Input	Channel 3 low reference voltage; connect to AGND
43	$V_{REF}2-$	Input	Channel 2 low reference voltage; connect to AGND
44	$V_{REF}2+$	Input	Channel 2 high reference voltage; connect to V_{CC}
45	$V_{CC}1$	Power	Analog power supply, 5 V
46	$V_{OUT}2-$	Output	Channel 2 analog output, inverted
47	$V_{OUT}2+$	Output	Channel 2 analog output, noninverted
48	$V_{COM}1$	Output	DC common mode voltage for channels 1 and 2, 2.5 V nominal

FIGURE 2. Terminal connections – Continued.

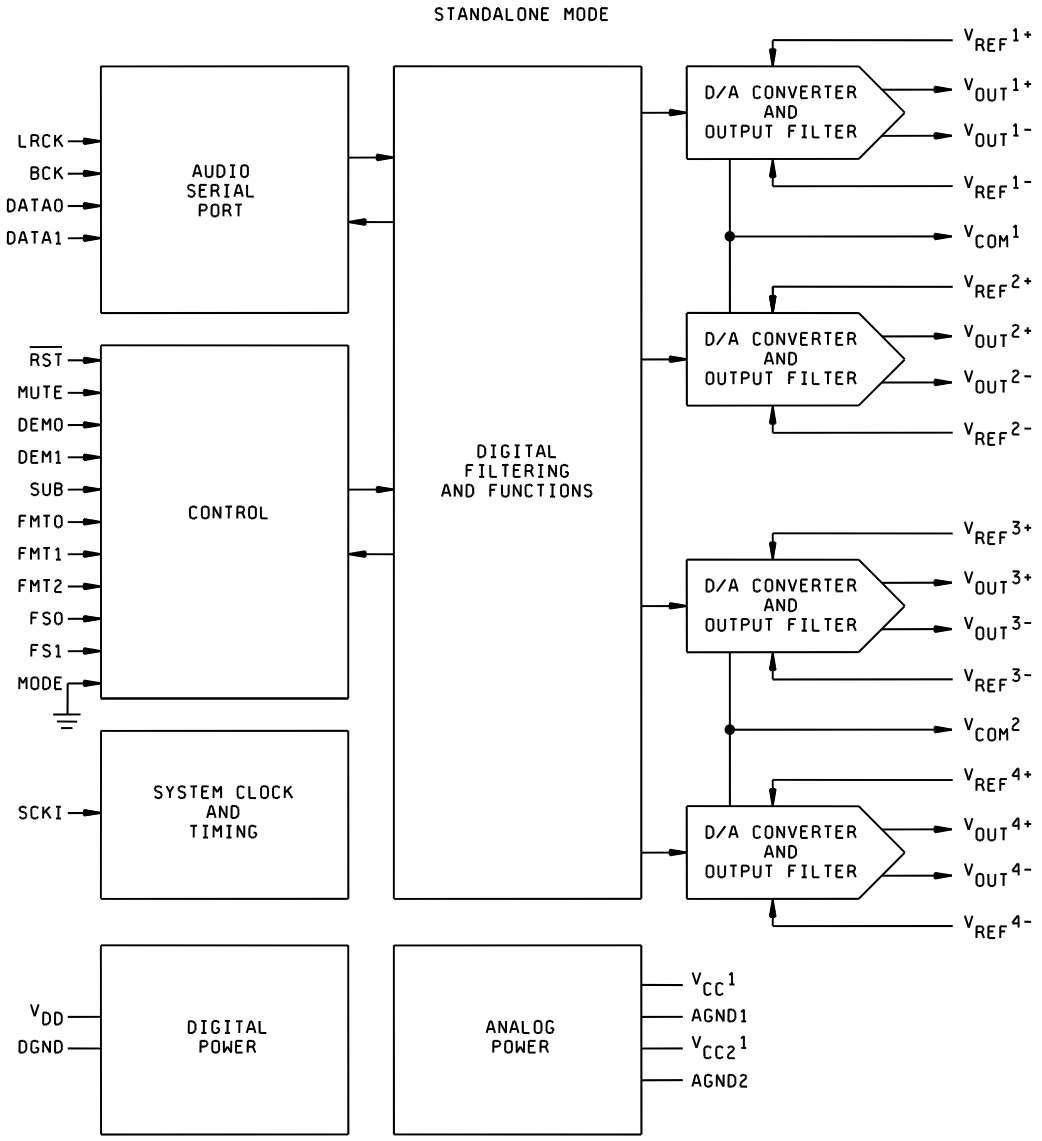

FIGURE 3. Block diagrams.

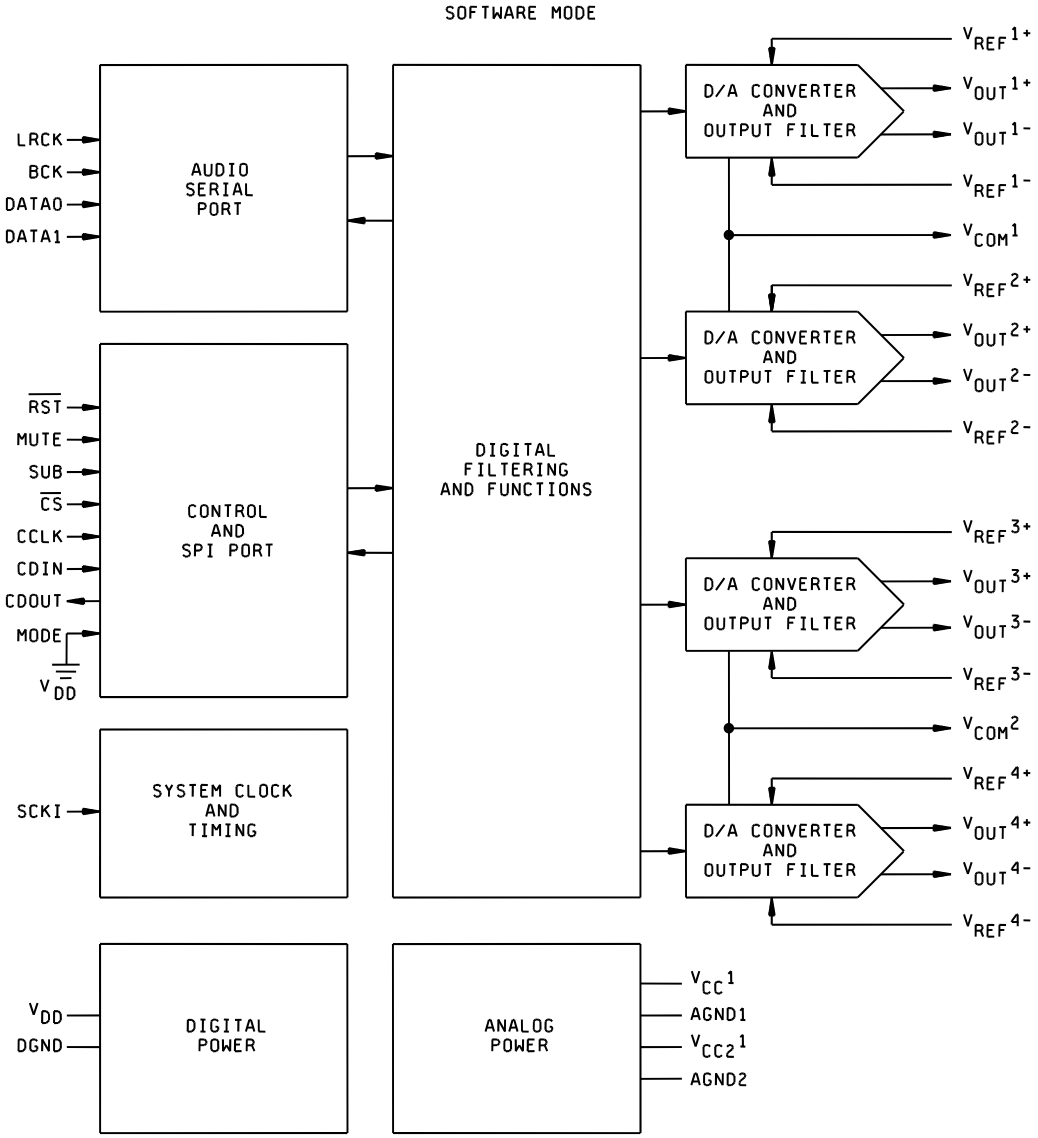

FIGURE 3. Block diagrams – Continued.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Package 2/	Top side marking	Vendor part number
V62/07643-01XE	01295	Tape and Reel, 2000	PCM4104EP	PCM4104IPFBREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ For the most current package and ordering information, see the package option addendum at the end of the manufacturer's datasheet, or at website www.ti.com.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. PO Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493