

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance crystal oscillator driver microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/07632</u> Drawing number	-	<u>01</u> Device type (See 1.2.1)	<u>X</u> Case outline (See 1.2.2)	<u>E</u> Lead finish (See 1.2.3)
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1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN74LVC1GX04-EP	Crystal oscillator driver

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	6	N/A	Plastic small outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (VCC).....	-0.5 V to 6.5 V
Input voltage range (VI)	-0.5 V to 6.5 V 2/
Voltage range applied to Y output in the high impedance or power off state (VO)	-0.5 V to 6.5 V 2/
Voltage range applied to any output in the high or low state (VO)	-0.5 V to VCC +0.5 V 2/ 3/
Maximum input clamp current (IIK) (VI < 0)	-50 mA
Maximum output clamp current (IOK) (VO < 0)	-50 mA
Maximum continuous output current (IO)	±50 mA
Maximum continuous current through VCC or GND	±100 mA
Maximum package thermal impedance (θJA)	142°C/W 4/
Storage temperature range (TSTG)	-65°C to 150°C

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ The input negative voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

3/ This value of VCC is provided in the recommended operating conditions stable.

4/ The package thermal impedance is calculated in accordance with JESD 51-7.

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1.4 Recommended operating conditions. 5/

Supply voltage range (VCC):	
Operating	1.65 V to 5.5 V
Minimum data retention only	1.5 V
Minimum crystal oscillator use	2.0 V
Minimum high level input voltage, (VIH) with (VCC = 1.65 V to 5.5 V)	0.75 x VCC
Maximum low level input voltage, (VIL) with (VCC = 1.65 V to 5.5 V)	0.25 x VCC
Input voltage (Vi)	0 V to 5.5 V
Output voltage (VO):	
X2, Y	0 to VCC
Y output only, Power down mode, VCC = 0 V	0 to 5.5 V
Maximum high level output current (IOH):	
VCC = 1.65 V	-4 mA
VCC = 2.3 V	-8 mA
VCC = 3 V	-16 mA
VCC = 3 V	-24 mA
VCC = 4.5 V	-32 mA
Maximum low level output current (IOL):	
VCC = 1.65 V	4 mA
VCC = 2.3 V	8 mA
VCC = 3 V	16 mA
VCC = 3 V	24 mA
VCC = 4.5 V	32 mA
Maximum input transition rise or fall rate ($\Delta t/\Delta v$):	
VCC = 1.8 V \pm 0.15 V, 2.5 V \pm 0.2 V	20 ns/V
VCC = 3.3 V \pm 0.3 V	10 ns/V
VCC = 5.0 V \pm 0.5 V	10 ns/V
Operating free-air temperature range (TA)	-55°C to +125°C

5/ All unused inputs of the device must be held at VCC or GND to ensure proper device operation.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

- EIA/JEDEC 51-7 – High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at <https://www.jedec.org>.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

- A. Manufacturer’s name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Function table. The Function table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Load circuit and timing waveforms. The load circuit and timing waveforms shall be as shown in figure 5.

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TABLE I. Electrical performance characteristics. 1/

Test		Symbol	Conditions -55°C ≤ TA ≤ 125°C unless otherwise specified	VCC	Limits		Unit
					Min	Max	
High level output voltage	VOH	IOH = -100 µA	1.65 V to 5.5 V	VCC - 0.1		V	
		IOH = -4 mA	1.65 V	1.2			
		IOH = -8 mA	2.3 V	1.9			
		IOH = -16 mA	3.0 V	2.4			
		IOH = -24 mA		2.3			
		IOH = -32 mA	4.5 V	3.8			
Low level output voltage	VOL	IOL = 100 µA	1.65 V to 5.5 V		0.1	V	
		IOL = 4 mA	1.65 V		0.45		
		IOL = 8 mA	2.3 V		0.3		
		IOL = 16 mA	3.0 V		0.4		
		IOL = 24 mA			0.63		
		IOL = 32 mA	4.5 V		0.70		
Input current	X1	II	VI = 5.5 V or GND	0 to 5.5 V		±5	µA
Off current	X1, Y	Ioff	VI or VO = 5.5 V	0		±10	µA
Supply current		ICC	VI = 5.5 V or GND, IO = 0,	1.65 V to 5.5V		10	µA
Input capacitance		CI	VI = VCC or GND, TA = 25°C	3.3 V	7 typical		pF

Test	Symbol	Conditions -55°C ≤ TA ≤ 125°C unless otherwise specified	VCC = 3.3 V ±0.3 V		VCC = 5.0 V ±0.5 V		Unit
			Min	Max	Min	Max	
Switching characteristics							
Propagation delay time, from input X1 to output X2	tpd	CL = 30 pF or 50 pF, See figure 5	0.8	3.7	0.8	3.2	ns
Propagation delay time, from input X1 to output Y 2/			2	7.8	2	5	

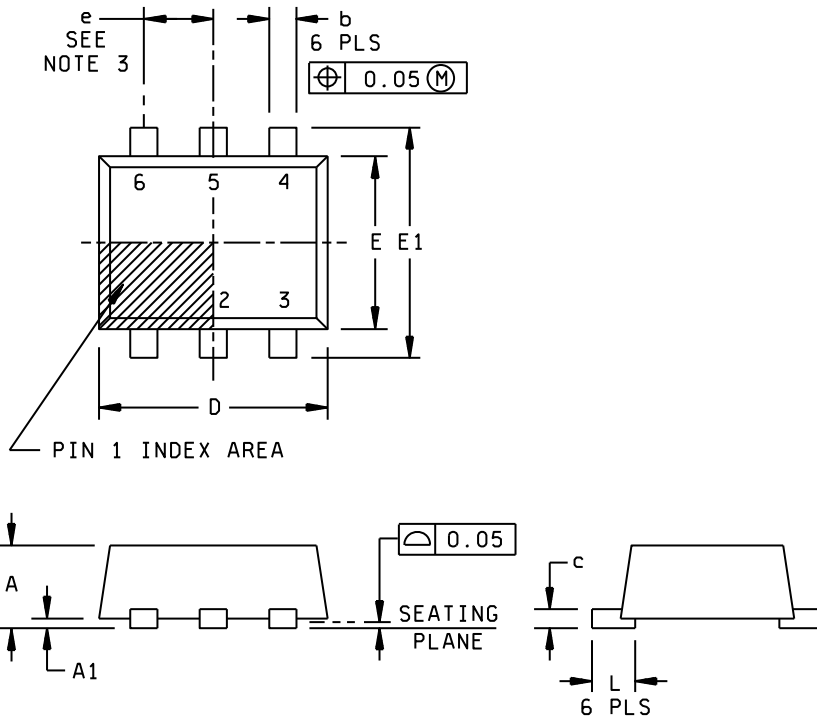
Test	Symbol	Conditions -55°C ≤ TA ≤ 125°C unless otherwise specified	VCC = 3.3 V		VCC = 5.0 V		Unit
			Min	Max	Min	Max	
Operating characteristics							
Power dissipation capacitance	Cpd	f = 10 MHz, TA = 25°C	24 typical		35 typical		pF

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ X2 – no external load.

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Case X



Dimension					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		0.60	E	1.10	1.30
A1	0.00	0.05	E1	1.50	1.70
b	0.15	0.27	e	0.50 BSC	
c	0.08	0.18	L	0.20	0.40
D	1.50	1.70			

NOTES:

1. This drawing is subject to change without notice.
2. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per end or side.
3. JEDEC package is pending.

FIGURE 1. Case outline.

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Case X

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	NC	4	X2
2	GND	5	Vcc
3	X1	6	Y

NC = No internal connection

FIGURE 2. Terminal connections.

Input X1	Outputs	
	X2	Y
H	L	H
L	H	L

FIGURE 3. Function table.

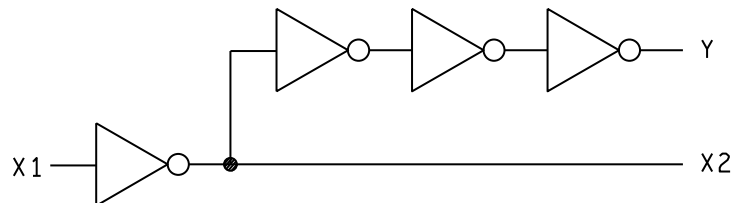
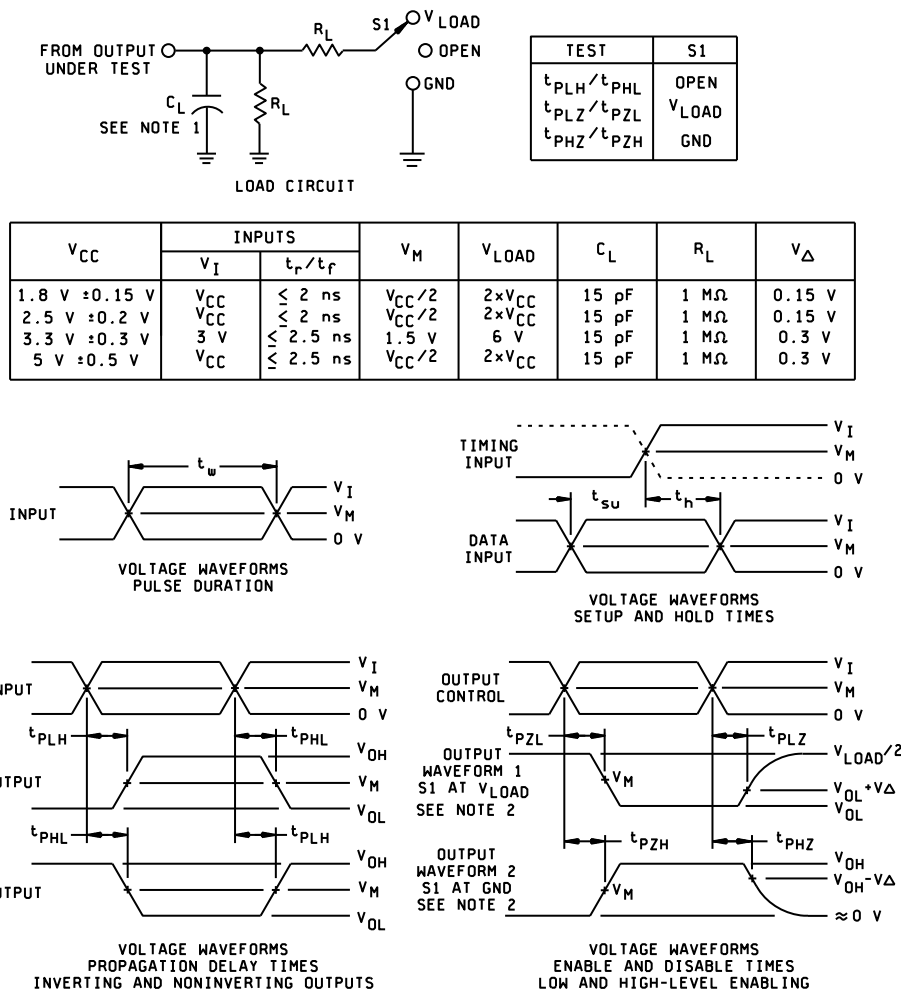


FIGURE 4. Logic diagram.

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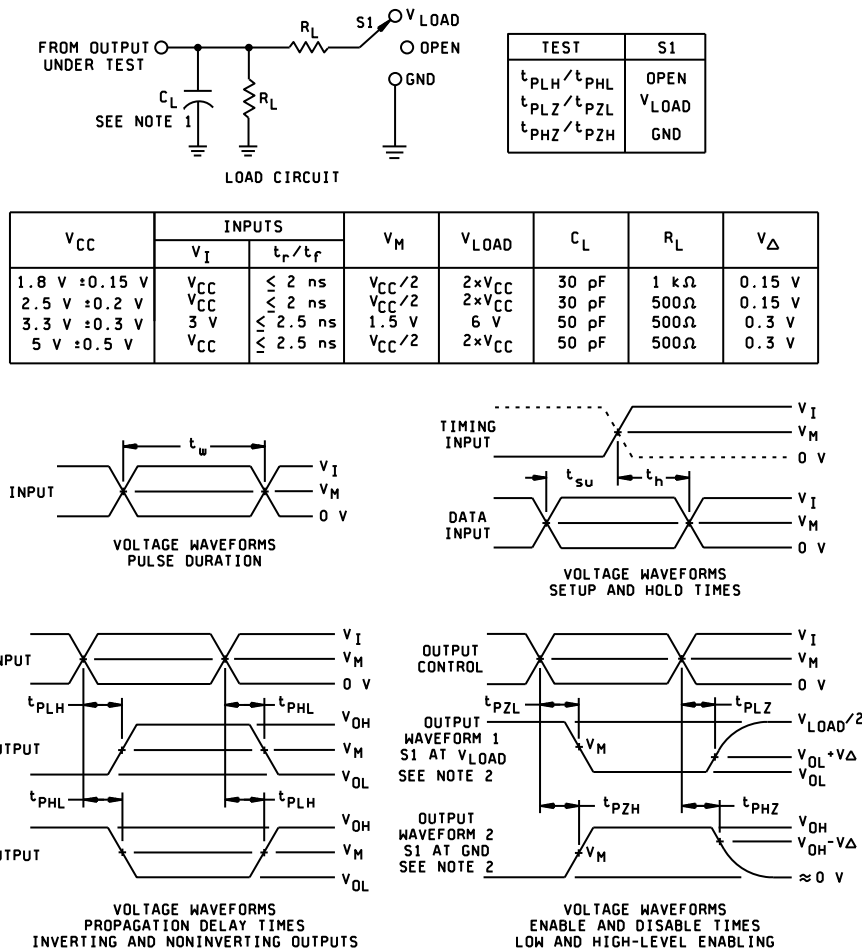


NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$.
4. The outputs are measured one at a time with one input transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
6. t_{PZL} and t_{PZH} are the same as t_{en} .
7. t_{PHL} and t_{PLH} are the same as t_{pd} .
8. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and timing waveforms.

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NOTES:

1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$.
4. The outputs are measured one at a time with one input transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
6. t_{PZL} and t_{PZH} are the same as t_{en} .
7. t_{PHL} and t_{PLH} are the same as t_{pd} .
8. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Load circuit and timing waveforms - Continued.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number ^{1/}	Device manufacturer CAGE code	Top side marking	Vendor part number
V62/07632-01XE	01295	CDD	CLVC1GX04MDRLREP

^{1/} The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest lane
P.O. Box 660199
Dallas, TX 75243

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