REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Update boilerplate to current MIL-PRF-38535 requirements. - PHN	15-02-24	Thomas M. Hess
B	Update boilerplate paragraphs to current VID description requirements. - PHN	22-01-18	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																						
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REV STATUS OF PAGES	**REV**			B	B	B	B	B	B	B	B	B										
	PAGE			1	2	3	4	5	6	7	8	9										

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO**
Original date of drawing YY-MM-DD 07-10-03	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, DIGITAL, 12 BIT ASYNCHRONOUS BINARY COUNTERS, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/07630**
	REV **B**	**PAGE** 1 **OF** 9

AMSC N/A

5962-V006-22

DISTRIBUTION STATEMENT A. Approved for public release. *Distribution is unlimited.*

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 12 bit asynchronous binary counters, with an operating temperature range of -55°C to +125°.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/07630	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74LV4040A	12 bit asynchronous binary counters

1.2.2 Case outlines. The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	MO-153	Plastic small-outline

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.5 V to +7.0 V
Input voltage range (V_I) ..... -0.5 V to 7.0 V 2/
Voltage range applied to any output in the high impedance or power off state ..... -0.5 V to 7.0 V 2/
Output voltage range (V_O) ..... -0.5 V to V_{CC} + 0.5 V 2/ 3/
Input clamp current (I_{IK}) ($V_I < 0$) ..... -20 mA
Output clamp current (I_{OK}) ($V_O < 0$) ..... -50 mA
Continuous output current (I_O) (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND ..... ±50 mA
Package thermal impedance (θ_{JA}): ..... 108°C/W 4/
Storage temperature range (T_{STG}) ..... -65°C to 150°C

1.4 Recommended operating conditions. 5/

Supply voltage range (V_{CC}) ..... 2.0 V to 5.5 V
Minimum high level input voltage
- V_{CC} = 2.0 V ..... 1.5 V
- V_{CC} = 2.3 V to 2.7 V ..... 0.7 x V_{CC}
- V_{CC} = 3 V to 3.6 V ..... 0.7 x V_{CC}
- V_{CC} = 4.5 V to 5.5 V ..... 0.7 x V_{CC}

Maximum high level input voltage
- V_{CC} = 2.0 V 0.5V
- V_{CC} = 2.3 V to 2.7 V ..... 0.3 x V_{CC}
- V_{CC} = 3 V to 3.6 V ..... 0.3 x V_{CC}
- V_{CC} = 4.5 V to 5.5 V ..... 0.3 x V_{CC}

Input voltage (V_I) ..... 0 V to 5.5 V
Output voltage (V_O) ..... 0 to V_{CC}
Maximum high level output current (I_{OH}):
- V_{CC} = 2.0 V ..... -50 µA
- V_{CC} = 2.3 V to 2.7 V ..... -2 mA
- V_{CC} = 3 V to 3.6 V ..... -6 mA
- V_{CC} = 4.5 V to 5.5 V ..... -12 mA

Maximum low level output current (I_{OL}):
- V_{CC} = 2.0 V ..... 50 µA
- V_{CC} = 2.3 V to 2.7 V ..... 2 mA
- V_{CC} = 3 V to 3.6 V ..... 6 mA
- V_{CC} = 4.5 V to 5.5 V ..... 12 mA

Maximum input transition rise or fall rate ($\Delta t/\Delta v$) :
- V_{CC} = 2.3 V to 2.7 V ..... 200 ns/V
- V_{CC} = 3 V to 3.6 V ..... 100 ns/V
- V_{CC} = 4.5 V to 5.5 V ..... 20 ns/V

Operating free-air temperature range (T_A) ..... -55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
3/ The value is limited to 5.5 V maximum.
4/ The package thermal impedance is calculated in accordance with JESD 51-7.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
JESD51-7	–	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

(Copies of these documents are available online at https://www.jedec.org).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Function table. The function table shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Terminal connections. The terminal connections shall be as shown in figure 4.

3.5.5 Test circuit and timing waveforms. The test circuit and timing waveforms shall be as shown in figure 5.

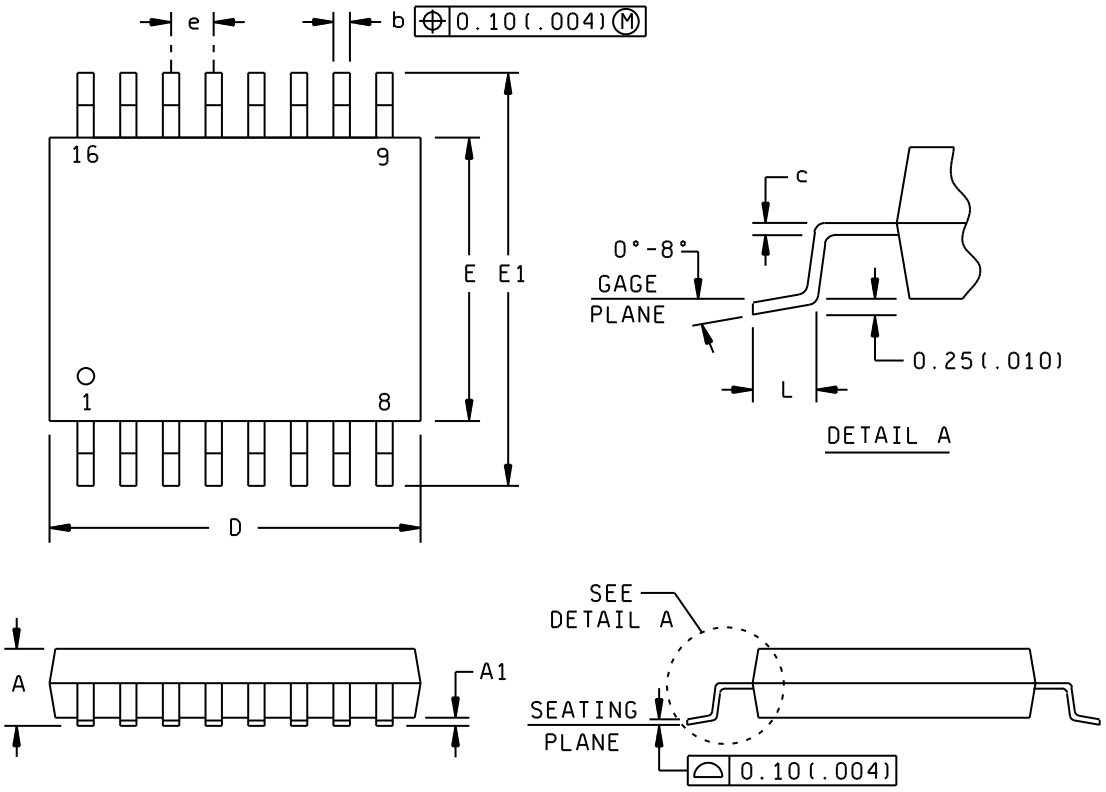
TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions $-55°C \le T_A \le 125°C$ unless otherwise specified	V_{CC}	Limits		Unit
				Min	Max	
High level output voltage	V_{OH}	I_{OH} = -50 µA	2.0 V to 5.5 V	V_{CC} – 0.1		V
		I_{OH} = -2 mA	2.3 V	2.0		
		I_{OH} = -6 mA	3.0 V	2.48		
		I_{OH} = -12 mA	4.5 V	3.8		
Low level output voltage	V_{OL}	I_{OL} = 50 µA	1.65 V to 5.5 V		0.1	V
		I_{OL} = 2 mA	1.65V		0.4	
		I_{OL} = 6 mA	2.3 V		0.44	
		I_{OL} = 12 mA	4.5 V		0.55	
Input current	I_I	V_I = 5.5 V or GND	0 to 5.5 V		±1	µA
Supply current	I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0,	5.5V		20	µA
Off current	I_{off}	V_I or V_O = 0 to 5.5 V	0		5	µA
Input capacitance	C_i	$V_I = V_{CC}$ or GND, T_A = 25°C	3.3 V	1.9 TYP		pF
Power dissipation capacitance	C_{pd}	CL = 50 pF, f = 10 MHz, T_A = 25°C	3.3 V	11.9 TYP		
			5.0 V	13.1 TYP		
Noise characteristics						
Quiet output, maximum dynamic V_{OL}	$V_{OL(P)}$	CL = 50 pF, T_A = 25°C	3.3 V		0.8	V
Quiet output, minimum dynamic V_{OL}	$V_{OL(V)}$				-0.8	
High level dynamic input voltage	$V_{IH(D)}$			2.31		
Low level dynamic input voltage	$V_{IL(D)}$				0.99	

Test	Symbol		Conditions $-55°C \le T_A \le 125°C$ unless otherwise specified	V_{CC} = 2.5 V ±0.2 V		V_{CC} = 3.3 V ±0.3 V		V_{CC} = 5.0 V ±0.5 V		Unit
				Min	Max	Min	Max	Min	Max	
Timing requirements										
Pulse duration	t_w		CLK high or low	7		5		5		ns
			CLR high	6.5		5		5		
Setup time	t_{su}		CLR inactive before CLK↓	6.5		5		5		
Switching characteristics										
Maximum frequency	f_{max}		C_L = 50 pF	35		50		80		MHz
Propagation delay from input $\overline{CLK}$ to output Q_A	t_{PLH}				28		17.5		10.5	ns
	t_{PHL}				28		17.5		10.5	
Propagation delay from input CLR to any output Q	t_{PHL}				28		18.5		12.0	
Propagation delay from input Q_n to output Q_{n+1}	Δt_{pd}				10.8		6.6		5.5	

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

Case X



Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	---	1.20	E	4.30	4.50
A1	0.05	0.15	E1	6.20	6.60
b	0.19	0.30	e	0.65 BSC	
c	0.15 NOM		L	0.50	0.75
D	4.90	5.10			

NOTES:
1. All linear dimensions are in millimeters(inches).
2. This case outline is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 millimeters.
4. Fall within JEDEC MO-153.

FIGURE 1. Case outlines - Continued.

Inputs		Function
CLK	CLR	
↑	L	No change
↓	L	Advance to next stage
X	H	All outputs L

FIGURE 2. Function table.

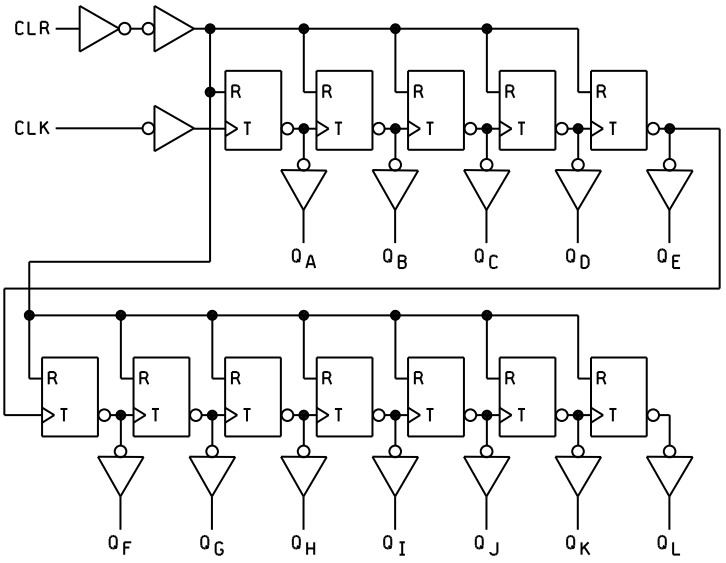
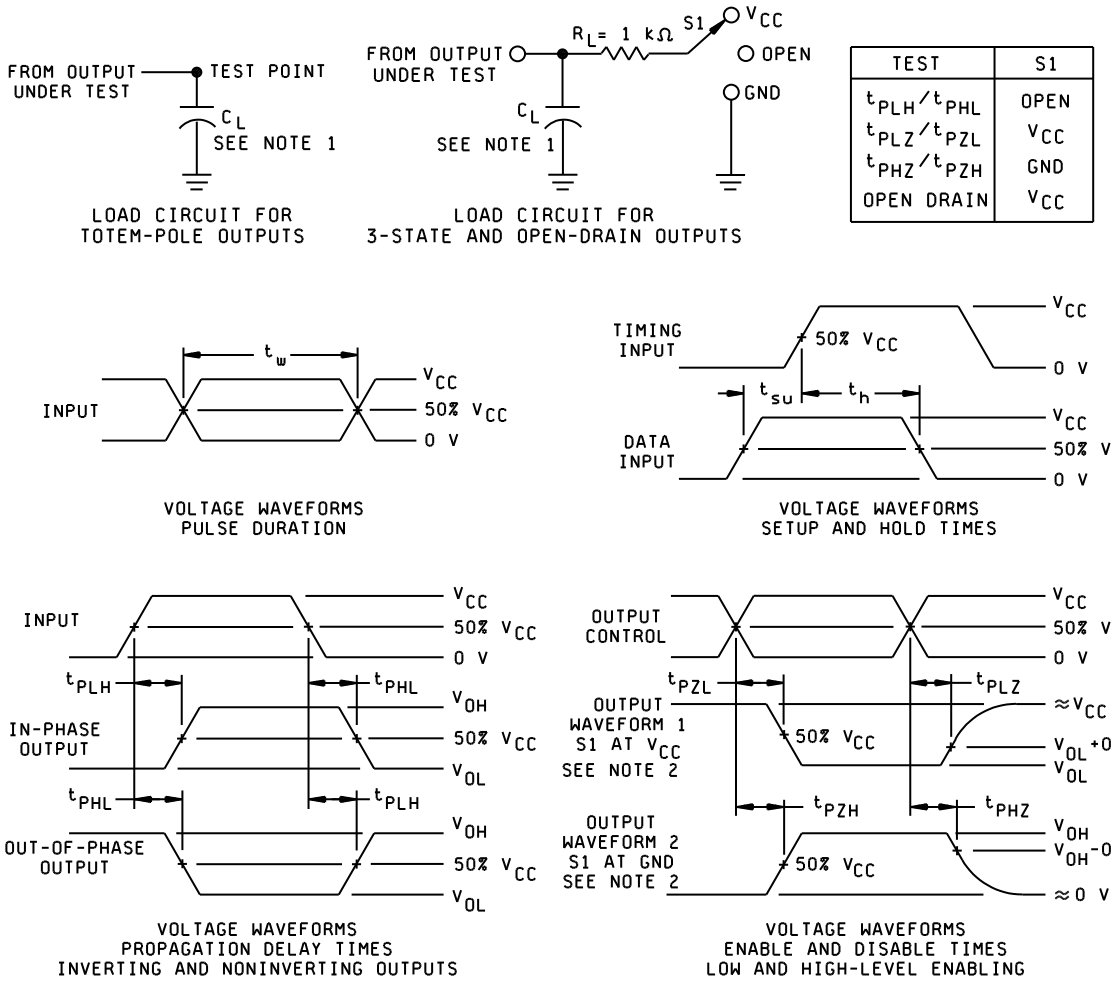


FIGURE 3. Logic diagram.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	Q_L	9	Q_A
2	Q_F	10	CLK
3	Q_E	11	CLR
4	Q_G	12	Q_I
5	Q_D	13	Q_H
6	Q_C	14	Q_J
7	Q_B	15	Q_K
8	GND	16	V_{CC}

FIGURE 4. Terminal connections.



NOTES:
1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
4. The outputs are measured one at a time with one input transition per measurement.
5. All parameters and waveforms are not applicable to all devices.

FIGURE 5. Test circuit and timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/07630-01XE	01295	SN74LV4040AMPWREP	LW040A

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243