

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Correct the vendor part number from SN65LVDS31MDTEP to SN65LVDS31MDREP. Make change to the VOC(PP) test by deleting 150 mV maximum and replacing with 50 mV typical.. - ro	14-03-24	C. SAFFLE

Prepared in accordance with ASME Y14.24

Vendor item drawing

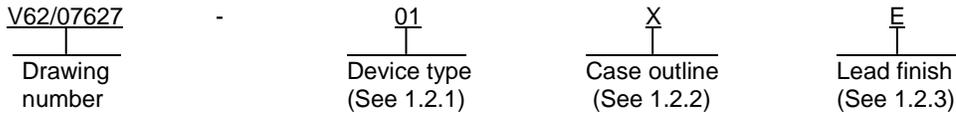
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REV STATUS OF PAGES	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A				
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PMIC N/A	PREPARED BY RICK OFFICER	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil/	
Original date of drawing YY-MM-DD 11-11-01	CHECKED BY RAJESH PITHADIA	TITLE MICROCIRCUIT, DIGITAL-LINEAR, DIFFERENTIAL LINE DRIVER, MONOLITHIC SILICON	
	APPROVED BY CHARLES F. SAFFLE		
	SIZE A	CODE IDENT. NO. 16236	DWG NO. V62/07627
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1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance differential line driver microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	SN65LVDS31-EP	High speed differential line driver

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	16	MS-012-AC	Plastic small outline surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to 4 V 2/
Input voltage range (V_I)	-0.5 V to $V_{CC} + 0.5$ V
Continuous total power dissipation (P_D)	See paragraph 1.5.
Junction temperature range (T_J)	+150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	+260°C
Storage temperature range (T_{STG})	-65°C to +150°C
Thermal resistance, junction to ambient (θ_{JC})	36.9°C/W
Thermal resistance, junction to ambient (θ_{JA})	73°C/W

1.4 Recommended operating conditions. 3/

Supply voltage range (V_{CC})	3 V to 3.6 V
High level input voltage (V_{IH})	2 V minimum
Low level input voltage (V_{IL})	0.8 V maximum
Operating free-air temperature range (T_A)	-55°C to +125°C

1.5 Dissipation ratings.

Package	Power rating $T_A < 25^\circ\text{C}$	Derating factor above $T_A = 25^\circ\text{C}$ 4/	Power rating $T_A = 70^\circ\text{C}$	Power rating $T_A = 85^\circ\text{C}$	Power rating $T_A = 125^\circ\text{C}$
Case X	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ All voltages, except differential I/O bus voltages, are with respect to the network ground terminal.

3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

4/ This is the inverse of the junction to ambient thermal resistance when board mounted and with no air flow.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at <http://www.jedec.org>)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figures 4, 5, 6, and 7.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Differential output voltage magnitude	V _{OD}	R _L = 100 Ω, see figure 5	-55°C to +125°C	01	247	454	mV
Change in differential output voltage magnitude between logic states	ΔV _{OD}	R _L = 100 Ω, see figure 5	-55°C to +125°C	01	-50	50	mV
Steady state common mode output voltage	V _{OC(SS)}	See figure 6	-55°C to +125°C	01	1.125	1.375	V
Change in steady state common mode output voltage between logic states	ΔV _{OC(SS)}	See figure 6	-55°C to +125°C	01	-50	50	mV
Peak to peak common mode output voltage	V _{OC(PP)}	See figure 6	-55°C to +125°C	01	50 typical		mV
Supply current	I _{CC}	V _I = 0.8 V or 2 V, enabled, no load	-55°C to +125°C	01		20	mA
		V _I = 0.8 V or 2 V, enabled, R _L = 100 Ω				35	
		V _I = 0 or V _{CC} , disabled				1	
High level input current	I _{IH}	V _{IH} = 2 V	-55°C to +125°C	01		20	μA
Low level input current	I _{IL}	V _{IL} = 0.8 V	-55°C to +125°C	01		10	μA
Short circuit output current	I _{OS}	V _{O(Y)} or V _{O(Z)} = 0	-55°C to +125°C	01		-24	mA
		V _{OD} = 0				±12	
High impedance output current	I _{OZ}	V _O = 0 or 2.4 V	-55°C to +125°C	01		±1	μA
Power off output current	I _{O(OFF)}	V _{CC} = 0, V _O = 2.4 V	-55°C to +125°C	01		±4	μA
Input capacitance	C _{IN}	V _{CC} = 3.3 V	+25°C	01	3 typical		pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Propagation delay time, low to high level output	t _{PLH}	R _L = 100 Ω, C _L = 10 pF, see figure 5	-55°C to +125°C	01	0.5	4	ns
Propagation delay time, high to low level output	t _{PHL}	R _L = 100 Ω, C _L = 10 pF, see figure 5	-55°C to +125°C	01	1	4.5	ns
Differential output signal rise time (20% to 80%)	t _r	R _L = 100 Ω, C _L = 10 pF, V _{CC} = 3.3 V, see figure 5	+25°C	01	0.5 typical		ns
Differential output signal fall time (80% to 20%)	t _f	R _L = 100 Ω, C _L = 10 pF, V _{CC} = 3.3 V, see figure 5	+25°C	01	0.5 typical		ns
Pulse skew (t _{PHL} – t _{PLH})	t _{sk(p)}	R _L = 100 Ω, C _L = 10 pF, see figure 5	-55°C to +125°C	01		0.6	ns
Channel to channel ^{2/} output skew	t _{sk(o)}	R _L = 100 Ω, C _L = 10 pF, see figure 5	-55°C to +125°C	01		0.8	ns
Propagation delay time, high impedance to high level output	t _{pZH}	See figure 7	-55°C to +125°C	01		17	ns
Propagation delay time, high impedance to low level output	t _{pZL}	See figure 7	-55°C to +125°C	01		17	ns
Propagation delay time, high level to high impedance output	t _{PHZ}	See figure 7	-55°C to +125°C	01		18	ns
Propagation delay time, low level to high impedance output	t _{PLZ}	See figure 7	-55°C to +125°C	01		17	ns

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ t_{sk(o)} is the maximum delay time difference between drivers on the same device.

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Case X

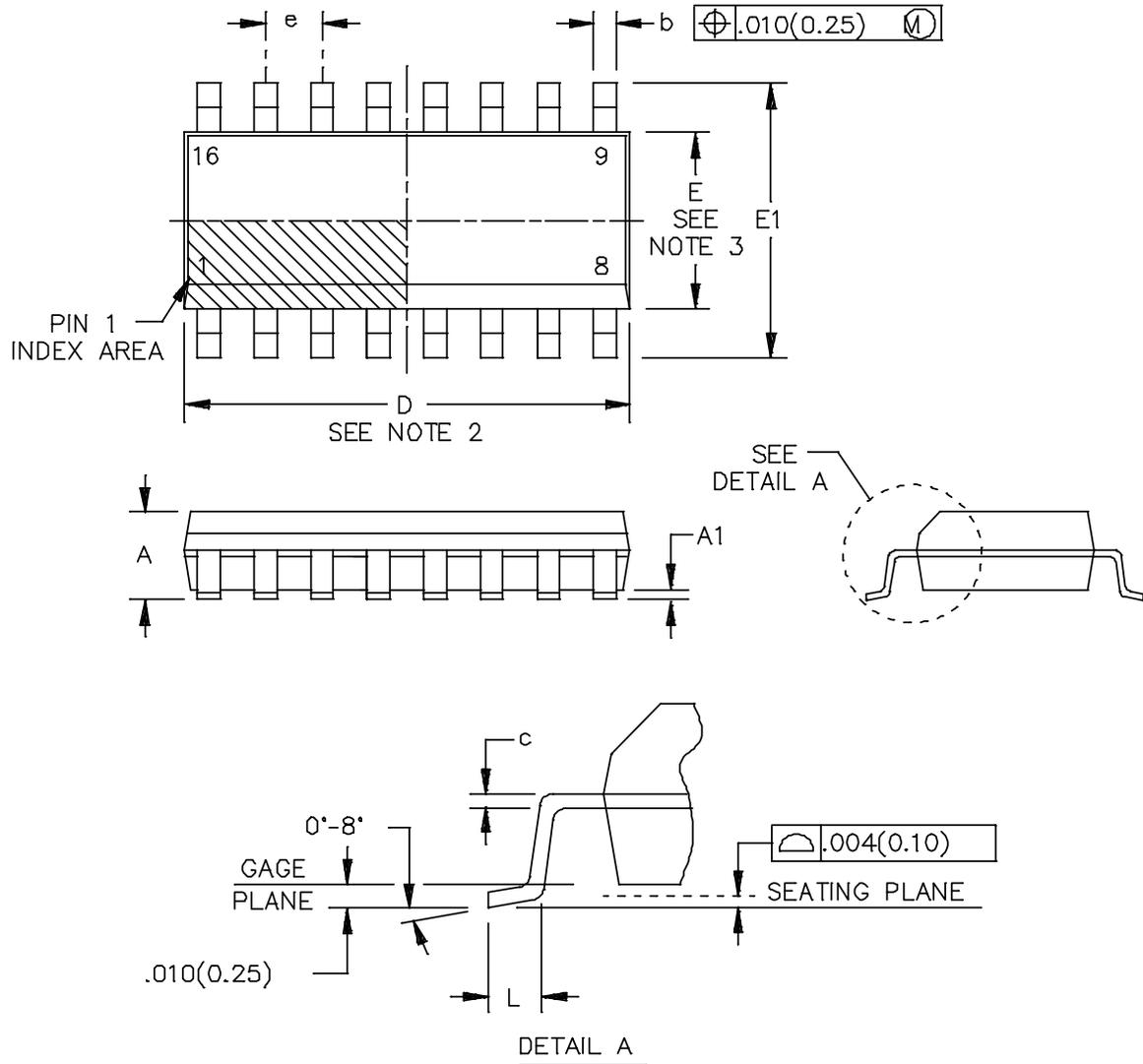


FIGURE 1. Case outline.

<p>DLA LAND AND MARITIME COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/07627</p>
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Case X – continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.069	---	1.75
A1	0.004	0.010	0.10	0.25
b	0.012	0.020	0.31	0.51
c	0.005	0.010	0.13	0.25
D	0.386	0.394	9.80	10.00
E	0.150	0.157	3.80	4.00
E1	0.228	0.244	5.80	6.20
e	0.050 BSC		1.27 BSC	
L	0.016	0.050	0.40	1.27

NOTES:

1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. For dimension D, body length does not include mold flash, protrusion, or gate burrs. Mold flash, protrusion, or gate burrs shall not exceed 0.006 inch (0.15 mm) each side.
3. For dimension E, body width does not include interlead flash. Interlead flash shall not exceed 0.017 inch (0.43 mm) each side.
4. Falls within reference to JEDEC MS-012-AC.

FIGURE 1. Case outline - Continued.

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Device type	01
Case outline	X
Terminal number	Terminal symbol
1	1A
2	1Y
3	1Z
4	G
5	2Z
6	2Y
7	2A
8	GND
9	3A
10	3Y
11	3Z
12	\bar{G}
13	4Z
14	4Y
15	4A
16	V _{CC}

FIGURE 2. Terminal connections.

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INPUT	ENABLES		OUTPUTS	
	G	\bar{G}	Y	Z
A	H	X	H	L
H	H	X	L	H
L	X	L	H	L
H	X	L	L	H
L	L	H	Z	Z
Open	H	X	L	H
Open	X	L	L	H

H = High level
 L = Low level
 X = Irrelevant
 Z = high impedance (off)

FIGURE 3. Truth table.

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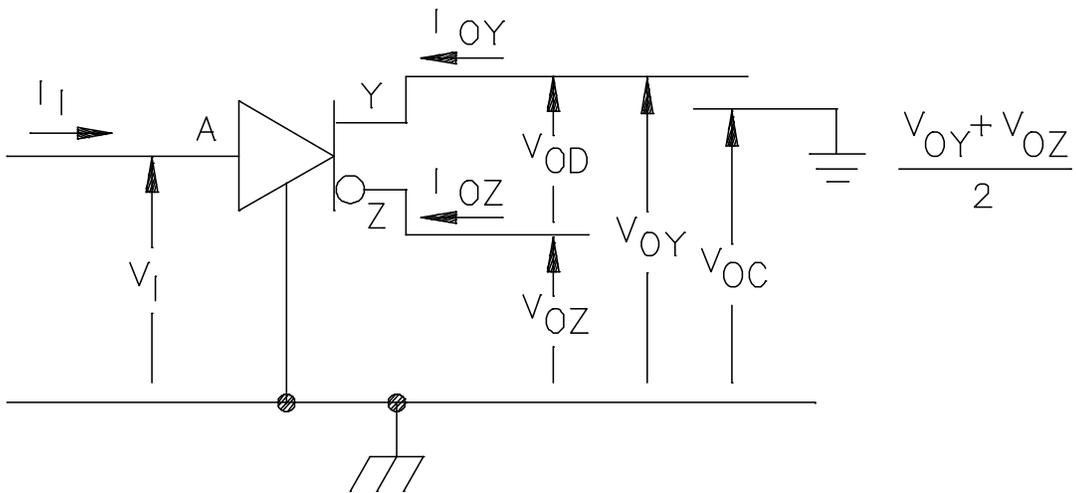
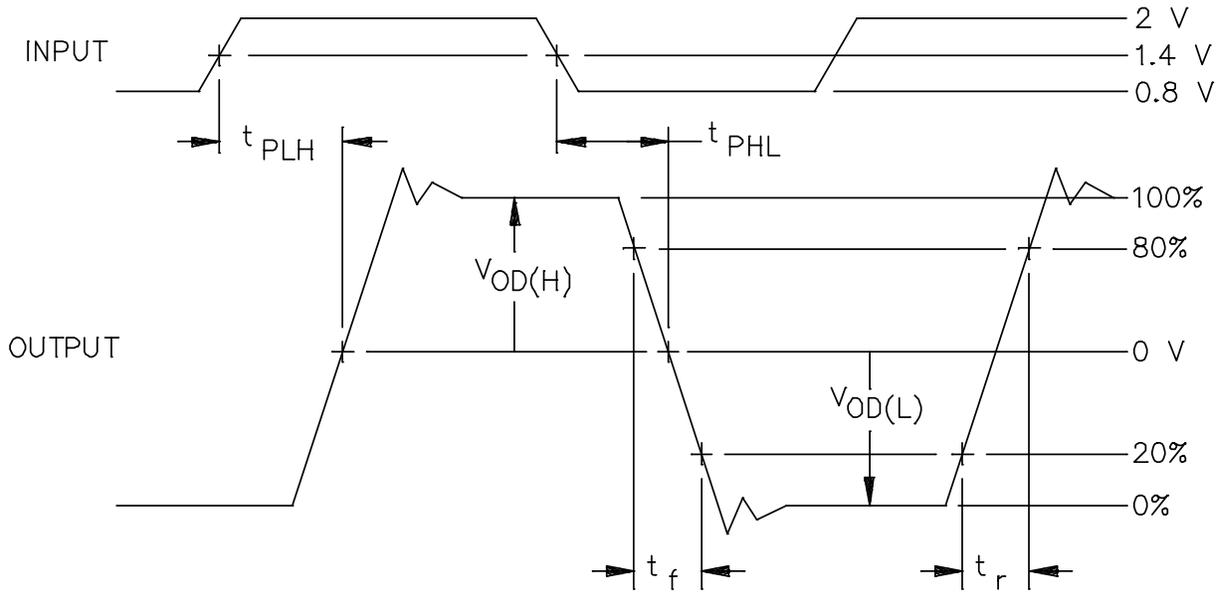
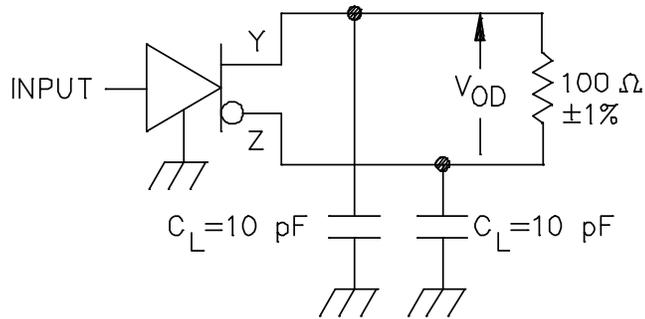


FIGURE 4. Voltage and current definitions.

<p>DLA LAND AND MARITIME COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/07627</p>
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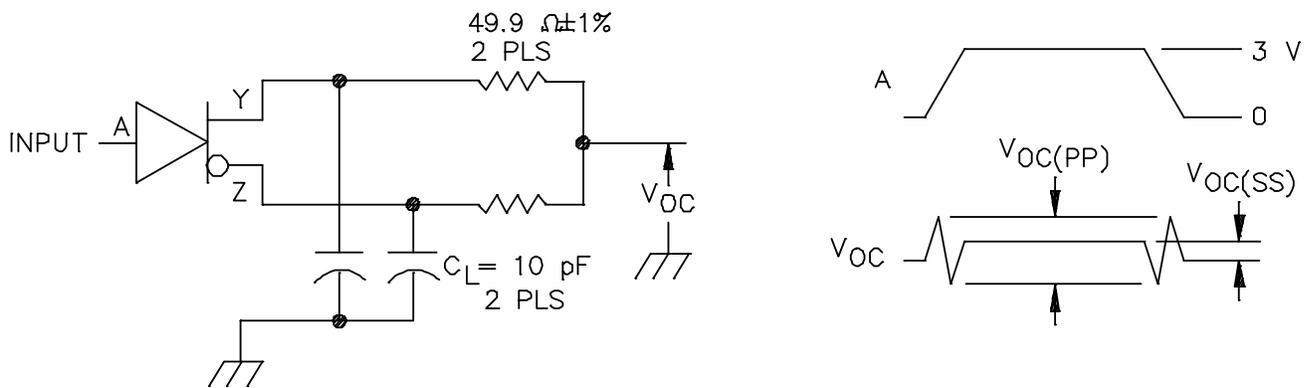


NOTES:

1. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.
2. C_L includes instrumentation and fixture capacitance within 6 mm of the device under test.

FIGURE 5. Timing waveforms and test circuit for the differential output signal.

<p align="center">DLA LAND AND MARITIME COLUMBUS, OHIO</p>	<p align="center">SIZE A</p>	<p align="center">CODE IDENT NO. 16236</p>	<p align="center">DWG NO. V62/07627</p>
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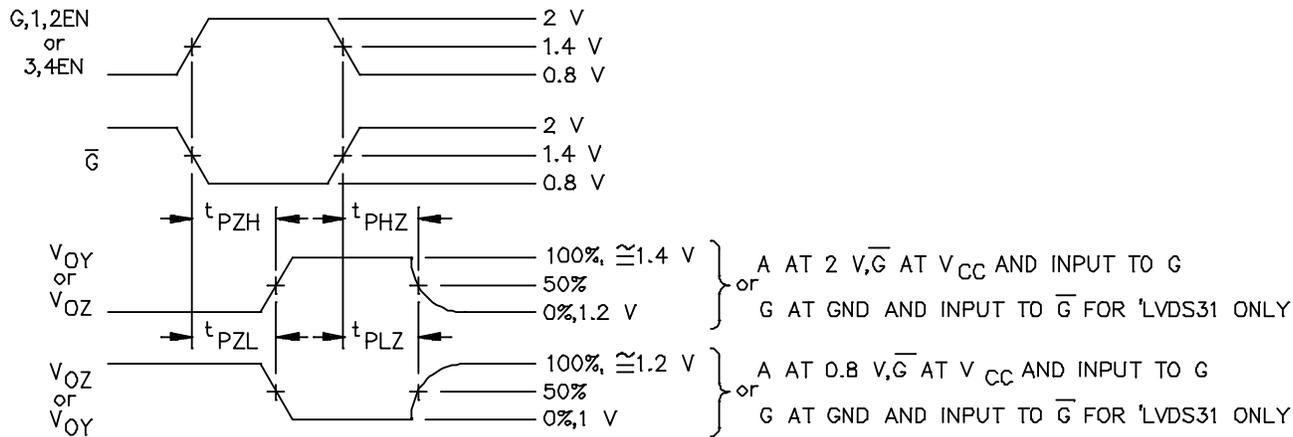
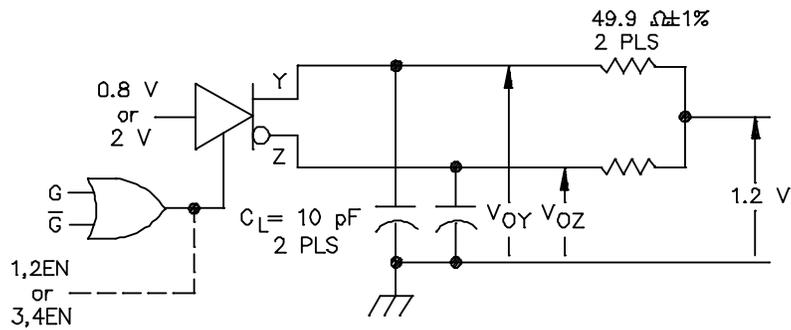


NOTES:

1. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.
2. C_L includes instrumentation and fixture capacitance within 6 mm of the device under test.
3. The measurement of V_{OC(PP)} is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

FIGURE 6. Timing waveforms and test circuit for the driver common mode output voltage.

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NOTES:

1. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns.
2. C_L includes instrumentation and fixture capacitance within 6 mm of the device under test.

FIGURE 7. Timing waveforms and test circuit for enable / disable.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Top siding marking	Vendor part number <u>2/ 3/</u>
V62/07627-01XE	01295	LVDS31EP	SN65LVDS31MDREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ For the most current package and ordering information, see manufacturer's website at www.ti.com.

3/ Package drawings, standard packaging quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available at www.ti.com/sc/package.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
 Semiconductor Group
 8505 Forest Lane
 P.O. Box 660199
 Dallas, TX 75243
 Point of contact: U.S. Highway 75 South
 P.O. Box 84, M/S 853
 Sherman, TX 75090-9493

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