REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Correct the top side marking identification to “SBLM” as specified under paragraph 6.3. - ro	07-12-11	R. HEBER
B	Update boilerplate to MIL-PRF-38535 requirements. - DRH	22-08-23	Muhammad A. Akbar

CURRENT DESIGN ACTIVITY CAGE CODE 16236
HAS CHANGED NAMES TO:
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	B	B	B	B	B	B	B	B	B	B	B	B	B									
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13									

PMIC N/A

Original date of drawing

07-03-22

PREPARED BY
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APPROVED BY
ROBERT H. HEBER

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
https://www.dla.mil/landandmaritime

TITLE
MICROCIRCUIT, DIGITAL, SINGLE SCHMITT TRIGGER INVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE	DWG NO.
A	16236	V62/07626
REV B		PAGE 1 OF 13

AMSC N/A

5962-V094-22

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance single schmitt trigger inverter microcircuit, with an operating temperature range of -40°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/07626	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	SN74LVC1G14-EP	Single schmitt trigger inverter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	5	MO-178-AA	Plastics surface mount

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V to 6.5 V
Input voltage range (V_I)	-0.5 V to 6.5 V 2/
Voltage range applied to any output in the high impedance or power off state (V_O)	-0.5 V to 6.5 V 2/
Voltage range applied to any output in the high or low state (V_O)	-0.5 V to V_{CC} +0.5 V 2/ 3/
Input clamp current (I_{IK}) ($V_I < 0$)	-50 mA maximum
Output clamp current (I_{OK}) ($V_O < 0$)	-50 mA maximum
Continuous output current (I_O)	±50 mA maximum
Continuous current through V_{CC} or GND	±100 mA maximum
Package thermal impedance (θ_{JA})	324°C/W maximum 4/
Storage temperature range (T_{STG})	-65°C to +150°C

1.4 Recommended operating conditions. 5/

Supply voltage range (V_{CC}):	
Operating	1.65 V to 5.5 V
Data retention only	1.5 V minimum
Input voltage (V_I)	0 V to 5.5 V
Output voltage (V_O)	0 V to V_{CC}
High level output current (I_{OH}):	
V_{CC} = 1.65 V	-4 mA maximum
V_{CC} = 2.3 V	-8 mA maximum
V_{CC} = 3 V	-16 mA maximum
V_{CC} = 3 V	-24 mA maximum
V_{CC} = 4.5 V	-32 mA maximum
Low level output current (I_{OL}):	
V_{CC} = 1.65 V	4 mA maximum
V_{CC} = 2.3 V	8 mA maximum
V_{CC} = 3 V	16 mA maximum
V_{CC} = 3 V	24 mA maximum
V_{CC} = 4.5 V	32 mA maximum
Operating free-air temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ The input and output negative voltage ratings may be exceeded if the input and output current ratings are observed.
3/ This value of V_{CC} is provided in the recommended operating conditions table.
4/ The package thermal impedance is calculated in accordance with JESD 51-2.
5/ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Truth table. The truth table shall be as shown in figure 3.

3.5.4 Logic diagram. The logic diagram shall be as shown in figure 4.

3.5.5 Timing waveforms and test circuit. The timing waveforms and test circuit shall be as shown in figures 5 and 6.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Electrical characteristics section							
Positive going input threshold voltage	V_{T+}	V_{CC} = 1.65 V	-55°C to +125°C	01	0.79	1.16	V
		V_{CC} = 2.3 V			1.11	1.56	
		V_{CC} = 3 V			1.5	1.87	
		V_{CC} = 4.5 V			2.16	2.74	
		V_{CC} = 5.5 V			2.61	3.33	
Negative going input threshold voltage	V_{T-}	V_{CC} = 1.65 V	-55°C to +125°C	01	0.39	0.62	V
		V_{CC} = 2.3 V			0.58	0.87	
		V_{CC} = 3 V			0.84	1.14	
		V_{CC} = 4.5 V			1.41	1.79	
		V_{CC} = 5.5 V			1.87	2.29	
Hysteresis (V_{T+} - V_{T-})	ΔV_T	V_{CC} = 1.65 V	-55°C to +125°C	01	0.37	0.62	V
		V_{CC} = 2.3 V			0.48	0.77	
		V_{CC} = 3 V			0.56	0.87	
		V_{CC} = 4.5 V			0.71	1.04	
		V_{CC} = 5.5 V			0.71	1.11	
High level output voltage	V_{OH}	I_{OH} = -100 μA, V_{CC} = 1.65 to 4.5 V	-55°C to +125°C	01	V_{CC} - 0.1		V
		I_{OH} = -4 mA, V_{CC} = 1.65 V			1.2		
		I_{OH} = -8 mA, V_{CC} = 2.3 V			1.9		
		I_{OH} = -16 mA, V_{CC} = 3 V			2.4		
		I_{OH} = -24 mA, V_{CC} = 3 V			2.3		
		I_{OH} = -32 mA, V_{CC} = 4.5 V			3.8		

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Electrical characteristics section – Continued.							
Low level output voltage	V_{OL}	I_{OL} = 100 µA, V_{CC} = 1.65 V to 4.5 V	-55°C to +125°C	01		0.1	V
		I_{OL} = 4 mA, V_{CC} = 1.65 V				0.45	
		I_{OL} = 8 mA, V_{CC} = 2.3 V				0.3	
		I_{OL} = 16 mA, V_{CC} = 3 V				0.4	
		I_{OL} = 24 mA, V_{CC} = 3 V				0.55	
		I_{OL} = 32 mA, V_{CC} = 4.5 V				0.55	
Input current, A input	I_I	V_I = 5.5 V or GND, V_{CC} = 0 to 5.5 V	-55°C to +125°C	01		±5	µA
Off current	I_{off}	V_I or V_O = 5.5 V, V_{CC} = 0 V	-55°C to +125°C	01		±10	µA
Supply current	I_{CC}	V_I = 5.5 V or GND, I_O = 0, V_{CC} = 1.65 V to 5.5 V	-55°C to +125°C	01		19	µA
Quiescent supply current	ΔI_{CC}	One input at V_{CC} – 0.6 V, other inputs at V_{CC} or GND, V_{CC} = 3 V to 5.5 V	-55°C to +125°C	01		500	µA
Input capacitance	C_I	V_I = V_{CC} or GND, V_{CC} = 3.3 V	+25°C	01	4.5 typical		pF

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Switching characteristics section.							
Propagation delay time, from input A to output Y	t_{pd}	V_{CC} = 1.8 V ±0.15 V, C_L = 15 pF, see figure 5	-55°C to +125°C	01	2.8	9.9	ns
		V_{CC} = 2.5 V ±0.2 V, C_L = 15 pF, see figure 5			1.6	5.5	
		V_{CC} = 3.3 V ±0.3 V, C_L = 15 pF, see figure 5			1.5	4.6	
		V_{CC} = 5 V ±0.5 V, C_L = 15 pF, see figure 5			0.9	4.4	
		V_{CC} = 1.8 V ±0.15 V, C_L = 30 pF or 50 pF, see figure 6			3.8	16	
		V_{CC} = 2.5 V ±0.2 V, C_L = 30 pF or 50 pF, see figure 6			2	7.5	
		V_{CC} = 3.3 V ±0.3 V, C_L = 30 pF or 50 pF, see figure 6			1.8	6.0	
		V_{CC} = 5 V ±0.5 V, C_L = 30 pF or 50 pF, see figure 6			1.2	5	
Operating characteristics section.							
Power dissipation capacitance	C_{pd}	f = 10 MHz, V_{CC} = 1.8 V	+25°C	01	20 typical		pF
		f = 10 MHz, V_{CC} = 2.5 V			21 typical		
		f = 10 MHz, V_{CC} = 3.3 V			22 typical		
		f = 10 MHz, V_{CC} = 5 V			25 typical		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

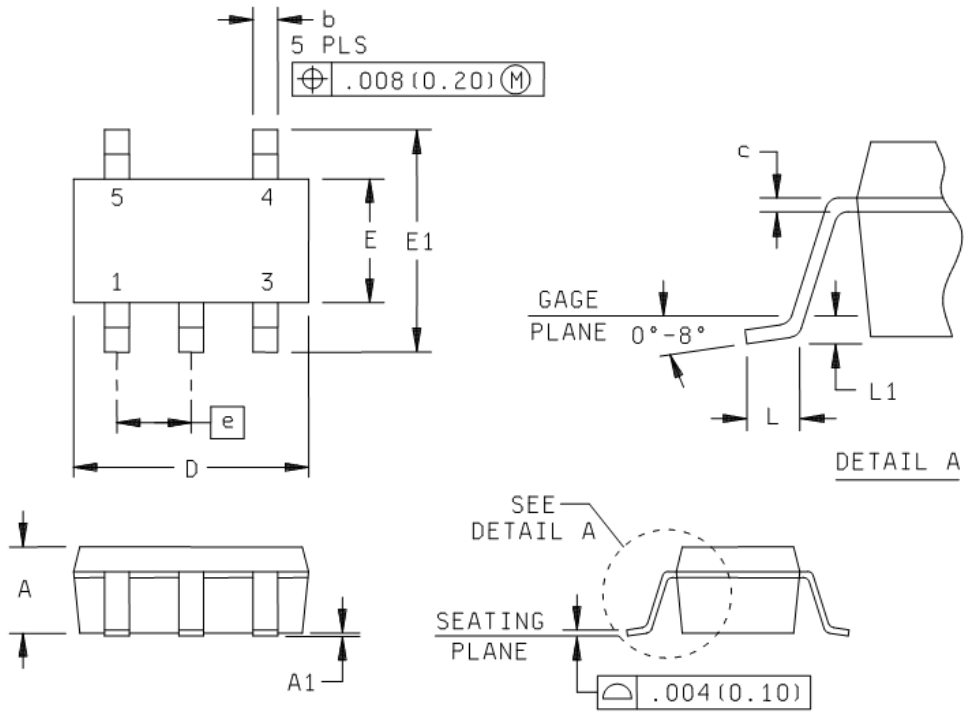


FIGURE 1. Case outline.

Symbol	Dimensions			
	Inch		Millimeters	
	Min	Max	Min	Max
A	---	.057	---	1.45
A1	.000	.005	0.00	0.15
b	.011	.019	0.30	0.50
c	.003	.008	0.08	0.22
D	.108	.121	2.75	3.05
E	.057	.068	1.45	1.75
E1	.102	.118	2.60	3.00
e	.037 BSC		0.95 BSC	
L	.011	.021	0.30	0.55
L1	.009 BSC		0.25 BSC	
n	5 leads		5 leads	

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 mm (0.006 inch) per side.
3. Falls with JEDEC MO-178 variation AA.

FIGURE 1. Case outline – Continued.

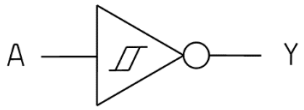
Device type 01	
Case outline X	
Terminal number	Terminal symbol
1	NC
2	A
3	GND
4	Y
5	V_{CC}

FIGURE 2. Terminal connections.

Input	Output
A	Y
H	L
L	H

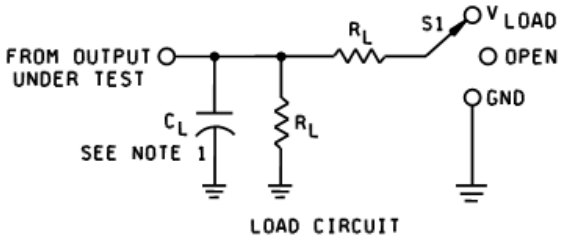
H = High voltage level
L = Low voltage level

FIGURE 3. Truth table.



(Positive logic)

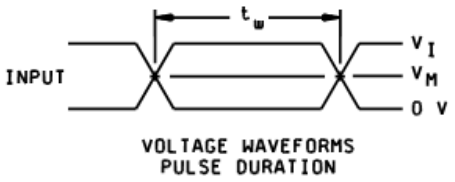
FIGURE 4. Logic diagram.



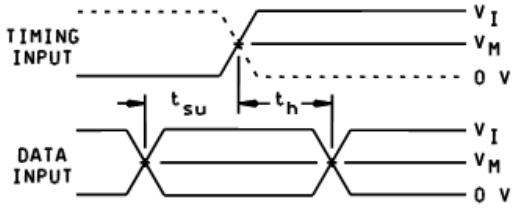
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

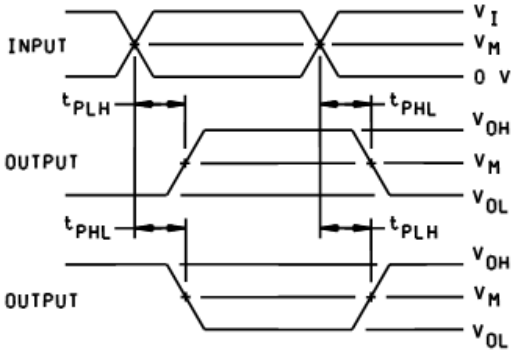
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ±0.15 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2\times V_{CC}$	15 pF	1 MΩ	0.15 V
2.5 V ±0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2\times V_{CC}$	15 pF	1 MΩ	0.15 V
3.3 V ±0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	15 pF	1 MΩ	0.3 V
5 V ±0.5 V	V_{CC}	≤ 2.5 ns	$V_{CC}/2$	$2\times V_{CC}$	15 pF	1 MΩ	0.3 V



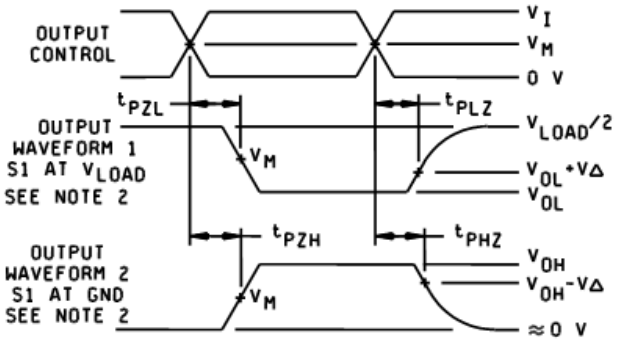
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



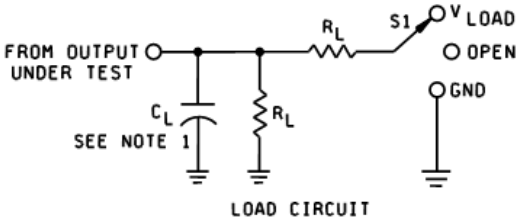
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW AND HIGH-LEVEL ENABLING

NOTES:
1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
4. The outputs are measured one at a time with one input transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
6. t_{PZL} and t_{PZH} are the same as t_{en}.
7. t_{PLH} and t_{PHL} are the same as t_{pd}.
8. All parameters and waveforms are not applicable to all devices.

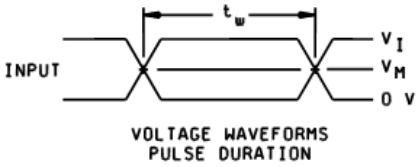
FIGURE 5. Timing waveforms and test circuit.



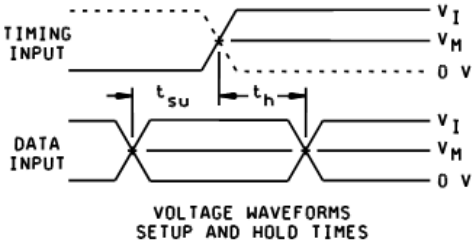
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

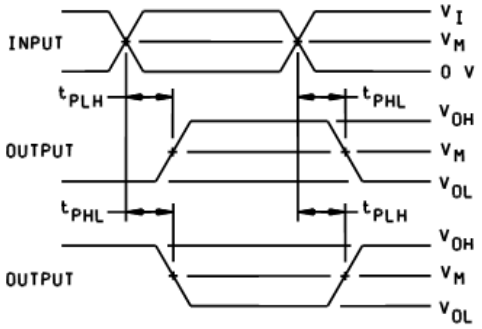
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ±0.15 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2\times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ±0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	$2\times V_{CC}$	30 pF	500Ω	0.15 V
3.3 V ±0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500Ω	0.3 V
5 V ±0.5 V	V_{CC}	≤ 2.5 ns	$V_{CC}/2$	$2\times V_{CC}$	50 pF	500Ω	0.3 V



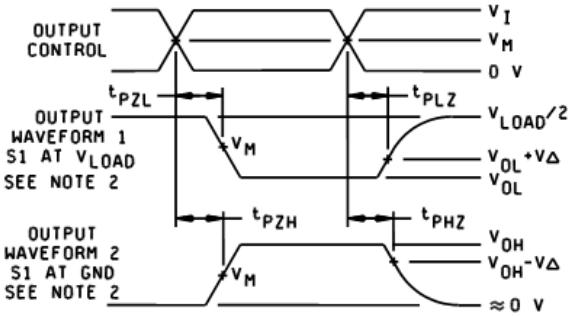
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW AND HIGH-LEVEL ENABLING

NOTES:
1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
4. The outputs are measured one at a time with one input transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
6. t_{PZL} and t_{PZH} are the same as t_{en}.
7. t_{PLH} and t_{PHL} are the same as t_{pd}.
8. All parameters and waveforms are not applicable to all devices.

FIGURE 6. Timing waveforms and test circuit.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Package 2/	Top side marking 3/	Vendor part number
V62/07626-01XE	01295	Reel of 3000	SBLM	SN74LVC1G14MDBVREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ For the most current package and ordering information, see the package option addendum at the end of this document, or see the Texas Instruments web site at www.ti.com.
3/ The actual top side marking has one additional character that designates the assembly/test site.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243